PCI-Express Gen-4: How far can a Bit travel before it needs to refuel?
PCI-Express Gen-4 System Topologies

Q1: How far can a Bit travel before it needs to refuel?

- System designers anticipate various topologies ranging from one to five connectors.
- High channel attenuation:
  - ~5 dB from CPU package
  - ~3 dB from End Point package
  - ~1 dB from each connector
  - ~1 dB / inch from PCB (FR4)

**PCle4 Spec: <20.5dB @8GHz**

→ ~10 inches end-to-end channel

- **Linear Repeaters** are commonly used to achieve reach extension while minimizing added latency, cost, and power consumption.
Root Complex Tx Parameters

Q2: How to find the optimum configuration of the system?

- Xilinx FPGA SerDes is used as the Root Complex Tx in this analysis.

<table>
<thead>
<tr>
<th>Preset</th>
<th>Pre-shoot (dB)</th>
<th>De-emphasis (dB)</th>
<th>c-1</th>
<th>c+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4</td>
<td>0.0</td>
<td>0.0</td>
<td>0.000</td>
<td>0.000</td>
</tr>
<tr>
<td>P1</td>
<td>0.0</td>
<td>-3.5 ± 1</td>
<td>0.000</td>
<td>-0.167</td>
</tr>
<tr>
<td>P0</td>
<td>0.0</td>
<td>-6.0 ± 1.5</td>
<td>0.000</td>
<td>-0.250</td>
</tr>
<tr>
<td>P9</td>
<td>3.5 ± 1</td>
<td>0.0</td>
<td>-0.166</td>
<td>0.000</td>
</tr>
<tr>
<td>P8</td>
<td>3.5 ± 1</td>
<td>-3.5 ± 1</td>
<td>-0.125</td>
<td>-0.125</td>
</tr>
<tr>
<td>P7</td>
<td>3.5 ± 1</td>
<td>-6.0 ± 1.5</td>
<td>-0.100</td>
<td>-0.200</td>
</tr>
<tr>
<td>P5</td>
<td>1.9 ± 1</td>
<td>0.0</td>
<td>-0.100</td>
<td>0.000</td>
</tr>
<tr>
<td>P6</td>
<td>2.5 ± 1</td>
<td>0.0</td>
<td>-0.125</td>
<td>0.000</td>
</tr>
<tr>
<td>P3</td>
<td>0.0</td>
<td>-2.5 ± 1</td>
<td>0.000</td>
<td>-0.125</td>
</tr>
<tr>
<td>P2</td>
<td>0.0</td>
<td>-4.4 ± 1.5</td>
<td>0.000</td>
<td>-0.200</td>
</tr>
</tbody>
</table>

De-emphasis = 20 log,10 Vb/Va
Pre-shoot = 20 log,10 Vc/Vb
Boost = 20 log,10 Vd/Vb

\[ v_{\text{out}} = v_{\text{in}} + c_1 \]
\[ |c_1| + |c_0| + |c_{-1}| = 1 \]
\[ c_{-1} \leq 0 \quad c_0 \leq 0 \]
Repeater Parameters

Q2: How to find the optimum configuration of the system?

- A Texas Instruments Linear Repeater is used to extend the reach between the RC and EP.
- 10 Repeater parameters
- Two major mechanisms for signal conditioning:
  - High-frequency boost (BST1 and BST2, 6 values for each)
  - Wide-band amplitude gain. (EQ-Gain 2 values)

The Repeater’s settings must be co-optimized together with Tx and Rx settings to maximize the overall link performance.

Tx + Repeater sweep parameters \(6 \times 6 \times 2 \times 10 = 720\) cases!
System designers need a way to gain confidence in their chosen topology and its viability. *System-level simulations are one way to achieve this goal.*

The proposed methodology for simulating a *Tx+Repeater+Rx system* of PCIe Gen-4:

1. Determine if a Repeater is required.
2. Define a simulation space.
3. Define evaluation criteria.
4. Execute the simulation matrix and analyze the results.

**Goal:** Reach a conclusion regarding the optimum configuration of the system in an efficient and timely manner.

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**PCIe Gen-4 topology considered for this presentation:**
Step 1: Determine if a Repeater is Necessary

Two ways to determine if a Repeater is necessary:

1. Compare end-to-end channel loss to PCIe channel requirements
2. End-to-end channel simulation in ADS

<table>
<thead>
<tr>
<th>Channel analysis method</th>
<th>Value</th>
<th>PCIe Requirement</th>
<th>Conclusion</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. End-to-end channel insertion loss</td>
<td>38.8 dB at 8 GHz</td>
<td>≤ 20.5 dB at 8 GHz</td>
<td>Repeater is required</td>
</tr>
<tr>
<td>2. Channel simulation with behavioral Tx, Rx, and package</td>
<td>EH = 8.7 mV</td>
<td>EH ≥ 15 mV</td>
<td>Repeaters is required</td>
</tr>
<tr>
<td></td>
<td>EW = 0.395 UI</td>
<td>EW ≥ 0.3 UI</td>
<td></td>
</tr>
</tbody>
</table>

Introduction | Repeater Required? | Define Sim Space | Define Pass Criteria | Execute & Analyze | Conclusion
Step 2: Define a Simulation Space

The system-level simulation task is broken down into two sequential phases:

1. **Initial link performance analysis.** Analyze the Tx/Repeater/Rx settings on link performance.
2. **Sensitivity analysis.** Quantify the sensitivity of Repeater placement.

<table>
<thead>
<tr>
<th>Simulation Phase</th>
<th>RC Tx Parameters</th>
<th>Repeater Parameters</th>
<th>EP Rx Parameters</th>
<th>Channel Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial link performance analysis</td>
<td>Presets: 0, 1, ..., 9 VOD: 1000 mVppd</td>
<td>Boost: Sweep six values Wide-band gain: -1 dB</td>
<td>Rx parameters automatically adaptive</td>
<td>Channel topologies considered: 1. Repeater placed on Main Board 2. Total 21 inches channel</td>
</tr>
<tr>
<td>Sensitivity analysis</td>
<td>Presets: 0, 1, ..., 9 VOD: 1000 mVppd</td>
<td>Boost: Optimum setting from Phase 1 Wide-band gain: ±4 dB</td>
<td>Rx parameters automatically adaptive</td>
<td>Focus on optimum topology. 1. Place Repeater on Riser card 2. Vary Repeater placement by ±2 inch to assess sensitivity to placement.</td>
</tr>
</tbody>
</table>
Step 3: Define Pass/Fail Criteria

The methodology proposed here uses two criteria to establish link performance:

1. A link must meet receiver’s EH and EW requirements
2. A link must meet criterion 1 for all Tx Preset settings

Criterion 1 establishes that there is a viable set of settings which will result in the desired BER.

Criterion 2 ensures that the link has adequate margin and is not overly-sensitive to the Tx Preset setting.
Step 4: Execute and Analyze

- **IBIS-AMI** models are used for each active component:
  - Tx and Rx Models from Xilinx
  - Linear Repeater Models from Texas Instruments.
- **Keysight ADS Channel Simulation** is used to execute the IBIS-AMI simulations
- **ADS Batch Mode Simulation** is used to sweep all Tx/Repeater configurations automatically

<table>
<thead>
<tr>
<th>Simulation Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>16.0 GT/s</td>
</tr>
<tr>
<td>Data Pattern</td>
<td>PRBS31</td>
</tr>
<tr>
<td>Total number of bits</td>
<td>1 Million</td>
</tr>
</tbody>
</table>

Simulation Schematic used for this Analysis
Step 4: Initial Link Performance Analysis

### Rx Post-Equalization EW vs Repeater Boost (dB)

<table>
<thead>
<tr>
<th>Repeater Boost (dB)</th>
<th>Average EW (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.0</td>
<td>0.340</td>
</tr>
<tr>
<td>16.7</td>
<td>0.468</td>
</tr>
<tr>
<td>17.0</td>
<td>0.468</td>
</tr>
<tr>
<td>18.7</td>
<td>0.340</td>
</tr>
<tr>
<td>19.0</td>
<td>0.468</td>
</tr>
<tr>
<td>19.5</td>
<td>0.468</td>
</tr>
<tr>
<td>20.0</td>
<td>0.468</td>
</tr>
<tr>
<td>20.5</td>
<td>0.468</td>
</tr>
<tr>
<td>21.4</td>
<td>0.468</td>
</tr>
</tbody>
</table>

### Rx Post-Equalization EH vs Repeater Boost (dB)

<table>
<thead>
<tr>
<th>Repeater Boost (dB)</th>
<th>Average EH (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.0</td>
<td>133</td>
</tr>
<tr>
<td>16.7</td>
<td>133</td>
</tr>
<tr>
<td>17.0</td>
<td>133</td>
</tr>
<tr>
<td>18.7</td>
<td>133</td>
</tr>
<tr>
<td>19.0</td>
<td>133</td>
</tr>
<tr>
<td>19.5</td>
<td>133</td>
</tr>
<tr>
<td>20.0</td>
<td>133</td>
</tr>
<tr>
<td>20.5</td>
<td>133</td>
</tr>
<tr>
<td>21.4</td>
<td>133</td>
</tr>
</tbody>
</table>

**Legend:**
- Red: Fail
- Orange: Marginal
- Yellow: Pass
- Green: Pass
Step 4: Initial Link Performance Analysis

Post-equalized eye diagram for all Tx Preset settings. The optimum Repeater boost (20.5 dB) is used for these cases. Tx Preset 8 yields the largest post-equalized eye opening.
Step 4: Sensitivity Analysis

- A similar analysis is conducted for the alternate placement: Repeater on the Riser Card.
- In this configuration, the pre-channel loss is ~25 dB at 8 GHz; post-channel loss is ~14 GHz at 8 GHz.
- This placement shows consistently reduced performance compared to Main Board placement of the Repeater.

Repeater on Main Board, Preset 8, Boost=20.5 dB

Repeater on Riser Card, Preset 9, Boost=20.5 dB
Step 4: Sensitivity to Placement

- Optimum Repeater placement is on the Main Board.
- Analyze the sensitivity of link performance due to the specific placement of the Repeater.
- Simulations are run with a ±2 inch variation in Repeater placement.

Introduction
Repeater Required?
Define Sim Space
Define Pass Criteria
Execute & Analyze
Conclusion

Optimum Repeater placement is on the Main Board. Analyze the sensitivity of link performance due to the specific placement of the Repeater. Simulations are run with a ±2 inch variation in Repeater placement.
**Question:** Does the optimum Repeater setting change with a relatively minor shift in the specific placement?

**Answer:** No. Both plots peak at the same setting.
A simple four-step process for evaluating **Root Complex + Repeater + End Point** PCIe Links:

1. **Determine if a Repeater is necessary**
   - Does end-to-end channel exceed PCIe Base Specification?
   - Does Channel Sim EH/EW meet the Spec?

2. **Setup simulation sweep space**
   - Include all Tx Presets
   - Choose Repeater boost around pre-channel loss

3. **Define a pass/fail criteria**
   - Final Receiver’s post-equalized eye height (EH) and eye width (EW)
   - Achieving Rx EH/EW requirements across *all Tx Presets*

4. **Execute simulation matrix**
   - Break execution into two phases to minimize overall simulation time.
   - Use Batch Mode Simulation to reduce the simulation cost

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**Summary**

**Introduction**

**Repeater Required?**

**Define Sim Space**

**Define Pass Criteria**

**Execute & Analyze**

**Conclusion**
Simulation vs. Measurement
Analog Bits PCIe® 4.0 SerDes Test Chip

Data rate: 16 GT/s
High-Speed SerDes grade socket (for ABITC16P4 test chip)
Simulation vs. Measurement
ADS Test Bench

- Tx-AMI model
- S-parameter model of channel
- AMI model representation of the scope (Receiver)
- Eye observation at the Rx output
Simulation vs. Measurement
EW & EH Comparison

Eye Width [ps]

Eye Height [mV]
Simulation vs. Measurement

P0-P4 Eye Diagram
Simulation vs. Measurement
P5-P9 Eye Diagram

Measurement

Simulation
Reference

End-to-End System-Level Simulations with Repeaters for PCIe Gen4: A How-To Guide

Casey Morrison, Texas Instruments
Cindy Cui, Keysight

Yongyao Li (Huawei), Casey Morrison (Texas Instruments), Fangyi Rao (Keysight), Cindy Cui (Keysight), Geoff Zhang (Xilinx)


PCI Express: Techniques for 16 GT/s Deployment

March 23, 2017

Want More Resources?

ADS Bundle Used for PCI-Express 4.0 Analysis:

• **W2223BP ADS Core, TransConv, Channel, CILD, Layout, SIPro, PIPro Bundle**

Signal Integrity & Power Integrity Resources

www.keysight.com/find/eosof-ads-sipi-resources

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Thank you!

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QUESTIONS?