PCI Express®

- PCI Express: Where is it used in computers?
- DUTs and J-BERT match
- Testing PCI Express
  - PCIe 2 theory
  - realization of RX-tests w/ J-BERT-A
- PCIe 3, another outlook

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Processor Architecture Block Diagram for PCIe

- Central Processing Unit
- Northbridge
  - RAM (memory)
  - AGP (video card)
  - PCI express
- Southbridge
  - PCI Bus
  - Real Time Clock
  - APM (power management)
  - USB
  - Other Devices
  - PCI express
Processor Architecture Block Diagram for PCIe
Processor Architecture Block Diagram for PCIe
Testing PCI Express Electrical Layer
PCI Express Electrical Layer Test

Physical Layer Measurements

- TX waveform characterization and jitter decomposition
- Jitter transfer PLL or CDR frequency response measurements
- RX sensitivity and jitter tolerance test

Infiniium Scope

J-BERT
## DUTs and Tests

<table>
<thead>
<tr>
<th>DUT</th>
<th>mandatory test / recommended tests</th>
<th>relevant spec</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/Os of test chips</td>
<td>TX, RX, jitter transfer</td>
<td>PCIe base spec</td>
</tr>
<tr>
<td>I/Os of final ASICs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Add in cards (graphic)</td>
<td>TX, jitter transfer</td>
<td>CEM card spec</td>
</tr>
<tr>
<td>Motherboards</td>
<td>RX sensitivity w/ stressed eye</td>
<td></td>
</tr>
</tbody>
</table>
### Which Tests, Addressed When and How

<table>
<thead>
<tr>
<th>Test</th>
<th>Now</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX sensitivity and jitter tolerance</td>
<td>J-BERT A + 81150A &amp; 15431A for correct RJ spectrum trace #2 for ISI / DJ</td>
</tr>
<tr>
<td>TX waveform tests</td>
<td>Scope</td>
</tr>
<tr>
<td>TX jitter transfer</td>
<td>Scope</td>
</tr>
</tbody>
</table>
The Theory Behind the Specs
Common Clock Topology

\[ H(s) = \frac{2s \zeta_1 \omega_n + \omega_n^2}{s^2 + 2s \zeta_1 \omega_n + \omega_n^2} e^{-sT_1} \]

5 MHz, 1 dB or 8 MHz, 3 dB

\[ \frac{2s \zeta_2 \omega_n + \omega_n^2}{s^2 + 2s \zeta_2 \omega_n + \omega_n^2} \]

16 MHz, 3 dB

\[ Y(s) = X_1(s) * H(s) \]

PLL difference function

- Tx and Rx paths track LF jitter in accordance with PLL difference function.
- PLL difference function removes jitter in below 5 MHz and above 16 MHz.
- SSC residual jitter reduced to 33 KHz, 75 ps triangular waveform.
# 5.0 GT/s Rx Tolerancing Parameters (common clock architecture)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td>199.94</td>
<td>200.06</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{RX_HF_RMS}$</td>
<td>&gt; 1.5 MHz $R_j$</td>
<td></td>
<td>3.4$^1$</td>
<td>ps RMS</td>
</tr>
<tr>
<td>$T_{RX_HF_DJ_DD}$</td>
<td>&gt; 1.5 MHz $D_j$ (including channel effects)</td>
<td>88$^2,3$</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$T_{RX_SSC_RES}$</td>
<td>0-1.5 MHz $D_j$ (SSC residual)</td>
<td>75$^4$</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$T_{RX_LF_RMS}$</td>
<td>0-1.5 MHz $R_j$</td>
<td>4.2</td>
<td></td>
<td>ps RMS</td>
</tr>
<tr>
<td>$T_{RX_MIN_PULSE}$</td>
<td>Minimum width pulse at Rx</td>
<td>120</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$V_{RX_MAX_MIN_RATIO}$</td>
<td>min/max pulse voltage ratio on consecutive UI</td>
<td>5</td>
<td></td>
<td>--</td>
</tr>
<tr>
<td>$V_{RX_EYE}$</td>
<td>Receive eye voltage aperture</td>
<td>120</td>
<td>1200</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{RX_CM_AC_PP}$</td>
<td>Common mode noise</td>
<td>300</td>
<td></td>
<td>mVPP</td>
</tr>
</tbody>
</table>

1. Jitter BW: 1.5 – 100 MHz, spectrally flat, consisting of contributions from Refolk and Tx
2. Includes sinusoidal component plus channel effects. Sinusoid swept continuously from 1.5 – 100 MHz or over same range in 10$^{th}$ octave steps
3. Two different tests must be performed: maximum channel with minimum sinusoidal $D_j$ and zero channel with max sinusoidal $D_j$. In both cases $D_j$ total = 88 ps pp.
4. SSC residual consists of 33 KHz triangular wave with 75 ps PP magnitude
5. 0 – 1.5 MHz, spectrally flat, consisting of contributions from Refolk and Tx
Data Driven Topology

\[ H_1(s) = \left[ \frac{2s \zeta_1 \omega_n + \omega_n^2}{s^2 + 2s \zeta_1 \omega_n + \omega_n^2} \right] \]

\[ Y(s) = X_1(s) * H_1(s) \]

PLL difference function

- The full 20 ns of SSC jitter must be tracked by the CDR
- Receiver must track additional <1.5 MHz Rj and Rj in the 1.5-8 MHz range that would otherwise be removed by the PLL difference function in the CC case.
- Rx must also track LF Refclk jitter from 1.5 MHz down to 10 KHz
## 5.0 GT/s Rx Tolerancing Parameters (data driving architecture)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td>199.94</td>
<td>200.06</td>
<td>ps</td>
</tr>
<tr>
<td>(T_{RX_HF_RMS})</td>
<td>&gt; 1.5 MHz Rj</td>
<td></td>
<td>4.2¹</td>
<td>ps RMS</td>
</tr>
<tr>
<td>(T_{RX_HF_DJ_DD})</td>
<td>Max Dj impinging on Rx under tolerancing</td>
<td></td>
<td>88²,³</td>
<td>ps</td>
</tr>
<tr>
<td>(T_{RX_LF_SSC_FULL})</td>
<td>0-1.5 MHz Dj (Full SSC)</td>
<td></td>
<td>20⁴</td>
<td>ns</td>
</tr>
<tr>
<td>(T_{RX_LF_RMS})</td>
<td>10 Khz – 1.5 MHz RMS jitter</td>
<td></td>
<td>8</td>
<td>ps RMS</td>
</tr>
<tr>
<td>(T_{RX_MIN_PULSE})</td>
<td>Minimum width pulse at Rx</td>
<td>120</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>(V_{RX_MAX_MIN_RATIO})</td>
<td>min/max pulse voltage ratio on consecutive UI</td>
<td></td>
<td>5</td>
<td>--</td>
</tr>
<tr>
<td>(V_{RX_EYE})</td>
<td>Receive eye voltage aperture</td>
<td>100</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>(V_{RX_CM_AC_PP})</td>
<td>Common mode noise</td>
<td>300</td>
<td></td>
<td>mVPP</td>
</tr>
</tbody>
</table>

1. Spectrally flat from 0 – 1.5 MHz. Includes 3.9 ps from Refclk and 1.4 ps from Tx
2. Two different tests must be performed: maximum channel with minimum sinusoidal Dj and zero channel with max sinusoidal Dj
3. Two different tests must be performed: maximum channel with minimum sinusoidal Dj and zero channel with max sinusoidal Dj
4. Full SSC must be tracked. Includes sinusoidal component plus channel effects.
5. Over 10 Khz – 1.5 MHz BW with -20 dB/decade to account for 1/f noise slope
RX Jitter Tolerance Specs Based Upon Channel Behavior: DJ (ISI+PJ)

- channel is specified in terms of pulse amplitude compression\(^1\), not directly in terms of ISI or DJ
  \(^1\) there is a return loss spec of <20dB as well

- a total of DJ=88ps is specified
  - combined from ISI from channel (maybe less than 88ps) plus
  - swept PJ (1.5MHz...100MHz)

Pattern consists of 0.9 UI low followed by 5.1 UI high and represents w/c pulse DCD distortion

\[ V_{SWING} \] min/max ratio is ~ 5.0/1

Transient behavior
Trace # 2 OK for PCI Express 2.0

pattern:
1111 1011 1111 1111 0000 0100 0000 0000
normal only, trig / 16

levels of lone 1 (0) are about 20% of those of long duration.

Levels of long duration are equivalent to those of w/o channel
ISI “compliant channel” (trace # 2)

PRBS $2^{15}-1$

through trace # 2

⇒ 84ps ISI

⇒ add ~4ps PJ, 100MHz

⇒ DJ = 88ps
two different clocking architectures:

common ref-clk
- RX sampling on (multiplied) ref clk
- RX w/DLL only
- SSC off: no phase error induced
- SSC on:
  - small error (femto seconds) due to path delay difference (!) but
  - significant residual phase error due to potentially different transfer functions (BW and peaking) of TX and RX clock multiplying PLLs

data clocked (embedded clock)
- RX w/ PLL-CDR (using ref clock only until locked)
- SSC on or off
  - common for TX and RX
  - both TX’s use same ref clk

<table>
<thead>
<tr>
<th></th>
<th>Com Ref-clk</th>
<th></th>
<th>Data Clocked</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>rms</td>
<td>pp</td>
<td></td>
</tr>
<tr>
<td>SSC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RJ (?)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HF</td>
<td>3.4</td>
<td>47.6</td>
<td>RJ (?)</td>
</tr>
<tr>
<td>LF</td>
<td>4.2</td>
<td>58.8</td>
<td>LF</td>
</tr>
<tr>
<td>RJ, sqrt sum</td>
<td>5.4</td>
<td>75.7</td>
<td>RJ, sqrt sum</td>
</tr>
<tr>
<td>DJ</td>
<td></td>
<td></td>
<td>DJ</td>
</tr>
<tr>
<td></td>
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<td></td>
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<td></td>
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<tr>
<td>total</td>
<td>sqrt</td>
<td>150.7 - 238.7</td>
<td>total</td>
</tr>
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<td></td>
<td></td>
<td>sqrt</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>total</td>
<td></td>
<td>126.5 - 214.5</td>
<td>total</td>
</tr>
</tbody>
</table>

“UHF”
two different clocking architectures:

common ref clk
• RX sampling on (multiplied) ref clk
• RX w/DLL only
• SSC off: no phase error induced
• SSC on:
  – small error (femtoseconds) due to path delay difference (!) but
  – significant residual phase error due to potentially different transfer functions (BW and peaking) of TX and RX clock multiplying PLLs

data clocked (embedded clock)
• RX w/ PLL-CDR (using ref clock only until locked)
• SSC on or off
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<table>
<thead>
<tr>
<th>SSF</th>
<th>rms</th>
<th>pp</th>
<th></th>
<th>SSF</th>
<th>rms</th>
<th>pp</th>
</tr>
</thead>
<tbody>
<tr>
<td>RMS</td>
<td>3.4</td>
<td>47.6</td>
<td>HF</td>
<td>1.4</td>
<td>58.8</td>
<td></td>
</tr>
<tr>
<td>LF</td>
<td>4.2</td>
<td>58.8</td>
<td>RJ,</td>
<td>3.0</td>
<td>112</td>
<td></td>
</tr>
<tr>
<td>sqrt sum</td>
<td>5.4</td>
<td>75.7</td>
<td>RJ,sqrt sum</td>
<td>9.0</td>
<td>126.5</td>
<td></td>
</tr>
<tr>
<td>HF</td>
<td>30</td>
<td>DJ</td>
<td></td>
<td>“UHF”</td>
<td>27</td>
<td>“UHF”</td>
</tr>
<tr>
<td>“UHF”</td>
<td>27</td>
<td>total</td>
<td>132.7</td>
<td>total</td>
<td>sqrt</td>
<td>126.5</td>
</tr>
</tbody>
</table>
Three Steps To RX-jitter Tolerance Testing

1. Prepare DUT-RX for test
   – exit mission mode
   – enter test mode, set into loopback-mode

2. Stimulate DUT with all required signals and applicable properties
   – free running or synchronized to DUT
   – signal levels
   – delay between signals
   – jitter, absolute and between signals

3. Determine correctness of RX’s conversion
   – synch on looped back data
   – analyze digital content: de-code, unpack, strip idles, …
   – compare and count errors: BER, FER,…
J-BERT, with 81150A for Spectral RJ and Residual SSC

- RJ generated through appropriately filtered noise from and external modulation capability of J-BERT residual SSC generated through 2nd Pulsar channel
- DJ (ISI+PJ) generated by J-BERT: trace #2 and internal source
- de-box used if de-emphasized signals are required
- patterns for DUT-RX programming available
Outlook PCIe-3
PCIe3, rev 0.5

- Symbol rate 8Gbs (includes a coding of 130/128?)
- Some as PCIe2, **two architectures**, common ref clk and data clocked
  - **common ref clk**: BERT sources **clean clock & residual SSC on data**
  - **data clocked**: no clock supplied but **full SSC on data**
- RX measured **w/ & w/o ISI-channel** (calibration channel) - specs tbd
- **RJ** is always **spectrally flat** between 10MHz and 1GHz
- **PJ** is **two-tone sinusoidal** (two frequencies **simultaneously**)!
  - 1st tone 70ps if 10KHz-1MHz, or 70..7ps if 1MHz-10MHz (tbd)
  - 2nd tone 7ps, 10MHz-1GHz (tbd)
- Noise injection
  - common mode: single sinusoidal; Vpp and frq tbd
  - differential mode: spectrally flat white noise BW (>1GHz), Vpp tbd
- DCD 4ps
- necessity of de-emph tbd in rev .07