Keysight D9040PCIC PCI-Express Compliance Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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CAUTION

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WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

In This Book

This book is your guide to programming the Keysight Technologies D9040PCIC PCI-Express Compliance Application.

- Chapter 1, “Introduction to Programming,” starting on page 7 describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 29, and Chapter 4, “Instruments,” starting on page 65 provide information specific to programming the D9040PCIC PCI-Express Compliance Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, and 4 for changes.

Contents

1 Introduction to Programming

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9040PCIC PCI-Express Compliance Application uses Remote Interface Revision 6.00. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9040PCIC PCI-Express Compliance Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Delta Time	ClockRecoveryDeltaTime	Fixed, Variable	Select the clock recovery delta time from compliance pattern of 64 zeroes and 64 ones
Configure	De-Emphasis Removal	EnableDeEmpRemoval	1.0, 0.0	Enable or Disable De-Emphasis Removal feature for the jitter and eye width measurement of the transmitter test.
Configure	Differential clock waveform file name	DiffClkWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the differential clock waveform file.
Configure	Differential waveform file name	DiffWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the differential data waveform file.
Configure	Display Preset Signal	DisplayPresetSignal	1.0, 0.0	When Display Preset Signal is Yes, the preset signal will display in the report.
Configure	Execution Timeout(s)	SigTestTimeOut	(Accepts user-defined text), 200.0	Estimate of time needed for sigtest to process any template. The timeout will be used to detect if the sigtest is crashing or not.
Configure	Gen 2 Ref Clock Transfer Function (Common Clock)	Gen2CommonRefClkTF	H1: 5MHz, 1.0dB peaking | H2: 16MHz, 3.0dB peaking, H1: 8MHz, 3.0dB peaking | H2: 16MHz, 3.0dB peaking	Select the transfer function for Gen 2 reference clock signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Gen 3 Ref Clock Transfer Function (Common Clock)	Gen3CommonRefClkTF	H1: 2MHz, 0.01dB peaking | H2: 2MHz, 0.01dB peaking, H1: 2MHz, 0.01dB peaking | H2: 2MHz, 1.0dB peaking, H1: 2MHz, 0.01dB peaking | H2: 5MHz, 0.01dB peaking, H1: 2MHz, 0.01dB peaking | H2: 5MHz, 1.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 2MHz, 0.01dB peaking, H1: 2MHz, 2.0dB peaking | H2: 2MHz, 1.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 5MHz, 0.01dB peaking, H1: 2MHz, 2.0dB peaking | H2: 5MHz, 1.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 2MHz, 0.01dB peaking, H1: 4MHz, 0.01dB peaking | H2: 2MHz, 1.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 5MHz, 0.01dB peaking, H1: 4MHz, 0.01dB peaking | H2: 5MHz, 1.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 2MHz, 0.01dB peaking, H1: 4MHz, 2.0dB peaking | H2: 2MHz, 1.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 5MHz, 0.01dB peaking, H1: 4MHz, 2.0dB peaking | H2: 5MHz, 1.0dB peaking, All Transfer Function	Select the transfer function for Gen 3 reference clock signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Gen 3 Ref Clock Transfer Function (Data Clock)	Gen3DataRefClkTF	H1: 2MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 1.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 2.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 2MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 2MHz, 1.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 2MHz, 2.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 4MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 4MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 4MHz, 2.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 4MHz, 2.0dB peaking | H2: 10MHz, 2.0dB peaking, H1: 5MHz, 0.01dB peaking | H2: 10MHz, 0.5dB peaking, H1: 5MHz, 0.01dB peaking | H2: 10MHz, 2.0dB peaking, H1: 5MHz, 1.0dB peaking | H2: 10MHz, 0.5dB peaking, H1: 5MHz, 1.0dB peaking | H2: 10MHz, 2.0dB peaking, All Transfer Function	Select the transfer function for Gen 3 reference clock signal.
Configure	Noise Reduction BW, GHz	EBW1	0.0, 6.0E+9, 5.5E+9, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Noise Reduction BW, GHz	EBW2	0.0, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Noise Reduction BW, GHz	EBW3	0.0, 13.0E+9, 12.5E+9, 12.0E+9, 10.0E+9, 8.0E+9, 7.0E+9, 6.5E+9, 6.0E+9, 5.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Noise Reduction BW, GHz	EBW4	0.0, 50.0E+9, 25.0E+9, 20.0E+9, 16.0E+9, 13.0E+9, 12.0E+9, 10.0E+9, 8.0E+9, 5.0E+9	(Limited availability*) Specify the noise reduction bandwidth to use for all tests.
Configure	Number of Clock UI	NumClockUI	(Accepts user-defined text), 1000000, 500000, 100000, 50000	This is the number of clock unit intervals processed when calculating clock jitter. For compliance testing, this measurement requires 1,000,000 UI to guarantee the proper bit error rate (10E-6 BER) as specified in the PCI Express Base Specification Rev. 1.1. The allowed values for this control are between 1000 and 3,000,000 UIs.
Configure	Number of UI	NumUIGen1Test	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of UI	NumUIGen2Test	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1E+6 (1,000,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUIGen3Test	(Accepts user-defined text), 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1.6E+6 (1,600,000) UI as specified in the PCI Express CEM Specification Rev. 2.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Number of UI	NumUIGen4Test	(Accepts user-defined text), 2.0E+6, 1.6E+6, 1.0E+6, 500.0E+3, 250.0E+3, 100.0E+3, 50.0E+3	This is the minimum number of unit intervals used in the Eye-Width, TJ at BER-12, Maximum DJ , RMS RJ and Template tests. These measurements should be made using the compliance pattern at a sample size of at least 1.6E+6 (1,600,000) UI as specified in the PCI Express CEM Specification Rev. 4.0. Specifying a greater number of UI will increase the test time and accuracy of the tests.
Configure	Output Filename	RefClkOutputCSVFilename	(Accepts user-defined text), None, Auto	Output Filename.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	ProbeHead Check	EnableProbeHeadCheck	1.0, 0.0	When ProbeHead check is enabled, the input signal's probe head configuration is verified. This is only done when performing DualPort Testing in Gen2 System Board Test.
Configure	RJ Bandwidth	RJBW	NARR, WIDE	Select the RJ bandwidth.
Configure	RefClk Noise Reduction BW, GHz	ClockEBW	0.0, 5.0E+9, 4.5E+9, 4.0E+9, 3.5E+9, 3.0E+9, 2.5E+9, 2.0E+9, 1.5E+9, 1.0E+9	Select the bandwidth to acquire reference clock signal.
Configure	Rise/Fall Time Measurement Count	RiseFallCount	10.0E+3, 5.0E+3, 2.0E+3, 1.0E+3, 500.0E+0, 200.0E+0	Select the minimum measurement count for each rise time and fall time for the Rise/Fal time measurement with variable threshold.
Configure	S-Parameter for Add-in Card	AddInSParamFilePath	(Accepts user-defined text), AicTx_Test_Embed01_SigTest.s4p, AICTx_Test_Embed_SigTest.s4p	Stores the s-parameter file path for Add-in card tests.
Configure	S-Parameter for System Board	SystemSParamFilePath	(Accepts user-defined text), SystemTx_Test_Embed01_SigTest.s4p	Stores the s-parameter file path for System board tests.
Configure	S-Parameter for U.2 Add-in Card	U2AddInSParamFilePath	(Accepts user-defined text), U.2_DeviceTx_SigTest_Embed05.s4p, U.2_DeviceTx_SigTest_Embed05_20G.s4p, U.2_DeviceTx_SigTest_Embed05_25G.s4p, U.2_DeviceTx_SigTest_Embed05_40G.s4p, U.2_DeviceTx_SigTest_Embed05_50G.s4p	Stores the s-parameter file path for U.2 Add-in card tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	S-Parameter for U.2 System Board	U2SystemSParamFilePath	(Accepts user-defined text), U.2_HostTx_SigTest_Embed04.s4p, U.2_HostTx_SigTest_Embed04_20G.s4p, U.2_HostTx_SigTest_Embed04_25G.s4p, U.2_HostTx_SigTest_Embed04_40G.s4p, U.2_HostTx_SigTest_Embed04_50G.s4p	Stores the s-parameter file path for U.2 System board tests.
Configure	Sample Rate, GSa/s	SRate	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 5.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 1.0a, PCIE 1.1 , PCIe 2.0 (2.5 GT/s) and Express Card 1.0 tests.
Configure	Sample Rate, GSa/s	SRate_Gen2	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_Gen3	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 2.0 (5.0 GT/s) tests or PCIE 3.0 (8.0 GT/s) tests.
Configure	Sample Rate, GSa/s	SRate_Gen4	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	(Limited availability*) Specify the sample rate to use for all PCIE 4.0 (16.0 GT/s) tests.
Configure	Sample rate, GSa/s	ClockSR	80.0E+9, 40.0E+9, 20.0E+9, 10.0E+9, 5.0E+9, 128.0E+9, 64.0E+9, 32.0E+9, 16.0E+9, 8.0E+9	Select the sample rate to acquire reference clock signal.
Configure	Selected SigTest Version	BS_SigTestVer16GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 16.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Selected SigTest Version	BS_SigTestVer2_5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 2.5 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	BS_SigTestVer5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 5.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	BS_SigTestVer8GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 8.0 GT/s Base Transmitter Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	EP_SigTestVer16GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 16.0 GT/s End Point Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	EP_SigTestVer2_5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 2.5 GT/s End Point Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	EP_SigTestVer5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 5.0 GT/s End Point Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	EP_SigTestVer8GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 8.0 GT/s End Point Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	RC_SigTestVer16GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 16.0 GT/s Root Complex Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	RC_SigTestVer2_5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 2.5 GT/s Root Complex Tests. Setting is defined according to Data Rate.
Configure	Selected SigTest Version	RC_SigTestVer5GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 5.0 GT/s Root Complex Tests. Setting is defined according to Data Rate.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Selected SigTest Version	RC_SigTestVer8GT	3.2.0, 3.2.0.1, 3.2.0.3, 4.0.37, 4.0.39, 4.0.46	Specify the version of the SigTest for 8.0 GT/s Root Complex Tests. Setting is defined according to Data Rate.
Configure	Show Jitter Filter Plot	ShowJitterFilterPlot	0, 2, 3, 4, 5	Select the clock jitter plot to display. Generating plots will increase test runtime.
Configure	Signal Check	EnableSignalCheck	1.0, 0.0	When signal check is enabled, the input signal is pre-tested and verified to be within a reasonable range of timing and voltage limits. This can be useful for detecting problems like cabling errors before a test is run.
Configure	Silent Mode	SigTestSilentMode	0.0, 1.0	Allow SigTest.exe to be executed in silent mode or with GUI. Put 1 for Silent Mode or 0 otherwise. SigTest 4.0.19 onwards only supporting silent mode.
Configure	Sine(x)/x Interpolation	SineXInterpolation	ON, OFF, INT1, INT2, INT4, INT8	Sine(x)/x Interpolation.
Configure	Single ended negative clock waveform file name	ClkDNWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended negative clock waveform file.
Configure	Single ended negative waveform file name	DNWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended negative data waveform file.
Configure	Single ended positive clock waveform file name	ClkDPWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended positive clock waveform file.
Configure	Single ended positive waveform file name	DPWfmFile	(Accepts user-defined text), None	This variable use to store the directory of the single ended positive data waveform file.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Stitch Method	StitchMethod	Absolute, Dynamic	Select the method to stitch the waveform for reference clock phase jitter test. Absolute method stitches the waveform based on absolute data. Dynamic method aligns waveform data to have common offset before stitching. This option only applies when Spread Sprectrum Clocking is enabled.
Configure	Toggle Mode	optToggleMode	CalOut (100 Mhz), 81150A	This variable for toggle mode options
Configure	Transition Time Threshold	TransitionTimeThreshold	Fixed, Variable	Select the threshold method used to measure transition time.Fixed method applied the same threshold for all edges. Variable method applied threshold based on the previous and the next unit interval.
Configure	Trigger Pulse Width, s	TrigPulseWidth	8.0E-9, 7.0E-9, 6.0E-9, 5.0E-9	(Limited availability*) Specify the width in second for the Pulse Width Trigger setup.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	DUT Toggle Mode	PFAIPOrSICL	IP, SICL	DUT Toggle Mode
Set Up	DUT Toggle Mode	PFAIPOrSICL	IP, SICL	DUT Toggle Mode
Set Up	DUT Toggle Mode	ToggleModeOpt	81150A/81160A, AuxOut (100Mhz), AuxOut (HF Osc)	DUT Toggle Mode
Set Up	DUT Toggle Mode	ToggleModeOpt	81150A/81160A, AuxOut (100Mhz), AuxOut (HF Osc)	DUT Toggle Mode

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DevicePCIErev	DevicePCIErev	PCIE 1.0a, PCIE 1.1, PCIE 2.0, PCIE 3.0, PCIE 4.0	Select the PCI Express device specification to use.
Set Up	DevicePCIErev	DevicePCIErev	PCIE 1.0a, PCIE 1.1, PCIE 2.0, PCIE 3.0, PCIE 4.0	Select the PCI Express device specification to use.
Set Up	Enable Collective Data Acquisition	saveWfmFirst	0.0, 1.0	Enable Collective Data Acquisition
Set Up	Enable DUT Automation	Dut_Automation	0.0, 1.0	Enable DUT Automation
Set Up	Enable DUT Automation	Dut_Automation	0.0, 1.0	Enable DUT Automation
Set Up	Enable Workshop Compliance Mode	PlugFest_Mode	0.0, 1.0	Enable Workshop Compliance Mode
Set Up	Flag for Device Definition Done status	DeviceDefinitionDone	0.0, 1.0	Flag for Device Definition Done status
Set Up	OfflineEnable	OfflineEnable	0.0, 1.0	Enable the application use saved waveform for testing.
Set Up	OfflineEnable	OfflineEnable	0.0, 1.0	Enable the application use saved waveform for testing.
Set Up	SavedWfmSignalType	SavedWfmSignalType	Single Ended, Differential	Select the Signal Type for saved waveform.
Set Up	Select 16.0GT/s related tests.	TestPoint_DataRate_16_0	0.0, 1.0	Select 16.0GT/s related tests.
Set Up	Select 16.0GT/s related tests.	TestPoint_DataRate_16_0	0.0, 1.0	Select 16.0GT/s related tests.
Set Up	Select 2.5GT/s related tests.	TestPoint_DataRate_2_5	0.0, 1.0	Select 2.5GT/s related tests.
Set Up	Select 2.5GT/s related tests.	TestPoint_DataRate_2_5	0.0, 1.0	Select 2.5GT/s related tests.
Set Up	Select 5.0GT/s related tests.	TestPoint_DataRate_5_0	0.0, 1.0	Select 5.0GT/s related tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Select 5.0GT/s related tests.	TestPoint_DataRate_5_0	0.0, 1.0	Select 5.0GT/s related tests.
Set Up	Select 5GT/s De-emphasis -3.5dB tests.	DeEmpOpt_3_5dB	0.0, 1.0	Select 5GT/s De-emphasis -3.5dB tests.
Set Up	Select 5GT/s De-emphasis -6.0dB tests.	DeEmpOpt_6_0dB	0.0, 1.0	Select 5GT/s De-emphasis -6.0dB tests.
Set Up	Select 8.0GT/s related tests.	TestPoint_DataRate_8_0	0.0, 1.0	Select 8.0GT/s related tests.
Set Up	Select 8.0GT/s related tests.	TestPoint_DataRate_8_0	0.0, 1.0	Select 8.0GT/s related tests.
Set Up	Select BitiFeye4Probe Lane.	BitiFeye4ProbeLane	Lane 0-7, Lane 8-15	Select BitiFeye4ProbeLane.
Set Up	Select BitiFeye4Probe Lane.	BitiFeye4ProbeLane	Lane 0-7, Lane 8-15	Select BitiFeye4ProbeLane.
Set Up	Select Connection Type.	ConnectionType	Single-Ended, Differential Probe	Select Connection Type.
Set Up	Select Connection Type.	ConnectionType	Single-Ended, Differential Probe	Select Connection Type.
Set Up	Select DeEmphasis level for 5GT/s DUT.	DeEmp5G		Select DeEmphasis level for 5GT/s DUT.
Set Up	Select Power Level.	PowerLevel	Full, Half	Select Power Level.
Set Up	Select Power Level.	PowerLevel	Full, Half	Select Power Level.
Set Up	Select Power Level.	SRISEnabled	None, Enabled	Select Power Level.
Set Up	Select Switch Lane Config.	SwitchLaneConfig	x1, x4, x8, x16	Select Switch Lane Config.
Set Up	Select Switch Lane Config.	SwitchLaneConfig	x1, x4, x8, x16	Select Switch Lane Config.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Select Switch Matrix.	optSwitchMatrix	No Switch, BitifEye BIT 2100, Keysight U3020A S26	Select Switch Matrix.
Set Up	Select Switch Matrix.	optSwitchMatrix	No Switch, BitifEye BIT 2100, Keysight U3020A S26	Select SwitchMatrix.
Set Up	Select connection probe type.	ProbeConnection	2 Probes, 4 Probes	Select connection probe type.
Set Up	Select connection probe type.	ProbeConnection	2 Probes, 4 Probes	Select connection probe type.
Set Up	Select if DUT has SRIS.	SRISEnabled	None, Enabled	Select if DUT has SRIS.
Set Up	Select preset for 16GT/s related tests..	cmbPresetType16G	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, None	Select preset for 16GT/s related tests.
Set Up	Select preset for 16GT/s related tests..	cmbPresetType16G	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, None	Select preset for 16GT/s related tests.
Set Up	Select preset for 8GT/s related tests..	cmbPresetType	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, None	Select preset for 8GT/s related tests.
Set Up	Select preset for 8GT/s related tests..	cmbPresetType	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, None	Select preset for 8GT/s related tests.
Set Up	Select switching modules in BIT2100 Frame.	BIT2100Modules	2xSP4T, 2xSP6T, 2xSP8T	Select switching modules in BIT2100 Frame.
Set Up	Select the Reference Clock Type.	RefClk	CleanClock, SSC	Select the Reference Clock Type.
Set Up	Select the Reference Clock Type.	RefClk	CleanClock, SSC	Select the Reference Clock Type.
Set Up	Specifies ConnectionSetupDone.	ConnectionSetupDone	0.0, 1.0	Specifies ConnectionSetupDone.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Specifies Device ID.	txtDeviceID	(Accepts user-defined text)	Optional Device ID displayed in the test report.
Set Up	Specifies Lane0.	Lane0	0.0, 1.0	Specifies Lane0.
Set Up	Specifies Lane0.	Lane0	0.0, 1.0	Specifies Lane0.
Set Up	Specifies Lane1.	Lane1	0.0, 1.0	Specifies Lane1.
Set Up	Specifies Lane1.	Lane1	0.0, 1.0	Specifies Lane1.
Set Up	Specifies Lane10.	Lane10	0.0, 1.0	Specifies Lane10.
Set Up	Specifies Lane10.	Lane10	0.0, 1.0	Specifies Lane10.
Set Up	Specifies Lane11.	Lane11	0.0, 1.0	Specifies Lane11.
Set Up	Specifies Lane11.	Lane11	0.0, 1.0	Specifies Lane11.
Set Up	Specifies Lane12.	Lane12	0.0, 1.0	Specifies Lane12.
Set Up	Specifies Lane12.	Lane12	0.0, 1.0	Specifies Lane12.
Set Up	Specifies Lane13.	Lane13	0.0, 1.0	Specifies Lane13.
Set Up	Specifies Lane13.	Lane13	0.0, 1.0	Specifies Lane13.
Set Up	Specifies Lane14.	Lane14	0.0, 1.0	Specifies Lane14.
Set Up	Specifies Lane14.	Lane14	0.0, 1.0	Specifies Lane14.
Set Up	Specifies Lane15.	Lane15	0.0, 1.0	Specifies Lane15.
Set Up	Specifies Lane15.	Lane15	0.0, 1.0	Specifies Lane15.
Set Up	Specifies Lane2.	Lane2	0.0, 1.0	Specifies Lane2.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Specifies Lane2.	Lane2	0.0, 1.0	Specifies Lane2.
Set Up	Specifies Lane3.	Lane3	0.0, 1.0	Specifies Lane3.
Set Up	Specifies Lane3.	Lane3	0.0, 1.0	Specifies Lane3.
Set Up	Specifies Lane4.	Lane4	0.0, 1.0	Specifies Lane4.
Set Up	Specifies Lane4.	Lane4	0.0, 1.0	Specifies Lane4.
Set Up	Specifies Lane5.	Lane5	0.0, 1.0	Specifies Lane5.
Set Up	Specifies Lane5.	Lane5	0.0, 1.0	Specifies Lane5.
Set Up	Specifies Lane6.	Lane6	0.0, 1.0	Specifies Lane6.
Set Up	Specifies Lane6.	Lane6	0.0, 1.0	Specifies Lane6.
Set Up	Specifies Lane7.	Lane7	0.0, 1.0	Specifies Lane7.
Set Up	Specifies Lane7.	Lane7	0.0, 1.0	Specifies Lane7.
Set Up	Specifies Lane8.	Lane8	0.0, 1.0	Specifies Lane8.
Set Up	Specifies Lane8.	Lane8	0.0, 1.0	Specifies Lane8.
Set Up	Specifies Lane9.	Lane9	0.0, 1.0	Specifies Lane9.
Set Up	Specifies Lane9.	Lane9	0.0, 1.0	Specifies Lane9.
Set Up	Specifies S-Parameter file to be used for 16GT/s CEM-EndPoint Tests	AddIn16GSParamFilePath	(Accepts user-defined text)	Specifies S-Parameter file to be used for 16GT/s CEM-EndPoint Tests

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Specifies S-Parameter file to be used for 16GT/s CEM-RootComplex Tests	System16GSParamFilePath	(Accepts user-defined text)	Specifies S-Parameter file to be used for 16GT/s CEM-RootComplex Tests
Set Up	Specifies S-Parameter file to be used for 8GT/s CEM-EndPoint Tests	AddInSParamFilePath	(Accepts user-defined text)	Specifies S-Parameter file to be used for 8GT/s CEM-EndPoint Tests
Set Up	Specifies S-Parameter file to be used for 8GT/s CEM-RootComplex Tests	SystemSParamFilePath	(Accepts user-defined text)	Specifies S-Parameter file to be used for 8GT/s CEM-RootComplex Tests
Set Up	Specifies file of differential signal.	DPWfmFile	(Accepts user-defined text)	Specifies file of differential signal.
Set Up	Specifies file of differential signal.	DiffWfmFile	(Accepts user-defined text)	Specifies file of differential signal.
Set Up	Specifies folder to store result from SigTest.	SigTestReportPath	(Accepts user-defined text)	Specifies folder to store result from SigTest.
Set Up	Specifies if user will manually toggle the DUT.	chkbManualDUTToggle	0.0, 1.0	Specifies if user will manually toggle the DUT.
Set Up	Specifies if user will manually toggle the DUT.	chkbManualDUTToggle	0.0, 1.0	Specifies if user will manually toggle the DUT.
Set Up	Specifies the DUT will be reset using a power switch.	chkbResetPowerSwitch	0.0, 1.0	Specifies the DUT will be reset using a power switch.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Specifies the DUT will be reset using a power switch.	chkbResetPowerSwitch	0.0, 1.0	Specifies the DUT will be reset using a power switch.
Set Up	Specifies transfunction file.	InfiniiSimTransferFunction	(Accepts user-defined text)	Specifies transfunction file.
Set Up	Specifies waveform file for D- signal.	DNWfmFile	(Accepts user-defined text)	Specifies waveform file for D- signal.
Set Up	Specifies waveform file for clock+ signal.	ClkDPWfmFile	(Accepts user-defined text)	Specifies waveform file for clock+ signal.
Set Up	Specifies waveform file for clock- signal.	ClkDNWfmFile	(Accepts user-defined text)	Specifies waveform file for clock- signal.
Set Up	Specifies waveform file for differential clock signal.	DiffClkWfmFile	(Accepts user-defined text)	Specifies waveform file for differential clock signal.
Set Up	Speficies IP Address of the DUT toggling source (81150A/81160A).	txtIPAddrPFA	(Accepts user-defined text)	Speficies IP Address of the DUT toggling source (81150A/81160A).
Set Up	Speficies IP Address of the DUT toggling source (81150A/81160A).	txtIPAddrPFA	(Accepts user-defined text)	Speficies IP Address of the DUT toggling source (81150A/81160A).
Set Up	Speficies SICL Address of the DUT toggling source (81150A/81160A).	txtSICLAddrPFA	(Accepts user-defined text)	Speficies SICL Address of the DUT toggling source (81150A/81160A).

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Speficies SICL Address of the DUT toggling source (81150A/81160A).	txtSICLAddrPFA	(Accepts user-defined text)	Speficies SICL Address of the DUT toggling source (81150A/81160A).
Set Up	TestPoint	TestPoint	Base - Transmitter Tests, CEM - EndPoint Tests, CEM - RootComplex Tests, U.2 - EndPoint Tests, U.2 - RootComplex Tests, Base - RefClk Tests	Select the PCIExpress device test point to be tested.
Set Up	TestPoint	TestPoint	Base - Transmitter Tests, CEM - EndPoint Tests, CEM - RootComplex Tests, U.2 - EndPoint Tests, U.2 - RootComplex Tests, Base - RefClk Tests	Select the PCIExpress device test point to be tested. TestPoint
Set Up	TestPoint_Calibration	TestPoint_Calibration	0.0, 1.0	Select to run Preset Tests (Gen 3 and 4 Only).
Set Up	TestPoint_Calibration	TestPoint_Calibration	0.0, 1.0	Select to run Preset Tests (Gen 3 and 4 Only).
Set Up	User Comments	txtUserComment	(Accepts user-defined text)	Optional user comments displayed in the test report.
*Limited availability: Availability of this setting depends upon the oscilloscope model and installed license options.				

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application:

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
EndPoint Tests - SigTest (16.0 GT/s) - Far End	5028	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-12 of section 4.8.4 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. This test considered a physical ISI channel and a package model embedded with InfiniiSim.
EndPoint Tests - SigTest (16.0 GT/s) - Near End	5026	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-12 of section 4.8.4 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB.
EndPoint Tests - SigTest (2.5 GT/s)	5002	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-7 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 1.1, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-8.
EndPoint Tests - SigTest (5.0 GT/s) -3.5dB	5003	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.
EndPoint Tests - SigTest (5.0 GT/s) -6.0dB	5004	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.
EndPoint Tests - SigTest (8.0 GT/s)	5005	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-11 of section 4.8.3 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
EndPoint Tests - SigTest (PCIE 1.0a ,2.5 GT/s)	5001	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification, Rev 1.0a, Section 4.3.3.1, Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications as measured at the package pins into the Compliance Test and Measurement Load, defined in section 4.3.3.2
EndPoint Tests, Eye Width (16.0 GT/s)	4440	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
EndPoint Tests, Eye-Width (2.5 GT/s)	203	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
EndPoint Tests, Eye-Width (2.5 GT/s)	1330	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
EndPoint Tests, Eye-Width (2.5 GT/s)	2330	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
EndPoint Tests, Eye-Width (8.0 GT/s)	3430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
EndPoint Tests, Eye-Width -3.5dB with crosstalk (5.0 GT/s)	2336	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
EndPoint Tests, Eye-Width -3.5dB without crosstalk (5.0 GT/s)	2337	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
EndPoint Tests, Eye-Width -6.0dB with crosstalk (5.0 GT/s)	2338	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
EndPoint Tests, Eye-Width -6.0dB without crosstalk (5.0 GT/s)	2339	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
EndPoint Tests, Maximum Deterministic Jitter -3.5dB with crosstalk (5.0 GT/s)	2392	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Maximum Deterministic Jitter -3.5dB without crosstalk (5.0 GT/s)	2393	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
EndPoint Tests, Maximum Deterministic Jitter -6.0dB with crosstalk (5.0 GT/s)	2394	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Maximum Deterministic Jitter -6.0dB without crosstalk (5.0 GT/s)	2395	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Median to Max Jitter (2.5 GT/s)	202	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
EndPoint Tests, Median to Max Jitter (2.5 GT/s)	1320	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
EndPoint Tests, Median to Max Jitter (2.5 GT/s)	2320	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
EndPoint Tests, Peak Differential Output Voltage (2.5 GT/s)	207	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage (Non Transtion)(8.0 GT/s)	3421	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage (Non-Transition) (16.0 GT/s)	4430	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
EndPoint Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	2350	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	1350	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage (Transition) (16.0 GT/s)	4420	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
EndPoint Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	1340	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	2340	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
EndPoint Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	3420	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s)	2356	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)	2346	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non Transition)(5.0 GT/s)	2358	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s)	2348	This test verifies that the Peak Differential Output Voltage is within the allowed range.
EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s)	2382	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s)	2383	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s)	2384	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s)	2385	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Template Tests (16.0 GT/s)	4410	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
EndPoint Tests, Template Tests (2.5 GT/s)	210	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-6 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 1.0a, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-8.
EndPoint Tests, Template Tests (2.5 GT/s)	1310	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-7 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 1.1, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-8.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
EndPoint Tests, Template Tests (2.5 GT/s)	2310	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-7 of section 4.7.1 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-6.
EndPoint Tests, Template Tests (8.0 GT/s)	3410	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-11 of section 4.8.3 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Template Tests -3.5dB (5.0 GT/s)	2316	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.
EndPoint Tests, Template Tests -6.0dB (5.0 GT/s)	2318	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-10 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in figure 4-7.
EndPoint Tests, Total Jitter at BER-12 -3.5dB with crosstalk (5.0 GT/s)	2396	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Total Jitter at BER-12 -3.5dB without crosstalk (5.0 GT/s)	2397	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Total Jitter at BER-12 -6.0dB with crosstalk (5.0 GT/s)	2398	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Total Jitter at BER-12 -6.0dB without crosstalk (5.0 GT/s)	2399	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-9 of section 4.7.2 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
EndPoint Tests, Uncorrelated Deterministic Pulse Width Jitter (16.0 GT/s)	4460	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
EndPoint Tests, Uncorrelated Total Pulse Width Jitter (16.0 GT/s)	4450	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
EndPoint Tests, Unit Interval (16.0 GT/s)	4400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval (2.5 GT/s)	200	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval (2.5 GT/s)	1300	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval (2.5 GT/s)	2301	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval (8.0 GT/s)	3400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval -3.5dB (5.0 GT/s)	2300	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
EndPoint Tests, Unit Interval -6.0dB (5.0 GT/s)	2302	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
ExpressCard Host Tx, Eye-Width (EC 1.0, 2.5 GT/s)	703	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
ExpressCard Host Tx, Median to Max Jitter (EC 1.0, 2.5 GT/s)	702	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
ExpressCard Host Tx, Peak Differential Output Voltage (EC 1.0, 2.5 GT/s)	707	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
ExpressCard Host Tx, Template Tests (EC 1.0, 2.5 GT/s)	710	ExpressCard Hosts must meet the ExpressCard Host Transmitter Path Compliance Eye Requirements specified in table 4-5 of section 4.2.1 of the ExpressCard(TM) Standard, referenced to an ideal 100 ohm load at the end of the interconnect path at the isolated module connector pad boundary of an ExpressCard Module when mated with a connector.
ExpressCard Host Tx, Unit Interval (EC 1.0, 2.5 GT/s)	700	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
ExpressCard Module Tx, Eye-Width (EC 1.0)	603	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
ExpressCard Module Tx, Median to Max Jitter (EC 1.0, 2.5 GT/s)	602	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
ExpressCard Module Tx, Peak Differential Output Voltage (EC 1.0, 2.5 GT/s)	607	This test verifies that the Peak Differential Output Voltage is within the allowed range.
ExpressCard Module Tx, Template Tests (EC 1.0, 2.5 GT/s)	610	ExpressCard Modules must meet the ExpressCard Module Transmitter Path Compliance Eye Requirements specified in table 4-3 of section 4.2.1 of the ExpressCard(TM) Standard, referenced to an ideal 100 ohm load at the end of the interconnect path at the module connector pad boundary.
ExpressCard Module Tx, Unit Interval (EC 1.0, 2.5 GT/s)	600	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
No tests available	9999	
Reference Clock, Absolute Crossing Point Voltage (2.5 GT/s)	880	This test verifies that the absolute crossing point voltage of the reference clock single-ended waveforms is within the allowed range.
Reference Clock, Absolute Max Input Voltage (2.5 GT/s)	900	This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.
Reference Clock, Absolute Min Input Voltage (2.5 GT/s)	910	This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.
Reference Clock, Average Clock Period (2.5 GT/s)	860	The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Clock Frequency (Common Clk)(16.0 GT/s)	4810	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Clock Frequency (Common Clk)(8.0 GT/s)	3810	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Clock Frequency (Data Clk) (16.0 GT/s)	4860	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Clock Frequency (Data Clk) (8.0 GT/s)	3860	This test verifies that the measured reference clock frequency, FREFCLK, is within than the allowed frequency range.
Reference Clock, Differential Input High Voltage (2.5 GT/s)	840	This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.
Reference Clock, Differential Input Low Voltage (2.5 GT/s)	850	This test verifies that the low voltage of the reference clock differential waveform is less than the maximum allowed value.
Reference Clock, Duty Cycle (2.5 GT/s)	870	This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.
Reference Clock, Falling Edge Rate (2.5 GT/s)	830	This test verifies that the falling edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, Full SSC Modulation (Data Clk) (5.0 GT/s)	2870	This test verifies that the reference clock full SSC modulation is less than the maximum allowed value.
Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	2810	This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.
Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	2860	This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.
Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (5.0 GT/s)	2830	This test verifies that the reference clock TREFCLK-LF-RMS is less than the maximum allowed value.
Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (5.0 GT/s)	2880	This test verifies that the RMS reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.
Reference Clock, Maximum SSC Slew Rate (Common Clk) (5.0GT/s)	2850	This test verifies that the reference clock SSC slew rate is less than the maximum allowed value.
Reference Clock, Maximum SSC Slew Rate (Data Clk) (5.0 GT/s)	2895	This test verifies that the reference clock SSC slew rate is less than the maximum allowed value.
Reference Clock, Peak to Peak (Common Clk) (2.5 GT/s)	1900	This test verifies that the measured Peak to Peak jitter, TREFCLK-PP-CC, is less than the maximum allowed value.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, Phase Jitter (2.5 GT/s)	810	This test verifies that the magnitude of the peak-peak reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (16.0 GT/s)	4900	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (5.0 GT/s)	2900	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	3820	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Common Clk) (8.0 GT/s)	3900	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (16.0 GT/s)	4901	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (2.5 GT/s)	1901	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (5.0 GT/s)	2901	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)	3870	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, RMS Jitter (Data Clk) (8.0 GT/s)	3901	This test verifies that the measured RMS jitter, TREFCLK-RMS-DC, is less than the maximum allowed value.
Reference Clock, Rise-Fall Matching (2.5 GT/s)	920	This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.
Reference Clock, Rising Edge Rate (2.5 GT/s)	820	This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.
Reference Clock, SSC Deviation (Common Clk) (16.0GT/s)	4840	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Common Clk) (5.0GT/s)	2840	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Deviation (Common Clk) (8.0GT/s)	3840	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk) (5.0 GT/s)	2890	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk)(16.0GT/s)	4890	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Reference Clock, SSC Deviation (Data Clk)(8.0GT/s)	3890	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Data Clk)(Min)(8.0GT/s)	3891	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Common Clk) (5.0GT/s)	2841	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Common Clk) (8.0GT/s)	3841	This test verifies that the reference clock SSC deviation, TSSC-FREQ-DEVIATION, is less than the maximum allowed value.
Reference Clock, SSC Deviation (Min)(Data Clk) (5.0 GT/s)	2891	This test verifies that the reference clock SSC deviation is less than the maximum allowed value.
Reference Clock, SSC Frequency Range (Common Clk) (16.0 GT/s)	4830	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Frequency Range (Common Clk) (8.0 GT/s)	3830	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Frequency Range (Data Clk) (16.0 GT/s)	4880	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Frequency Range (Data Clk) (8.0 GT/s)	3880	This test verifies that the measured SSC frequency, FSSC, is within the allowed SSC frequency range.
Reference Clock, SSC Residual (Common Clk) (5.0 GT/s)	2820	This test verifies that the measured SSC residual is less than the maximum allowed value.
Reference Clock, Variation of VCross (2.5 GT/s)	890	This test verifies that the variation of VCross over all rising clock edges is within the allowed range.
RootComplex Tests - SigTest (16.0 GT/s) - Far End	5029	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-21 of section 4.8.12 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. This test considered a physical ISI channel and a package model embedded with InfiniiSim.
RootComplex Tests - SigTest (16.0 GT/s) - Near End	5027	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-21 of section 4.8.12 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers. This test is run without InfiniiSim embedding and without an ISI channel added to the CBB.
RootComplex Tests - SigTest (2.5 GT/s)	5006	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.0a, as measured after the connector with an ideal load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
RootComplex Tests - SigTest (2.5 GT/s)	5007	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.1, as measured after the connector with an ideal load.
RootComplex Tests - SigTest (5.0 GT/s) -3.5dB	5008	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests - SigTest (5.0 GT/s) -6.0dB	50008	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests - SigTest (8.0 GT/s)	5009	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-19 of section 4.8.9 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	2496	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	2497	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests, Eye Width (16.0 GT/s)	4540	System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
RootComplex Tests, Eye-Width (2.5 GT/s)	403	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
RootComplex Tests, Eye-Width (2.5 GT/s)	1430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
RootComplex Tests, Eye-Width (2.5 GT/s)	2432	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Table 4 Test IDs and Names (continued)

Name	TestID	Description
RootComplex Tests, Eye-Width (8.0 GT/s)	3530	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	2430	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	2431	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	2492	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	2493	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.
RootComplex Tests, Median to Max Jitter (2.5 GT/s)	402	This test measures the maximum time between the jitter median and maximum deviation from the median.
RootComplex Tests, Median to Max Jitter (2.5 GT/s)	1420	This test measures the maximum time between the jitter median and maximum deviation from the median.
RootComplex Tests, Median to Max Jitter (2.5 GT/s)	2420	This test measures the maximum time between the jitter median and maximum deviation from the median.
RootComplex Tests, Peak Differential Output Voltage (2.5 GT/s)	407	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	2450	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	24500	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	44500	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Non Transition)(8.0 GT/s)	3521	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
RootComplex Tests, Peak Differential Output Voltage (Non-Transition) (16.0 GT/s)	4530	System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
RootComplex Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	1450	This test verifies that the Differential Peak Differential Output Voltage for non transition bits is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	2442	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition) (16.0 GT/s)	4520	System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.15 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	1440	This test verifies that the Differential Peak Differential Output Voltage for transition bits is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	2441	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	2440	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	24400	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	44400	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	3520	This test verifies that the Peak Differential Output Voltage is within the allowed range.
RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	2482	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	2483	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Template Tests (16.0 GT/s)	4510	System Board must meet the System Board Transmitter Path Compliance Eye Requirements specified section 4.8.5 of the PCI Express Card Electromechanical Specification (CEM) Rev 4.0, as measured at the card edge-fingers.
RootComplex Tests, Template Tests (2.5 GT/s)	2411	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-14 of section 4.7.5 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
RootComplex Tests, Template Tests (2.5 GT/s)	410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.0a, as measured after the connector with an ideal load.
RootComplex Tests, Template Tests (2.5 GT/s)	1410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.1, as measured after the connector with an ideal load.
RootComplex Tests, Template Tests (5.0 GT/s)	2410	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-17 of section 4.8.8 of the PCI Express Card Electromechanical (CEM) Specification, Rev 3.0, as measured after the connector with an ideal load.
RootComplex Tests, Template Tests (8.0 GT/s)	3510	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-19 of section 4.8.9 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
RootComplex Tests, Unit Interval (16.0 GT/s)	4500	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Unit Interval (2.5 GT/s)	400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Unit Interval (2.5 GT/s)	1400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Unit Interval (2.5 GT/s)	2401	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Unit Interval (5.0 GT/s)	2400	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
RootComplex Tests, Unit Interval (8.0 GT/s)	3500	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, AC Peak Common Mode Input Voltage (2.5 GT/s)	2250	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, AC Peak Common Mode Input Voltage (2.5 GT/s)	108	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, AC Peak Common Mode Input Voltage (2.5 GT/s)	1250	Receivers must reliably receive data when there is less than 150 mV of AC (>30 kHz) peak common mode input voltage. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Common RefClk Architecture Unit Interval (5.0 GT/s)	2202	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in the PCI Express Base Specification.
Rx, Common Refclk Architecture Maximum Deterministic Jitter (5.0 GT/s)	2294	This test verifies that the Deterministic Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Common Refclk Architecture Peak Differential Output Voltage (5.0 GT/s)	2243	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Common Refclk Architecture RMS Random Jitter (5.0 GT/s)	2284	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Rx, Common Refclk Architecture Template Test (5.0 GT/s)	2211	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Table 4-12 in the PCI Express Base Specification. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in Table 4-12.
Rx, Common Refclk Architecture Total Jitter at BER-12 (5.0 GT/s)	2298	This test verifies that the Total Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture Maximum Deterministic Jitter (5.0 GT/s)	2292	This test verifies that the Deterministic Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Data Clocked Architecture Peak Differential Output Voltage (5.0 GT/s)	2241	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture RMS Random Jitter (5.0 GT/s)	2282	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
Rx, Data Clocked Architecture Template Test (5.0 GT/s)	2210	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Table 4-12 in the PCI Express Base Specification. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in Table 4-12.
Rx, Data Clocked Architecture Total Jitter at BER-12 (5.0 GT/s)	2296	This test verifies that the Total Jitter is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Data Clocked Architecture Unit Interval (5.0 GT/s)	2200	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in the PCI Express Base Specification.
Rx, Eye-Width (2.5 GT/s)	2230	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, Eye-Width (2.5 GT/s)	103	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, Eye-Width (2.5 GT/s)	1230	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter]. Note that this test does NOT test the receiver's tolerance. Rather, it test the quality of the signal as the receiver would see it. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Long Channel CM Optimization (8.0 GT/s)	3695	This procedure minimizes the difference between the two components ofCM sinusoidal interference for Long Channel 8.0 Gbit/s.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Long Channel CM Sinusoidal Interference Calibration (8.0 GT/s)	3700	This procedure calibrates CM sinusoidal interference for Long Channel 8.0 Gbit/s.
Rx, Long Channel DM Sinusoidal Interference Calibration (8.0 GT/s)	3705	This procedure calibrates the differential mode sinusoidal interference for Long Channel 8.0 Gbit/s.
Rx, Long Channel Generator Launch Voltage Calibration (8.0 GT/s)	3690	This procedure calibrates the generator launch voltage for Long Channel 8.0 Gbit/s.
Rx, Long Channel Insertion Loss Calibration (8.0 GT/s)	3715	This procedure calculates the insertion loss at different de-emphasis levels for Long Channel 8.0 Gbit/s.
Rx, Long Channel Random Jitter Calibration (8.0 GT/s)	3710	This procedure calibrates random jitter for Long Channel 8.0 Gbit/s.
Rx, Long Channel Stressed Jitter Calibration (8.0 GT/s)	3730	
Rx, Long Channel Stressed Voltage Calibration (8.0 GT/s)	3720	This procedure calibrates the eye height for Long Channel 8.0 Gbit/s by adding CM differential interference at different launch voltage levels.
Rx, Median to Max Jitter (2.5 GT/s)	2220	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12 of the PCI Express Base Specification, Rev 2.0.
Rx, Median to Max Jitter (2.5 GT/s)	102	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, Median to Max Jitter (2.5 GT/s)	1220	Receivers must be able to reliably receive data with up to 120 ps between the jitter median and maximum deviation from the median. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, No Channel CM Optimization(8.0 GT/s)	3605	This procedure minimizes the difference between the two components of CM Sinusoidal Interference for No Channel 8.0 Gbit/s.
Rx, No Channel CM Sinusoidal Interference Calibration (8.0 GT/s)	3610	This procedure calibrates CM Sinusoidal Interference for No Channel 8.0 Gbit/s.
Rx, No Channel DM Sinusoidal Interference Calibration (8.0 GT/s)	3615	This procedure calibrates the differential mode sinusoidal interference for No Channel 8.0 Gbit/s.
Rx, No Channel Generator Launch Voltage Calibration(8.0 GT/s)	3600	This procedure calibrates the generator launch voltage for No Channel 8.0 Gbits/s.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, No Channel Insertion Loss Calibration (8.0 GT/s)	3625	This procedure calculates the insertion loss at different de-emphasis levels for No Channel 8.0 Gbit/s.
Rx, No Channel Random Jitter Calibration (8.0 GT/s)	3620	The procedure calibrates random jitter for No Channel 8.0 Gbit/s.
Rx, No Channel Stressed Voltage Calibration (8.0 GT/s)	3630	This procedure calibrates the eye height for No Channel 8.0 GBit/s by adding CM differential interference at different launch levels.
Rx, Peak Differential Output Voltage (2.5 GT/s)	2240	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Peak Differential Output Voltage (2.5 GT/s)	107	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Peak Differential Output Voltage (2.5 GT/s)	1240	This test verifies that the Peak Differential Output Voltage is within the allowed range. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Short Channel CM Optimization (8.0 GT/s)	3650	This procedure minimizes the difference between the two components of CM sinusoidal interference for Short Channel 8.0 Gbit/s.
Rx, Short Channel CM Sinusoidal Interference Calibration (8.0 GT/s)	3655	This procedure calibrates CM sinusoidal interference for Short Channel 8.0 GBit/s.
Rx, Short Channel DM Sinusoidal Interference Calibration (8.0 GT/s)	3660	This procedure calibrates the differential mode sinusoidal interference for Short Channel 8.0 Gbit/s.
Rx, Short Channel Generator Launch Voltage Calibration (8.0 GT/s)	3645	This procedure calibrates the generator launch voltage for Short Channel 8.0 Gbit/s.
Rx, Short Channel Insertion Loss Calibration (8.0 GT/s)	3670	This procedure calculates the insertion loss at different de-emphasis levels for Short Channel 8.0 Gbit/s.
Rx, Short Channel Random Jitter Calibration (8.0 GT/s)	3665	This procedure calibrates random jitter for Short Chanel 8.0 Gbit/s.
Rx, Short Channel Stressed Voltage Calibration (8.0 GT/s)	3675	This procedure calibrates the eye height for Short Channel 8.0 Gbit/s by adding CM differential interference at different launch voltage levels.
Rx, Template Test (2.5 GT/s)	110	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Figure 4-26: Minimum Receiver Eye Timing and Voltage Compliance Specification as shown in the PCI Express Base Specification, Rev 1.0. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Rx, Template Test (2.5 GT/s)	1210	The receiver must reliably receive all data that meets the differential receiver input specifications as shown in Figure 4-26: Minimum Receiver Eye Timing and Voltage Compliance Specification as shown in the PCI Express Base Specification, Rev 1.1. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6.
Rx, Template Test (2.5 GT/s)	2212	The receiver must reliably receive all data that meets the differential receiver input specifications in the PCI Express Base Specification, Rev 2.0. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-12.
Rx, Unit Interval (2.5 GT/s)	100	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.0a.
Rx, Unit Interval (2.5 GT/s)	1200	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications in table 4-6 of the PCI Express Base Specification, Rev 1.1.
Rx, Unit Interval (2.5 GT/s)	2201	A recovered RX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered RX UI is reported here. This test does NOT validate the receiver's tolerance, but rather that the signal at the receiver meets the specifications of the PCI Express Base Specification, Rev 2.0.
Signal Acquisition For PCIE 1, PCIE 2 and PCIE 3 (8.0 GT/s)	33301	
Signal Acquisition Preset #00 until Preset #10 (8.0 GT/s)	33300	
Tx, AC common mode voltage - 2.5GHz LPF (5.0 GT/s)	3170	The maximum allowable Tx AC peak-peak common mode voltage is 150mVpp (Vtx-cm-ac-pp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, AC common mode voltage - 30kHz to 500MHz (16.0 GT/s)	4170	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-CM-AC-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 30kHz to 500MHz (5.0 GT/s)	3175	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-CM-AC-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, AC common mode voltage - 30kHz to 500MHz (8.0 GT/s)	3022	This test verify the AC common mode lies in the 0.03-500MHz range, VTX-CM-AC-PP (30kHz - 500MHz) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 4GHz LPF (8.0 GT/s)	3021	This test verify the AC common mode, VTX-CM-AC-PP (4GHz LPF) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, AC common mode voltage - 8GHz LPF (16.0 GT/s)	4171	This test verify the AC common mode, VTX-CM-AC-PP (8GHz LPF) is within the allowed limit as specified in the PCI Express Base Specification. The peak-peak AC Common Mode voltage is reported here.
Tx, Absolute delta of DC common mode voltage between D+ and D- (16.0 GT/s)	4030	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage between D+ and D- (8.0 GT/s)	3030	This test verify the absolute delta of DC common mode voltage between D+ and D-, VTX-CM-DC-LINE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (16.0 GT/s)	4040	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE_IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (5.0 GT/s)	2040	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE_IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Absolute delta of DC common mode voltage during L0 and Idle (8.0 GT/s)	3040	This test verify the absolute delta of DC common mode voltage during L0 and Idle, VTX-CM-DC-ACTIVE_IDLE-DELTA is within the allowed limit as specified in the PCI Express Base Specification. This is absolute delta of the DC common mode voltage during active and electrical idle.
Tx, Avg DC Common Mode Voltage (2.5 GT/s)	6	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 1.0a. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Avg DC Common Mode Voltage (2.5 GT/s)	1180	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 1.1. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, Avg DC Common Mode Voltage (2.5 GT/s)	2181	This test measures VTX-DC-CM as specified in the PCI Express Base Specification, Rev 2.0. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, Avg DC Common Mode Voltage (5.0 GT/s)	2180	This test measures VTX-DC-CM as specified in the PCI Express Base Specification. This is the allowed DC Common Mode voltage under any conditions. The average DC Common Mode voltage is reported here.
Tx, DC Common Mode Line Delta (2.5 GT/s)	9	This test measures VTX-CM-DCLINE-DELTA as specified in Table 4-5 of the PCI Express Base Specification, Rev 1.0a. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (2.5 GT/s)	1184	This test measures VTX-CM-DCLINE-DELTA as specified in Table 4-5 of the PCI Express Base Specification, Rev 1.1. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (2.5 GT/s)	2185	This test measures VTX-CM-DCLINE-DELTA as specified in the PCI Express Base Specification, Rev 2.0. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Line Delta (5.0 GT/s)	2184	This test measures VTX-CM-DCLINE-DELTA as specified in the PCI Express Base Specification. This is absolute value of the difference between the average DC value of D+ and the average DC value of D-.
Tx, DC Common Mode Output Voltage Variation (2.5 GT/s)	11	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC Common Mode Output Voltage Variation (2.5 GT/s)	1182	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC Common Mode Output Voltage Variation (2.5 GT/s)	2182	The TX DC common mode voltage must fixed within the range of 0 to 3.6 V during all states. Any variation of this fixed value must be within +\- 100 mV.
Tx, DC common mode voltage (16.0 GT/s)	4010	This test verify the DC common mode, VTX-CM-DC is within the allowed limit as specified in the PCI Express Base Specification.
Tx, DC common mode voltage (8.0 GT/s)	3010	This test verify the DC common mode, VTX-CM-DC is within the allowed limit as specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Data dependent jitter (16.0 GT/s)	4130	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (2.5 GT/s)	1104	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (5.0 GT/s)	2104	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (8.0 GT/s)	43130	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, Data dependent jitter (8.0 GT/s)	3130	This test verifies that the maximum data dependent jitter, TTX-DDJ is within the allowed range.
Tx, De-emphasis Preset #0 (16.0 GT/s)	4220	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #0 (8.0 GT/s)	3220	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P0 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (16.0 GT/s)	4210	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #1 (8.0 GT/s)	3210	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P1 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #10 (16.0 GT/s)	4300	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in the PCI Express Base Specification. The P10 boost limits are not fixed. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-50 of the PCI Express Base Specification
Tx, De-emphasis Preset #10 (8.0 GT/s)	3300	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P10 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification. The P10 boost limits are not fixed. The allowable P10 boost range is defined by the coefficient space lying between the two diagonal lines in Figure 4-50 of the PCI Express Base Specification
Tx, De-emphasis Preset #2 (16.0 GT/s)	4290	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #2 (8.0 GT/s)	3290	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P2 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, De-emphasis Preset #3 (16.0 GT/s)	4280	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #3 (8.0 GT/s)	3280	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P3 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (16.0 GT/s)	4250	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #7 (8.0 GT/s)	3250	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (16.0 GT/s)	4240	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, De-emphasis Preset #8 (8.0 GT/s)	3240	The purpose of this test is to verify that the De-emphasis(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Deemphasized Voltage Ratio (2.5 GT/s)	5	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio (2.5 GT/s)	1160	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio (2.5 GT/s)	2160	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. The average de-emphasis value is tested against the specified value.
Tx, Deemphasized Voltage Ratio -3.5dB (5.0 GT/s)	2162	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -3.5dB.
Tx, Deemphasized Voltage Ratio -6.0dB (5.0 GT/s)	2164	This test measures the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition. This measurement is for de-emphasis level settings of -6dB.
Tx, Deterministic DjDD uncorrelated PWJ (16.0 GT/s)	4120	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Deterministic DjDD uncorrelated PWJ (2.5 GT/s)	1103	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (5.0 GT/s)	2103	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)	43120	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic DjDD uncorrelated PWJ (8.0 GT/s)	3120	This test verifies that the maximum deterministic DjDD uncorrelated PWJ TTX-UPW-DJDD is within the allowed range.
Tx, Deterministic Jitter > 1.5 MHz (5.0 GT/s)	2192	This test verifies that the high frequency(above 1.5MHz) Deterministic Jitter is within the allowed range.
Tx, Eye-Width (2.5 GT/s)	3	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s)	1130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s)	41130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s)	2130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s, Low Power)	10003	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s, Low Power)	11130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s, Low Power)	411130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (2.5 GT/s, Low Power)	12130	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
Tx, Eye-Width (5.0 GT/s)	2134	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
Tx, Eye-Width (5.0 GT/s)	42134	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Full swing Tx voltage with no TxEQ (16.0 GT/s)	4050	This test verifies that the full swing Tx voltage with no equalization VTX-FS-NO-EQ is within the allowed range.
Tx, Full swing Tx voltage with no TxEQ (8.0 GT/s)	3050	This test verifies that the full swing Tx voltage with no equalization VTX-FS-NO-EQ is within the allowed range.
Tx, Median to Max Jitter (2.5 GT/s)	2	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (2.5 GT/s)	1120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (2.5 GT/s)	2120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (2.5 GT/s, Low Power)	10002	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (2.5 GT/s, Low Power)	11120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Median to Max Jitter (2.5 GT/s, Low Power)	12120	This test measures the maximum time between the jitter median and maximum deviation from the median.
Tx, Min swing during EIEOS for full swing (16.0 GT/s)	4070	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for full swing (8.0 GT/s)	3070	This test verifies that the minimum swing during EIEOS for full swing VTX-EIEOS-FS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (16.0 GT/s, Low Power)	14070	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Min swing during EIEOS for reduced swing (8.0 GT/s, Low Power)	13080	This test verifies that the minimum swing during EIEOS for reduced swing VTX-EIEOS-RS is within the allowed range.
Tx, Peak Differential Output Voltage (2.5 GT/s, Low Power)	10007	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (2.5 GT/s, Low Power)	11140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (2.5 GT/s, Low Power)	12140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)	70	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)	11400	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(2.5 GT/s)	21400	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	2154	This test verifies that the Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Peak Differential Output Voltage (Non Transition)(5.0 GT/s, Low Power)	21540	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s)	2144	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition) (5.0 GT/s, Low Power)	21440	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s)	7	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s)	1140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Peak Differential Output Voltage (Transition)(2.5 GT/s)	2140	This test verifies that the Peak Differential Output Voltage is within the allowed range.
Tx, Preshoot Preset #5 (16.0 GT/s)	4260	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #5 (8.0 GT/s)	3260	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P5 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #6 (16.0 GT/s)	4270	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #6 (8.0 GT/s)	3270	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P6 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #7 (16.0 GT/s)	4251	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #7 (8.0 GT/s)	3251	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P7 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #8 (16.0 GT/s)	4241	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in the PCI Express Base Specification.
Tx, Preshoot Preset #8 (8.0 GT/s)	3241	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P8 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Preshoot Preset #9 (16.0 GT/s)	4230	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Preshoot Preset #9 (8.0 GT/s)	3230	The purpose of this test is to verify that the Preshoot(dB) of the transmitter Tx at preset number P9 is within the conformance limits specified in Table 4-16 of the PCI Express Base Specification.
Tx, Pseudo package loss (16.0 GT/s Non-root device)	4140	This test verifies that the maximum pseudo package loss for all devices not containing root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss (16.0 GT/s Root device)	414000	This test verifies that the maximum pseudo package loss of a devices containing root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss (8.0 GT/s Non-root device)	43140	This test verifies that the maximum pseudo package loss for all devices not containing root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss (8.0 GT/s Non-root device)	3140	This test verifies that the maximum pseudo package loss for all devices not containing root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss (8.0 GT/s Root device)	4314000	This test verifies that the maximum pseudo package loss of a devices containing root ports, ps21TX is within the allowed range.
Tx, Pseudo package loss (8.0 GT/s Root device)	314000	This test verifies that the maximum pseudo package loss of a devices containing root ports, ps21TX is within the allowed range.
Tx, RMS AC Peak Common Mode Output Voltage (2.5 GT/s)	8	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, RMS AC Peak Common Mode Output Voltage (2.5 GT/s)	1170	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, RMS AC Peak Common Mode Output Voltage (2.5 GT/s)	2170	The maximum allowable RMS AC (>30Khz) common mode voltage is 20mV (Vtx-cm-acp) as measured at the package pins of the transmitter using the Compliance Test and Measurement Load.
Tx, Random Jitter < 1.5 MHz (5.0 GT/s)	2194	This test verifies that the low frequency(10kH to 1.5MHz) Random Jitter(rms) is within the allowed range.
Tx, Random jitter (16.0 GT/s)	4160	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (2.5 GT/s)	1106	This test verifies that the random jitter, it is informative only.
Tx, Random jitter (5.0 GT/s)	2106	This test measures the RJ(p-p) for a DUT for informative only.
Tx, Random jitter (8.0 GT/s)	43160	This test verifies that the random jitter, it is informative only.
Tx, Reduced swing Tx voltage with no TxEQ (16.0 GT/s, Low Power)	14050	This test verifies that the reduced swing Tx output voltage with no equalization VTX-RS-NO-EQ is within the allowed range.
Tx, Reduced swing Tx voltage with no TxEQ (8.0 GT/s, Low Power)	13060	This test verifies that the reduced swing Tx output voltage with no equalization VTX-RS-NO-EQ is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Rise/Fall Time (2.5 GT/s)	4	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (2.5 GT/s)	1150	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (2.5 GT/s)	2151	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 10GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Rise/Fall Time (5.0 GT/s)	2150	This test verifies that the minimum rise and fall time (on both D+ and D- separately) is no less than the specified value. An oscilloscope and probe with at least 13GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, SSC Df/Dt (Max)(PCIE 4.0 16.0GT/s)	4390	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Df/Dt (Max)(PCIE 4.0 8.0GT/s)	43190	This test verifies that the SSC maximum slew rate is within the allowed range.
Tx, SSC Modulation Frequency (PCIE 4.0 16.0GT/s)	4370	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Modulation Frequency (PCIE 4.0 8.0GT/s)	43170	This test verifies that the SSC frequency range is in the allowable range.
Tx, SSC Peak Deviation (Max) (PCIE 4.0 16.0GT/s)	4380	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Max) (PCIE 4.0 8.0GT/s)	43180	This test verifies that the SSC maximum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 4.0 16.0GT/s)	4385	This test verifies that the SSC minimum deviation within the allowed range.
Tx, SSC Peak Deviation (Min) (PCIE 4.0 8.0GT/s)	43185	This test verifies that the SSC minimum deviation within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Template Tests (2.5 GT/s)	10	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification, Rev 1.0a, Section 4.3.3.1, Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications as measured at the package pins into the Compliance Test and Measurement Load, defined in section 4.3.3.2
Tx, Template Tests (2.5 GT/s)	1110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification, Rev 1.1, Section 4.3.3.1, Figure 4-24: Minimum Transmitter Timing and Voltage Output Compliance Specifications as measured at the package pins into the Compliance Test and Measurement Load, defined in section 4.3.3.2
Tx, Template Tests (2.5 GT/s)	41110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (2.5 GT/s)	2110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (2.5 GT/s, Low Power)	10010	All PCI Express Device Types must meet the Transmitter eye diagram as specified in Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0, Figure 2.2
Tx, Template Tests (2.5 GT/s, Low Power)	411110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in PCIE Base Specification.
Tx, Template Tests (2.5 GT/s, Low Power)	11110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the Mobile Graphic Low Power Addendum to The PCIE Base Specification 1.0, Figure 2.2
Tx, Template Tests (2.5 GT/s, Low Power)	12110	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification
Tx, Template Tests (5.0 GT/s)	21141	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (5.0 GT/s)	2114	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (5.0 GT/s)	42114	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (5.0 GT/s, Low Power)	21140	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.
Tx, Template Tests (5.0 GT/s, Low Power)	421140	All PCI Express Device Types must meet the Transmitter eye diagram as specified in the PCI Express Base Specification.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Tmin-Pulse (5.0 GT/s)	2152	This test verifies that the minimum pulse width is no less than the specified value. An oscilloscope and probe with at least 13GHz bandwidth is recommended for accurate characterization of PCI-Express rise times less than 50ps. If the number is close to the specified value, you may need to verify this measurement with a higher bandwidth oscilloscope.
Tx, Total uncorrelated PWJ (16.0 GT/s)	4110	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (2.5 GT/s)	1102	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (5.0 GT/s)	2102	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (8.0 GT/s)	43110	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Total uncorrelated PWJ (8.0 GT/s)	3110	This test verifies that the maximum total uncorrelated PWJ TTX-UPW-TJ is within the allowed range.
Tx, Uncorrelated deterministic jitter (16.0 GT/s)	4100	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (2.5 GT/s)	1101	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (5.0 GT/s)	2000	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (8.0 GT/s)	43100	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated deterministic jitter (8.0 GT/s)	3100	This test verifies that the maximum uncorrelated deterministic jitter TTX-UDJDD is within the allowed range.
Tx, Uncorrelated total jitter (16.0 GT/s)	4090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (2.5 GT/s)	1090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (5.0 GT/s)	2090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (8.0 GT/s)	3090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Uncorrelated total jitter (8.0 GT/s)	43090	This test verifies that the maximum uncorrelated total jitter TTX-UTJ is within the allowed range.
Tx, Unit Interval (2.5 GT/s)	1	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Tx, Unit Interval (2.5 GT/s)	1100	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit Interval (2.5 GT/s)	2101	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit Interval (5.0 GT/s)	2100	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here.
Tx, Unit interval (16.0 GT/s)	4000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.
Tx, Unit interval (8.0 GT/s)	3000	The purpose of this test is to verify that the unit interval measured at the transmitter Tx is within the conformance limits specified in Table 4-19 of the PCI Express Base Specification.
U.2 EndPoint Tests - SigTest (2.5 GT/s)	5010	Compliance mode test for U.2 type DUT.
U.2 EndPoint Tests - SigTest (5.0 GT/s) -3.5dB	5012	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in the PCI Express U.2 Specification.
U.2 EndPoint Tests - SigTest (5.0 GT/s) -6.0dB	5014	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in PCI Express U.2 Specification.
U.2 EndPoint Tests - SigTest (8.0 GT/s)	5016	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in PCI Express U.2 Specification.
U.2 EndPoint Tests, Eye-Width (2.5 GT/s)	18005	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
U.2 EndPoint Tests, Eye-Width (8.0 GT/s)	38004	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
U.2 EndPoint Tests, Eye-Width -3.5dB with crosstalk (5.0 GT/s)	28008	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
U.2 EndPoint Tests, Eye-Width -3.5dB without crosstalk (5.0 GT/s)	28016	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [TJ at BER-12].
U.2 EndPoint Tests, Eye-Width -6.0dB with crosstalk (5.0 GT/s)	28012	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
U.2 EndPoint Tests, Eye-Width -6.0dB without crosstalk (5.0 GT/s)	28020	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Table 4 Test IDs and Names (continued)

Name	TestID	Description
U.2 EndPoint Tests, Maximum Deterministic Jitter -3.5dB with crosstalk (5.0 GT/s)	28010	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Maximum Deterministic Jitter -3.5dB without crosstalk (5.0 GT/s)	28018	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Maximum Deterministic Jitter -6.0dB with crosstalk (5.0 GT/s)	28014	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Maximum Deterministic Jitter -6.0dB without crosstalk (5.0 GT/s)	28022	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Median to Max Jitter (2.5 GT/s)	18002	This test measures the maximum time between the jitter median and maximum deviation from the median. The specified and measured values are shown in picoseconds here.
U.2 EndPoint Tests, Peak Differential Output Voltage (Non Transtion)(8.0 GT/s)	38003	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	18004	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	18003	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	38002	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage -3.5dB (Non-Transition)(5.0 GT/s)	28003	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage -3.5dB (Transition) (5.0 GT/s)	28002	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage -6.0dB (Non Transition)(5.0 GT/s)	28007	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, Peak Differential Output Voltage -6.0dB (Transition)(5.0 GT/s)	28006	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 EndPoint Tests, RMS Random Jitter -3.5dB with crosstalk (5.0 GT/s)	28009	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
U.2 EndPoint Tests, RMS Random Jitter -3.5dB without crosstalk (5.0 GT/s)	28017	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
U.2 EndPoint Tests, RMS Random Jitter -6.0dB with crosstalk (5.0 GT/s)	28013	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
U.2 EndPoint Tests, RMS Random Jitter -6.0dB without crosstalk (5.0 GT/s)	28021	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
U.2 EndPoint Tests, Template Tests (2.5 GT/s)	18001	U.2 Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Template Tests (8.0 GT/s)	38001	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements specified in table 4-11 of section 4.8.3 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
U.2 EndPoint Tests, Template Tests -3.5dB (5.0 GT/s)	28001	U.2 Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Template Tests -6.0dB (5.0 GT/s)	28005	U.2 Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Total Jitter at BER-12 -3.5dB with crosstalk (5.0 GT/s)	28011	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Total Jitter at BER-12 -3.5dB without crosstalk (5.0 GT/s)	28019	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Total Jitter at BER-12 -6.0dB with crosstalk (5.0 GT/s)	28015	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Total Jitter at BER-12 -6.0dB without crosstalk (5.0 GT/s)	28023	Add-in cards must meet the Add-in Card Transmitter Path Compliance Eye Requirements.
U.2 EndPoint Tests, Unit Interval (2.5 GT/s)	18000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
U.2 EndPoint Tests, Unit Interval (8.0 GT/s)	38000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
U.2 EndPoint Tests, Unit Interval -3.5dB (5.0 GT/s)	28000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
U.2 EndPoint Tests, Unit Interval -6.0dB (5.0 GT/s)	28004	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
U.2 RootComplex Tests - SigTest (2.5 GT/s)	5020	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in PCI Express U.2 Specification.
U.2 RootComplex Tests - SigTest (5.0 GT/s)	5022	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in PCI Express U.2 Specification.
U.2 RootComplex Tests - SigTest (8.0 GT/s)	5024	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in PCI Express U.2 Specification.
U.2 RootComplex Tests, Total Jitter at BER-12 with crosstalk (5.0 GT/s)	27007	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Total Jitter at BER-12 without crosstalk (5.0 GT/s)	27011	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Eye-Width (2.5 GT/s)	17005	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
U.2 RootComplex Tests, Eye-Width (8.0 GT/s)	37004	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] -[TJ at BER -12].
U.2 RootComplex Tests, Eye-Width with crosstalk (5.0 GT/s)	27004	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
U.2 RootComplex Tests, Eye-Width without crosstalk (5.0 GT/s)	27008	This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].
U.2 RootComplex Tests, Maximum Deterministic Jitter with crosstalk (5.0 GT/s)	27006	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Maximum Deterministic Jitter without crosstalk (5.0 GT/s)	27010	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Median to Max Jitter (2.5 GT/s)	17002	This test measures the maximum time between the jitter median and maximum deviation from the median.
U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition)(5.0 GT/s)	27003	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
U.2 RootComplex Tests, Peak Differential Output Voltage (Non Transition)(8.0 GT/s)	37003	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 RootComplex Tests, Peak Differential Output Voltage (NonTransition)(2.5 GT/s)	17004	This test verifies that the Peak Differential Output Voltage for non transition bits is within the allowed range.
U.2 RootComplex Tests, Peak Differential Output Voltage (Transition)(2.5 GT/s)	17003	This test verifies that the Peak Differential Output Voltage for transition bits is within the allowed range.
U.2 RootComplex Tests, Peak Differential Output Voltage (Transition)(5.0 GT/s)	27002	This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.
U.2 RootComplex Tests, Peak Differential Output Voltage (Transition)(8.0 GT/s)	37002	This test verifies that the Peak Differential Output Voltage is within the allowed range.
U.2 RootComplex Tests, RMS Random Jitter with crosstalk (5.0 GT/s)	27005	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
U.2 RootComplex Tests, RMS Random Jitter without crosstalk (5.0 GT/s)	27009	The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.
U.2 RootComplex Tests, Template Tests (2.5 GT/s)	17001	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Template Tests (5.0 GT/s)	27001	System boards must meet the System Board Transmitter Path Compliance Eye Requirements.
U.2 RootComplex Tests, Template Tests (8.0 GT/s)	37001	System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-19 of section 4.8.9 of the PCI Express Card Electromechanical Specification (CEM) Rev 2.0, as measured at the card edge-fingers.
U.2 RootComplex Tests, Unit Interval (2.5 GT/s)	17000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
U.2 RootComplex Tests, Unit Interval (5.0 GT/s)	27000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.
U.2 RootComplex Tests, Unit Interval (8.0 GT/s)	37000	A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 6 Instrument Names

Instrument Name	Description
81150A	81150A
Infiniium	Infiniium
N4903B	N4903B
PFAGenerator	PFAGenerator
scope	The primary oscilloscope

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