PCI Express Gen 5 Specification & latest information of Gen 4 testing

Internet Infrastructure, CSG
Rick Eads
Agenda

• PCI Express 5.0 Motivation to 32GT/s
• PCIe 5.0 Development Timeline
• PCIe 5.0 Goals
• PCIe 5.0 Electrical Details
• PCIe 5.0 Logical Phy (LTSSM) changes
• PCIe 4.0 Test Tools
• Keysight PCIe Challenger Message
Justification for PCIe Gen5

**PCIe 5.0 Spec w/ 32 GT/s Bandwidth Ideal for:**

- High end networking solutions (400 Gb Ethernet and dual 200Gb/s InfiniBand technologies)
- Accelerator and GPU attachments for high bandwidth applications
- Constricted form factors that cannot increase lane width but need higher bandwidth
- Continued use of L1 sub states to constrain power consumption during idle transmission periods
Drivers of PCIe Performance

- High end networking
  - 400Gb Ethernet
  - Dual 200Gb/s InfiniBand

- Storage Networking
  - NVM Express
  - Big Data

- Increased IC I/O Speeds
  - FPGA
  - ASIC
  - IP
Industry Drives Higher PCIe Bandwidth Requirements

- PCIe 5.0 = 32 Gb/s
- Required for 400Gb Ethernet
  - This equates to 50GB bidirectionally
  - 16 lanes gives up to 64GB/s
  - Total full duplex BW = 128 GB/s
- CEM connector for PCIe 5 is planned to be backward compatible with earlier PCIe technologies.
- Tentative schedule for spec release in 2019

<table>
<thead>
<tr>
<th></th>
<th>Raw Bit Rate/Lane</th>
<th>Link BW</th>
<th>BW/Lane</th>
<th>Total x16 Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 1.x</td>
<td>2.5GT/s</td>
<td>2Gb/s</td>
<td>250 MB/s</td>
<td>8GB/s</td>
</tr>
<tr>
<td>PCIe 2.x</td>
<td>5.0GT/s</td>
<td>4Gb/s</td>
<td>500 MB/s</td>
<td>16GB/s</td>
</tr>
<tr>
<td>PCIe 3.x</td>
<td>8.0GT/s</td>
<td>8Gb/s</td>
<td>~1GB/s</td>
<td>~32GB/s</td>
</tr>
<tr>
<td>PCIe 4.x</td>
<td>16.0GT/s</td>
<td>16Gb/s</td>
<td>~2GB/s</td>
<td>~64GB/s</td>
</tr>
<tr>
<td>PCIe 5.x</td>
<td>32.0GT/s</td>
<td>32 Gb/s</td>
<td>~4GB/s</td>
<td>~128 GB/s</td>
</tr>
</tbody>
</table>
PCI Express Technology Roadmap

- PCIe 1.0 (2.5 GT/s) 2003
- PCIe 2.0 (5 GT/s) 2006
- PCIe 3.0 (8 GT/s) 2010
- PCIe 4.0 (16 GT/s) 2017
- PCIe 5.0 (32 GT/s) 2019

Timeline:
- 2003
- 2006
- 2010
- 2017
- 2019
PCI Express Standards Development

PCISIG Board of Directors
KEYSIGHT, Intel, AMD, IBM, Synopsys, Qualcomm, Dell, HP, NVIDIA

Electrical Work Group
Protocol Work Group
Card Electromechanical Work Group
Serial Enabling Work Group

Deliverables:
Group Chairs:
- Electrical Spec
  AMD, Intel
- Protocol Spec
  AMD, Intel
- CEM Spec
  Intel
- Test Specification
  & Plugfests
  Intel, Synopsys

PCI Express 5.0
PCI Express 5.0 Timeline (estimated)

- Draft 0.3 June 2017
- Draft 0.5 December 2017
- Draft 0.7 May 2018
- Draft 0.9 Stretch Goal end of 2018
- Final 1.0 “first half of 2019”
PCI Express 5.0 Specifications and Scope

**Base Specification**
- Contains all the system knowledge
- Can directly be applied to Chip Test

**Card Electromechanical (CEM) Spec**
- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer’s need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

**Phy Test Specification**
- Defines compliance tests of CEM spec in detail

**Select the specifications that relate to your specific need**
PCI Express Specifications and Scope

**Base Specification**
- Contains all the system knowledge
- Can directly be applied to Chip Test

**Card Electromechanical (CEM) Spec**
- Applies to Add-In Cards and Mother Boards
- Mitigates card manufacturer’s need to study the base specification
- Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

**Phy Test Specification**
- Defines compliance tests of CEM spec in detail

PCIe 5.0 BASE
Currently at v0.7
PCIe 5.0 – Goals

DELIVERING THE FASTEST PCIE SPEED YET

• PCIe 5.0 is backwards compatible with prior generations.
  • Enhanced SMT connector
  • Same pinout

• Signaling is doubled (vGen4) to 32GT/s
  • Minimal spec changes – only ones needed to enable speed bump.
  • EIEOS changed to maintain frequency
  • Data rate bit defined
  • Encoding remains 128/130
  • Loss budget: Goal 35-36dB.
  • Equalization: 8GT->16GT-> 32GT/s

• Scaled flow control & extended tags from PCIe 4.0 sufficient for 32GT/s.
• BER target is 10e-12
• TX Presets P0-P10 to remain the same
• Backward compatibility with previous PCIe Gen1/2/3/4
• Same approach for TX and RX testing used for Gen4
  • Similar method for TX testing via de-embedding of breakout board traces
  • Similar method for calibrating the eye width and eye height as used with PCIe 4.0 (ISI based, fixed RJ)
• Same TX Voltage and Jitter parameters as Gen4
32 GT/s Targets

• Supports both common clock and SRIS
  • SSC PPM now 3000ppm

• Proposed CDR of 20MHz 2nd order at 32 GT/s

• Reference Receiver = CTLE+DFE (3 taps)
  32.0 GT/s behavioral Rx equalization defines a 2\textsuperscript{nd} order CTLE with fixed poles, and an adjustable DC gain (A\textsubscript{DC}). The A\textsubscript{DC} is adjustable over a range of -5 to -15 dB in steps of 1.0 dB. It has 4 poles and 2 zeros

\[
H(s) = \frac{\omega_{P1} \cdot \omega_{P2} \cdot \omega_{P4}}{\omega_{Z1}} \cdot \frac{(s + \omega_{Z1})(s + \omega_{P2} \cdot A_{DC})}{(s + \omega_{P1})(s + \omega_{P2})(s + \omega_{P3})(s + \omega_{P4})}
\]

• Eye Target Post EQ
  • 10mV EH, .3UI EW (9.375ps)
<table>
<thead>
<tr>
<th>Label</th>
<th>Jitter Parameter</th>
<th>2.5 GT/s</th>
<th>5.0 GT/s</th>
<th>8.0 GT/s</th>
<th>16.0 GT/s</th>
<th>32.0 GT/s (proposed)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_{TX-UTJ}</td>
<td>Tx uncorrelated total jitter</td>
<td>100 (max)</td>
<td>50 (max)</td>
<td>27.55 (max)</td>
<td>11.8 (max)</td>
<td>6.25 (max)</td>
<td>ps PP at 10^{-12} BER</td>
</tr>
<tr>
<td>T_{TX-UTJ-SRIS}</td>
<td>Tx uncorrelated total jitter when testing for the IR clock mode with SSC</td>
<td>100 (max)</td>
<td>66.51 (max)</td>
<td>33.83 (max)</td>
<td>15.85 (max)</td>
<td>7.15 (max)</td>
<td>ps PP at 10^{-12}</td>
</tr>
<tr>
<td>T_{TX-UDJDD}</td>
<td>Tx uncorrelated Dj for non-embedded Refclk</td>
<td>100 (max)</td>
<td>30 (max)</td>
<td>12 (max)</td>
<td>6.25 (max)</td>
<td>3.125 (max)</td>
<td>ps PP</td>
</tr>
<tr>
<td>T_{TX-UPW-TJ}</td>
<td>Total uncorrelated pulse width jitter</td>
<td>N/A</td>
<td>40 (max)</td>
<td>24 (max)</td>
<td>12.5 (max)</td>
<td>6.25 (max)</td>
<td>ps PP at 10^{-12}</td>
</tr>
<tr>
<td>T_{TX-UPWDJDD}</td>
<td>Deterministic DjDD uncorrelated pulse width jitter</td>
<td>N/A</td>
<td>40 (max)</td>
<td>10 (max)</td>
<td>5 (max)</td>
<td>2.5 (max)</td>
<td>ps PP</td>
</tr>
<tr>
<td>T_{TX-RJ}</td>
<td>Tx Random jitter</td>
<td>N/A</td>
<td>1.4 – 3.6</td>
<td>1.17 – 1.97</td>
<td>0.40 – 0.84</td>
<td>.23-.45</td>
<td>ps RMS</td>
</tr>
</tbody>
</table>
PCI Express 5.0 CTLE Equalization (Reference EQ)

INCLUDES + DC GAIN

\[
H(s) = \frac{\omega_p1 \omega_p3 \omega_p4}{\omega_{z1}} + \frac{(s + \omega_{z1})(s + \omega_{p2} A_{DC})}{(s + \omega_{p1})(s + \omega_{p2})(s + \omega_{p3})(s + \omega_{p4})}
\]

- \( \omega = 2 \cdot 3.14 \cdot \text{Frequency} \)
- \( F_{p1} = 1.65 \cdot F_{z1}, F_{p2} = 9.5 \text{GHz}, \)
- \( F_{p3} = 28 \text{GHz}, F_{p4} = 28 \text{GHz} \)
- \( F_{z1} = 450 \text{MHz}, F_{z2} = \text{mag(DC gain)} \cdot F_{p2} \)
- \( \text{ADC} = -5 \text{dB to } -15 \text{dB} \)
- No broadband gain
PCI Express 5.0 Channel Topology

- End-to-end loss target = -36dB @ 16GHz
- Root package loss = -9dB @ 16GHz
- Add-in Card package loss (non root) = -4dB @ 16 GHz
- Total add-in card loss budget = TBD
- PCIe 5.0 CEM Connector loss = 1.5dB @ 16 GHz
PCIe 5.0 Reference Clock and PLL Bandwidth Requirements

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>CC Jitter Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5GT/s</td>
<td>86ps (pk-pk)</td>
</tr>
<tr>
<td>5GT/s</td>
<td>3.1ps (RMS)</td>
</tr>
<tr>
<td>8GT/s</td>
<td>1.0ps (RMS)</td>
</tr>
<tr>
<td>16GT/s</td>
<td>0.5ps (RMS)</td>
</tr>
<tr>
<td>32GT/s</td>
<td>0.15ps (RMS)</td>
</tr>
</tbody>
</table>

- PCIe 5.0 specifies a short channel and a 50 ohm termination (100 ohm differential termination) for reference clock phase jitter measurements only.
- Lower PLL bandwidth limit for 8.0 and 16.0 GT/s now reduced to 0.5 MHz
  - Revised model CDR at 16GT/s to aid backward compatibility
  - Reduced TX UTJ limit at 8GT/s to aid backward compatibility

### PLL 

<table>
<thead>
<tr>
<th>BW_{PLL(min)} (MHz)</th>
<th>BW_{PLL(max)} (MHz)</th>
<th>\phi_{n1}</th>
<th>\phi_{n2}</th>
<th>\zeta_{1}</th>
<th>\zeta_{2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>1.8</td>
<td>.112</td>
<td>4.03</td>
<td>14</td>
<td>14</td>
</tr>
</tbody>
</table>

\begin{align*}
\phi_{n1} &= .112 \text{ Mrad/s} \\
\phi_{n2} &= 4.03 \text{ Mrad/s} \\
\zeta_{1} &= 14 \\
\zeta_{2} &= 14
\end{align*}

16 combinations

### 32.0 GT/s CC 

<table>
<thead>
<tr>
<th>0.01 dB peaking</th>
<th>2.0 dB peaking</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.51 Mrad/s</td>
<td>5.42 Mrad/s</td>
</tr>
</tbody>
</table>
PCle 5.0 Reference Clock Phase Jitter

• PCIle 5.0 Limits Clock Phase Jitter to 150fs.

• Keysight to introduce a new method for calibrating out inherent scope noise for phase jitter measurements.

• Noise removal lowers phase noise floor of real-time scope to better than -145dBc/Hz.
PCle 5.0 32GT/s RX Calibration (BASE)

10 MV EYE HEIGHT POST EQ (0.3UI EYE WIDTH) TARGET

Optimal TX EQ, Diff Swing 720 – 800 mV

32.0 GT/s PRBS Generator

Constrained Impairments

Rj .5 ps RMS
Sj 1-5 ps
Small EW Adjust
Diff Interference 5-30 mv
CM Interference

Constrained Impairments

Calibration Channel 35-38 db TP1 – TP2
EH or EW Adjust

CEM Connector

Heavily dependent upon physical ISI channel

Test Equipment

Post Processing Scripts:
Rx pkg model
Behavioral CTLE/DFE
Behavioral CDR

10 mV / .3 UI at E-12 BER

NOTE Very tight eye height margin.
PCle 5.0 32GT/s RX Calibration (BASE)

TARGET TEST CHANNEL BOARD W/ NEW CEM SMT CONNECTOR

- PCIe 5.0 BASE RX Calibration Prototypes – 2.92mm with Meg6 (low loss material)
  - Available through PCISIG Electrical Work Group Members (limited qty)
  - Amphenol FCI CEM Connector
  - Connector layout optimized (sentry vias, merged grounds, side-band termination)
  - Microstrip differential traces
  - 85 Ohm Impedance
- Huber-Suhner SUCOFLEX 102_E 2.92mm Cables
PCIe 3.0 32GT/s Logical Phy

LTSSM AND CONFIGURATION CHANGES IN PCIE 5.0
PCle 5.0 32GT/s Phy Logical Update

- Option to bypass intermediate link equalization
- Option to skip link equalization entirely
- SRIS is mandatory for every PCle 5.0 phy
  - Architecturally only CC or SRIS/SRNS is implemented at the system level
- Loopback with Crosstalk
  - Also multi-lane loopback
- Precoding
- 32GT/s Capability Enhancements
- Support of Alternate Protocols (encapsulation)
• Some vendors report each speed transition takes 100 ms.
• Thus, 2.5->8->16->32GT/s = 300ms
  • Can it be done faster?
• What if endpoint is never expected to ever run at 8 or 16 GT/s?
Bypass Link Equalization

PROPOSAL TO BYPASS TO 32GT/S

- Optional to bypass LEQ
- No Errors
- LEQ for 8, 16GT/s is not performed
- 8 & 16GT/s data rates cannot be used.
- Only 2.5, 5, and 32GT/s are available.
- Controlled via TS1/TS2 in training control field.
Skip Link EQ Altogether

- Eliminates all Link EQ time
- Requires foreknowledge of optional link EQ settings for root port and endpoint
  - From a previous LinkEQ session
  - An independent characterization of the channel
- All components in the link chain must support it.
- All advertised data rates are available
- Controlled via TS1/TS2 in training control field.
SRIS Required for 32GT/s Capable PCIe 5.0 ICs

**Problem:**
- Routing Refclk requires considerable resources in some form factors
- Difficult to construct systems under today’s rules (SRIS is optional in 3.1/4.0)
- Lose backwards compatibility if SRIS was made mandatory for 3.1/4.0

**Solution**
- SRIS is mandatory for all 32.0 GT/s capable components
Loopback Enhancements for 32GT/s Capable PCIe 5.0 ICs

Problem:
- Currently, Loopback checks lane 0 only
- All other Lanes are quiet (EI)
- Cross-talk contributions significant to Rx Margin loss at 32.0 GT/s
- Would like to test closer to real conditions (other Lanes transmitting)
- Would like to test other Lanes aside from L0

Resolution
- Add the ability to equalize and run Loopback on any Lane
- Add Loopback/Equalization arcs
  - Avoids checking Lane # conditions
  - Avoids needing a legitimate configuration
- Other lanes transmit the Modified Compliance Pattern to mimic crosstalk
Precoding for 32GT/s Capable PCIe 5.0 ICs

**Problem:**
- 32.0 GT/s insertion loss target (-36dB) leads to a higher DFE tap ratio which, in turn, may trigger burst errors due to error propagation following a single bit error.
  - If a bit flips and the data is a 01010 pattern and there is a high DFE tap ratio, then the bit that flipped influences the DFE the wrong way, so it flips the next bit, which then influences the next bit, and so on… the problem corrects if bits did not alternate since the DFE would settle properly.
  - Burst errors can eventually break the CRC detection capability. They can also lead to SKP Ordered Set corruption (causing FIFO overflow).

**Resolution**
- Precode the data stream.
Selectable Precoding at 32GT/s

- Only scrambled symbols are precoded
- The RX requests TX to enable precoder.
  - The link partner’s receiver determines if precoding is to be used or not.
  - It is enabled via control bit in TS1/TS2
- SKPOS is modified to change AAh to 99h
Summary of new control bits

PCIE 5.0 CHANGES

• Capabilities Control Register
  • Bypass equalization supported/enabled
  • Skip equalization supported/enabled
  • Modified TS1/TS2 supported/selected
  • Precoding supported
• Status Register
  • Equalization phases successful
  • Modified TS/Bypass/Skip/Precoding status
• Rx/Tx Modified TS Data 1/2 register
  • Fields from the Modified TS1/TS2’s
• Lane Equalization Control Register
  • DSP/USP Transmitter Preset
Keysight Tools for PCI Express Gen5

TX TESTING AND RX TESTING

UXR Real Time Oscilloscope
- Bandwidth up to 110GHz
- ½ the noise floor of any prior oscilloscope

M8040A High Performance 64Gbaud BERT
- Data rates up to 64GBaud
- NRZ and PAM4 capable
- 4 tap de-emphasis
- Integrated Jitter injection
PCle 5.0 BW Requirements

HOW MUCH SCOPE BANDWIDTH FOR 32GT/S?
PCle 5.0 RX Calibration

TX VOLTAGE SWING AND DE-EMPHASIS P0-P9

M8040A JBERT

TX Voltage Swing and De-Emphasis Calibration Setup
PCle 5.0 RX Calibration

M8040A EDGE RATES AT 32GT/S MEASURED @ 80GHZ

M8040A JBERT w/ P4 (no de-emphasis)

80/20 P4 Rise-time at 80GHz BW

80/20 P7 Fall-time at 80GHz BW
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

25 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

32 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

40 GHz
PCle 5.0 RX Calibration

**P7 DE-EMPHASIS CALIBRATION**

45 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

50 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

55 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

60 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

80 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

100 GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

25GHz  32GHz  50GHz  60GHz
PCle 5.0 RX Calibration

P7 DE-EMPHASIS CALIBRATION

25GHz  32GHz  50GHz  60GHz

Keysight Recommendation with Z-Series
Keysight Recommendation with UXR
PCI Express 4.0 TX Testing

KEYSIGHT TOOLS FOR TRANSMITTER VALIDATION
PCI Express® 4.0 – Keysight Total Solution

Physical Layer – System Simulation
- ADS Design Software
- Compliance Test Bench
- N5393F PCI Express Electrical Compliance Software
- Complete System Simulation with the same compliance test used in the lab

Physical layer – interconnect design
- ADS design software
- 86100D DCA-X/TDR
- E5071C ENA option TDR
- Verify PCIe 4.0 Compliant Channels
- Verify Return Loss Compliance

Physical layer-transmitter test
- V-Series, Z-Series Real-Time Oscilloscopes
- N5393F PCI Express 4.0 TX Electrical compliance software
- DSA V-series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test
- M8020A J-BERT High Performance, Protocol Aware BERT
- N5990A automated compliance and device characterization test software
- Automated RX Test software
  - Accurate, Efficient
  - Comprehensive RX Testing

Keysight 2018
PCI Express 4.0 TX Measurement Test Setup

BASE SPEC

PCIe 4.0 ASIC/IC Custom Breakout Board

Keysight Z-Series Real Time Oscilloscope

S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB)

Low jitter clock source

Testboard

DUT

Breakout Channel

Replica Channel

TP1

TP2

PCle 4.0 ASIC/IC Custom Breakout Board

S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB)
N5393F Demonstration

PCIE 4.0 BASE SPEC TESTING
N5393F/G New Features

- Supports PCIe 4.0 BASE TX Testing at 2.5G, 5G, 8G and 16GT/s (v0.7 BASE)
- Supports PCIe 4.0 Reference Clock tests (2.5G, 5G, 8G, 16G)
- Supports U.2 (SFF-8639) CEM tests for endpoints and root complexes (2.5G, 5G, 8G).
- Automated DUT control using an 81150/60A Pulse Generator ARB.
- Enhanced Switch Matrix supporting arbitrary lane mapping
- New “Workshop Compliance Mode” for rapid PCISIG official compliance testing.
- Minimum oscilloscope BW: 25GHz
Keysight PCIe 4.0 (Gen4) TX N5393F Test Application

- New Test Plan Setup
- Select Standard Version to Test
- Select Speeds of Gen4 Device to Test
- Automatic DUT control for toggle signal
Keysight PCIe 4.0 (Gen4) TX N5393F Test Application
Keysight PCIe 4.0 (Gen4) TX N8816B Protocol Decode Software

- Supports all PCIe Speeds (16G, 8G, 5G, and 2.5G)
- Requires 25GHz for PCIe 4.0 Support
- N5461A Infiniium Serial Data Equalization (SDE) Software recommended for 16G decode.

### Ordering Information

<table>
<thead>
<tr>
<th>License Type</th>
<th>Infiniium Z-Series, V-Series, Q-Series, X-Series</th>
<th>Infiniium 90000 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Factory-Installed</td>
<td>DSOZ000-S28</td>
<td>DSOZ000-S28</td>
</tr>
<tr>
<td></td>
<td>DSOV000-S28</td>
<td>DSOV000-S28</td>
</tr>
<tr>
<td>User-Installed</td>
<td>N8816B-1FP</td>
<td>N8816B-1FP</td>
</tr>
<tr>
<td>Transportable</td>
<td>N8816B-1TP</td>
<td>N8816B-1TP</td>
</tr>
<tr>
<td>Floating</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Server Based</td>
<td></td>
<td>N543SA-134</td>
</tr>
</tbody>
</table>
PCle CEM Specific Information
CEM TX Test Setups

AIC and Motherboard Test Proposals

Add-in Card TX Test

- Real Time Scope (5dB package)
- Nominal 1.0 dB cable to scope
- Variable ISI Board (including cable) Nominal 10.3 dB trace
- 0.7 dB PCIe Connector
- 3.0 dB (3.0") CBB Tx trace

Motherboard TX Test

- Nominal 1.0 dB cable to scope
- CLB
- 2.0 dB (2.0") CLB Tx trace
- Variable ISI Board (including cable) Nominal 2.0 dB trace
- Real Time Scope (3dB package)

Note: This TX test proposal utilizes an external variable ISI board to ensure consistent insertion loss of the test setup.
CEM TX Test Setups

**PCle 4.0 (Add-in Card)**
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- 5dB package model embedded on scope
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- Waveforms post processed using SigTest
  - Time Domain CDR algorithm to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

---

**PCle 4.0 (System)**
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- 3dB package model embedded on scope
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- Waveforms post processed using SigTest
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
CEM TX Test Setup

- Cabling from CBB4 to ISI Channel
- Physical ISI Channel to achieve -17dB Compliance Toggle

DUT
CEM TX Test Setup

**CBB4 FIXTURE**

- **Toggle Button**
- **Toggle Circuit Output**
- **TX Output for DUT**
- **RX Lanes**
CEM TX Test Setups

CLB4 X4-X8 FIXTURE

- Toggle Button
- TX Output for X8
- TX Output for X4
- Toggle Circuit
CEM TX Test Setup

ISI FIXTURE

ISI Pairs
# CEM TX Test Setups

## AIC and Motherboard Test Channels

<table>
<thead>
<tr>
<th>Serial #</th>
<th>Configuration</th>
<th>Full Channel Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td>12</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td>22</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
</tbody>
</table>
## CEM TX Test Setups

### AIC and Motherboard Test Channels Loss Calculation

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>1</th>
<th>12</th>
<th>22</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Trace</td>
<td>1.27</td>
<td>1.09</td>
<td>1.2</td>
</tr>
<tr>
<td>Long Trace</td>
<td>11.84</td>
<td>11.8</td>
<td>11.73</td>
</tr>
<tr>
<td>Loss/inch</td>
<td>1.057</td>
<td>1.071</td>
<td>1.053</td>
</tr>
</tbody>
</table>

SMA Female to SMP Female Cable

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Coaxial Launch 2x</td>
<td>0.825</td>
<td>0.645</td>
<td>0.755</td>
</tr>
<tr>
<td>CBB Tx &lt;-&gt; CLB Rx</td>
<td>9.78</td>
<td>10.05</td>
<td>10.08</td>
</tr>
<tr>
<td>Mated CEM Connector Loss</td>
<td>1.111</td>
<td>1.463</td>
<td>1.509</td>
</tr>
</tbody>
</table>

CBB Tx Loss

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>4.6945</td>
<td>4.9985</td>
<td>5.0455</td>
</tr>
<tr>
<td>CLB Tx Loss</td>
<td>2.5265</td>
<td>2.4645</td>
</tr>
</tbody>
</table>

### AIC Tx

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CBB ISI (Desired)</td>
<td>10.3055</td>
<td>10.0015</td>
<td>9.9545</td>
</tr>
<tr>
<td>CBB ISI (Measured)</td>
<td>10.21</td>
<td>9.97</td>
<td>10.16</td>
</tr>
<tr>
<td>CBB ISI Pair</td>
<td>Pair 16</td>
<td>Pair 16</td>
<td>Pair 16</td>
</tr>
</tbody>
</table>

### System Tx

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CLB ISI (Desired)</td>
<td>2.4735</td>
<td>2.5355</td>
<td>2.5165</td>
</tr>
<tr>
<td>CLB ISI (Measured)</td>
<td>2.5</td>
<td>2.51</td>
<td>2.51</td>
</tr>
<tr>
<td>CLB ISI Pair</td>
<td>Pair 0</td>
<td>Pair 0</td>
<td>Pair 0</td>
</tr>
</tbody>
</table>
Keysight PCIe 4.0 (Gen4) TX N5393F Test Application
PCI-SIG Workshop 104 Gen4 TX Testing Suite
CEM RX Test Setup
RX AIC and Motherboard Test Channel loss calculation

<table>
<thead>
<tr>
<th>Serial #</th>
<th>Configuration</th>
<th>Full Channel Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>System (27dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 0 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
<td>Nominal 1.0 dB cable from signal generator</td>
</tr>
<tr>
<td>10</td>
<td>AIC (27dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 25 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
<tr>
<td>System (28dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 3 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
<td>Nominal 1.0 dB cable from signal generator</td>
</tr>
<tr>
<td>10</td>
<td>AIC (28dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 27 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
<tr>
<td>System (30dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 7 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
<td>Nominal 1.0 dB cable from signal generator</td>
</tr>
<tr>
<td>10</td>
<td>AIC (30dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 31 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
</tbody>
</table>
## CEM RX Test Setup
### AIC and Motherboard Test Channels Loss Calculation

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Trace</td>
<td>1.17</td>
<td>1.43</td>
<td>1.09</td>
</tr>
<tr>
<td>Long Trace</td>
<td>11.69</td>
<td>11.77</td>
<td>11.75</td>
</tr>
<tr>
<td>Loss/inch</td>
<td>1.052</td>
<td>1.034</td>
<td>1.066</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMA Female to SMP Female Cable</td>
<td>0.2225</td>
<td>0.2225</td>
<td>0.2225</td>
</tr>
<tr>
<td>Coaxial Launch 2x</td>
<td>0.725</td>
<td>0.985</td>
<td>0.645</td>
</tr>
<tr>
<td>CBB Tx &lt;-&gt; CLB Rx</td>
<td>9.69</td>
<td>10.32</td>
<td>9.71</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mated CEM Connector Loss</td>
<td>1.156</td>
<td>1.652</td>
<td>1.158</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBB Tx Loss</td>
<td>4.6745</td>
<td>5.2465</td>
<td>4.6785</td>
</tr>
<tr>
<td>CLB Tx Loss</td>
<td>2.4665</td>
<td>2.5605</td>
<td>2.4545</td>
</tr>
</tbody>
</table>

### System Rx CAL

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBB ISI (Desired)</td>
<td>10.3255</td>
<td>9.7535</td>
<td>10.3215</td>
</tr>
<tr>
<td>CBB ISI (Measured)</td>
<td>10.13</td>
<td>9.55</td>
<td>10.16</td>
</tr>
<tr>
<td>CBB ISI Pair</td>
<td>Pair 16</td>
<td>Pair 15</td>
<td>Pair 16</td>
</tr>
<tr>
<td>27dB (Measured)</td>
<td>21.87</td>
<td>21.87</td>
<td>22.14</td>
</tr>
<tr>
<td>27dB CLB ISI Pair</td>
<td>Pair 0</td>
<td>Pair 0</td>
<td>Pair 0</td>
</tr>
<tr>
<td>28dB (Measured)</td>
<td>23.17</td>
<td>23.28</td>
<td>23.01</td>
</tr>
<tr>
<td>28dB CLB ISI Pair</td>
<td>Pair 3</td>
<td>Pair 3</td>
<td>Pair 2</td>
</tr>
<tr>
<td>30dB (Measured)</td>
<td>25.11</td>
<td>25.15</td>
<td>25.05</td>
</tr>
<tr>
<td>30dB CLB ISI Pair</td>
<td>Pair 7</td>
<td>Pair 7</td>
<td>Pair 6</td>
</tr>
</tbody>
</table>

### AIC Rx CAL

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLB ISI (Desired)</td>
<td>2.5335</td>
<td>2.4395</td>
<td>2.5455</td>
</tr>
<tr>
<td>CLB ISI (Measured)</td>
<td>3</td>
<td>2.47</td>
<td>2.53</td>
</tr>
<tr>
<td>CLB ISI Pair</td>
<td>Pair 0</td>
<td>Pair 0</td>
<td>Pair 0</td>
</tr>
<tr>
<td>27dB (Measured)</td>
<td>24.25</td>
<td>24.2</td>
<td>24.32</td>
</tr>
<tr>
<td>27dB CLB ISI Pair</td>
<td>Pair 25</td>
<td>Pair 24</td>
<td>Pair 25</td>
</tr>
<tr>
<td>28dB (Measured)</td>
<td>25.16</td>
<td>25.26</td>
<td>25.25</td>
</tr>
<tr>
<td>28dB CLB ISI Pair</td>
<td>Pair 27</td>
<td>Pair 26</td>
<td>Pair 27</td>
</tr>
<tr>
<td>30dB (Measured)</td>
<td>26.9</td>
<td>26.94</td>
<td>27.18</td>
</tr>
<tr>
<td>30dB CLB ISI Pair</td>
<td>Pair 31</td>
<td>Pair 30</td>
<td>Pair 31</td>
</tr>
</tbody>
</table>
Workshop 104 Gen4 RX Testing Suite
PCIe 4.0 Cable and Adapter Recommendations

- **SMP to SMA (3.5mm) Cables**
  (Huber-Suhner PN: 80350960)

- **1 meter 3.5mm coaxial Cables**
  (Huber-Suhner PN: 85064115)

- **1 foot SMP Cables**
  (Huber-Suhner PN: 80345501)

- **SMP to SMA (3.5mm) Adaptors**
  (Huber-Suhner PN: 80350960)

- **Female to Female 3.5mm Adaptors**
  (Maury Microwave PN: CC-A-292-FF)
PCI Express M.2 Test TX and RX Testing
M.2 TX Test Setup

M.2 CLB Fixture

Toggle Button

M.2 connector

TX Output for DUT

RX Lanes
M.2 TX Test Setup

M.2 CLB3 FIXTURES

SMP connector
Toggle Button
Retention Detent
RX Lane 0
RX Lane 1
M.2 TX Test Setup

M.2 RX TEST CALIBRATION SETUP

Keysight V-Series RTS

Keysight M8020 16G JBERT

PCIe 4.0 ISI Board for optimal channel loss
PCI Express 4.0

16 GT/s Receiver Stress Signal Calibration Setup – Compliance Eye Calibration

- Channel determined by the channel calibration is applied
- DM-SI, SJ and $V_{\text{diff}}$ are adjusted to find correct combination for a compliant eye of the reference RX
PCI Express 4.0

Solution Summary

Test Solution:

- J-BERT M8020A new LTSSM with 16G support successfully used at PCIe compliance WS 101 for preliminary 16G RX and link EQ RX testing

- N5990A PCI 4.0 Test Automation with 16G base specification support available. CEM testing is in FYI testing still.

- Complete PCI Express RX test coverage through J-BERT M8020A and Infiniium V-, Z-Series DSA real-time scopes
PCle 5? PCle 4 isn’t even done yet!

**INDUSTRY DYNAMICS FORCE ACCELERATED SCHEDULE**

- Intel pushing schedule at an incredible pace
- Keysight was ahead of industry needs with tools for PCle Gen4
- PCle Gen5 tools are being developed as the spec evolves
- This creates exciting opportunities but also significant challenges…
PCI Express 5.0

37dB, 770mV launch, P8, 10mV DM-SI TP2P, 3.125ps SJ

- Calibrated PCIe 5 32G RX eye
- M8040A based stress signal generator
UXR Real Time Oscilloscope
- Bandwidth up to 110GHz
- ½ the noise floor of any prior oscilloscope

M8040A High Performance 64Gbaud BERT
- Data rates up to 64GBaud
- NRZ and PAM4 capable
- 4 tap de-emphasis
- Integrated Jitter injection

Keysight Tools for PCI Express Gen5
TX TESTING AND RX TESTING
PCI Express® 4.0 – Keysight Total Solution

Physical Layer – System Simulation
- ADS Design Software
- Compliance Test Bench
- N5393F PCI Express Electrical Compliance Software
- Complete System Simulation with the same compliance test used in the lab

Physical layer – interconnect design
- ADS design software
- 86100D DCA-X/TDR
- Verify PCIe 4.0 Compliant Channels
- Verify Return Loss Compliance

Physical layer-transmitter test
- V-Series, Z-Series Real-Time Oscilloscopes
- E5071C ENA option TDR
- N5393F PCI Express 4.0 TX Electrical compliance software
- DSA V-series & Z-Series Real-Time Oscilloscopes

Physical layer-receiver test
- M8020A J-BERT High Performance, Protocol Aware BERT
- N5990A automated compliance and device characterization test software
- Automated RX Test software
  - Accurate, Efficient
  - Comprehensive RX Testing
Infiniium HPS Scopes and M8000 Series of BER Test Solutions

MASTER YOUR NEXT PCIE DESIGN

Thank you!

More information:
www.keysight.com/find/M8000
www.keysight.com/find/M8040A
www.keysight/find/awg
www.keysight.com/find/pciexpress