Successfully negotiating the PCI EXPRESS® 2.0 Super Highway Towards Full Compliance

Agenda

• Introduction
• PCIe 2.0 changes from 1.0a/1.1 Spec
• 5GT/s Challenges
• Error Correction Techniques
• Test tool and fixture changes
• Agilent N5393B Compliance Application
• Additional Information Sources
PCI-SIG Compliance Testing

- Physical Layer
  - Validate Signal Quality of TX
- Configuration Space
  - Verify required fields and Values
- Link Layer & Transaction Layer
  - Exercise protocol and boundary layer conditions
- Platform Configuration
  - Validate BIOS correctly handling of PCI Express Devices
- Demonstrated Interop
  - Show that device drives load and device operates in actual PCI Express System

PHY Testing Goals for 2.0

Goals for PHY testing are unchanged
Achieving those goals is more challenging
Additional requirements added to increase confidence that designs are robust
Verify designs achieve critical specification targets
  - Jitter
  - Eye mask
  - Reference Clock
  - Voltage and Jitter margining
  - Receiver Margining

Predictor of interoperability
Changes Implemented under the 2.0 Specs

Changes to the PCIe Base Specification
- 5GT/s
- Different de-emphasis levels
- PLL bandwidth
- Backward compatibility

PCle Card Electromechanical (CEM) Specification Changes
- R̄j / D̄j tables and new jitter budgets
- Changes to Reference clock phase jitter specification
- 2 port measurement method for systems

Signal Level and BW

2.5G de-emphasis = -3.5 +/- 0.5
5G de-emphasis = -3.5 +/- 0.5 OR -6.0 +/- 0.5
Low swing voltage levels = no de-emphasis

BW dependant peaking requirements
- 3dB for 8 to 16M
- 1dB for 5 to 8M
- 2.5G same as 1.1
PLL Loop Bandwidth Testing

Equipment Required:
- Sine Wave Source (1GHz min)
- Spectrum Analyzer (3 GHz min)
- Microcircuits FTB-1-6 Balun
- Modified CBB

Steps:
- Sweep source 100-125MHz (-20dBm)
- SA: 35KHz Res BW, 40MHz Span, 2.5 GHz center
- Set display to peak hold
- Normalize response to note 3dB point

CEM Spec targets connector

Clarification of measurement location
Compared to 1.1
Chip + Interconnect
**5GT/s Jitter Challenges**

Jitter measurement more complex!

Jitter decomposition required

\[
\text{System } T_j = \sum D_j + 2Q_{BER} \sqrt{\sum R_j^2} \leq 1.0 \text{ UI}
\]

Speed dependant phase jitter filters

- 2.5G = 1 pole HPF
- 5G = step band pass filter

Error correction needed to measure TX at pins

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**Why New De-emphasis Levels**

<table>
<thead>
<tr>
<th>Speed</th>
<th>De-emphasis Level</th>
<th>Vp-p</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5G</td>
<td>-3.5dB</td>
<td>758mV</td>
</tr>
<tr>
<td>5G</td>
<td>-3.5dB</td>
<td>583mV</td>
</tr>
<tr>
<td>5G</td>
<td>-6dB</td>
<td>525mV</td>
</tr>
</tbody>
</table>
De-embedding

- New Transmitter base specification requirement
  “Measurements at 5.0 GT/s must de-embed the test fixture”
  “It is also acceptable to use a common test fixture and de-embed it for measurements at both 2.5 and 5.0 GT/s.”

- What does it mean to de-embed?
  “Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins.”

Error Correction Techniques

Pre-measurement operations  Post-measurement operations

- De-embedding the CLB/CBB
  - N5230A PNA-L Network Analyzer

- Calibrating the Scope
  - DSO91304 13GHz Oscilloscope
  - Skew Calibration
  - Probe Attenuation/offset
  - Channel Vertical Cal
  - Channel Trigger Cal
**Fixture Error Correction Techniques**

- **Most Accurate**
  - S-Parameter De-embedding
  - Line-Reflect-Match (LRM)
  - Thru-Reflect-Line (TRL)
  - Short-Open-Load-Thru (SOLT)

- **Easiest**
  - Normalization
  - Reference Plane Calibration
  - Port Rotation
  - Time Domain Gating

= Pre-measurement error correction
= Post-measurement error correction

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**SQ Test Tool Requirements – System Board**

Use of CLB 2.0
SMP to SMA adapter, phase matched SMA cables
Terminate all lanes except the lane under test
Measure transmitted clock and data waveforms simultaneously with high speed oscilloscope
Use compliance pattern
1M UI of data
Sample rate of 40GS/s (25ps)
Compute:
- eye diagram,
- Rj, Dj, Tj@10^-12 BER,
- average data rate,
- rise/fall time,
- mode toggle
Measure all lanes of all 5GT/s capable slots
System 2 port measurement

- Reference Clock
- SMP Test Points
- CLB G2 Test Fixture
- Diff Socket Probe
- SMP Lane Probe Points
- Motherboard PCIe slot

Test Tool and Fixture Changes

- 100Mhz RefClk
- 5GT/s -6dB PCIe Data

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Mar. 2008
Test Tool Requirements - AIC

Use of CBB 2.0
SMP for all lanes, phase matched SMA cables
Terminate all lanes except the lane under test
Measure transmitted waveform with high speed oscilloscope
Use compliance pattern
1M UI of data
Sample rate of no more than 25 ps
Compute:
  – eye diagram,
  – Rj, Dj, Tj@10^-12 BER,
  – average data rate,
  – rise/fall time,
  – mode toggle
Measure all lanes

What to Look for in PCI Express Compliance Automation

Key Requirements:
• 1M UI (single or multi-acquisition) automated data acquisition
• Batch run capability for greater testing coverage or quick spot checking
• Implement measurements that respect the PCIe Specification
• Automated tools should self-scale to ensure top accuracy for each measurement performed.
• Results must be consistent with PCI-SIG tools used at Compliance Workshops.
Test Results with the Agilent N5393B

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HTML based automatic report generator allows you to easily share test results.

Select the version to test

Select the test point

Logical Physical Layer testing

Link Training issues –

“I start link training but I cannot establish a link”

“I plugged my 1.1 card into a 2.0 system and it does not work, why?”

“I plugged my 2.0 card into a 1.1 system and it does not work”

“I pass electrical compliance but I still cannot link”

Although a card may successfully pass the electrical requirements, it may not be possible to link for other reasons.

This is critical for interoperability!
Logical Physical Layer testing

Some suggested reasons why a link may not successfully train –

Presence Detect:

- Are the PRSNT1# and PRSNT2# pins wired correctly on both the system slot and the add in card? Does the system support Hot-Plug?
- This is especially critical when the link width of the card and the mechanical and electrical link width of the slot do not match

Reference Clock:

- Are the reference clocks on both sides compatible?

Link Width:

- Does the link train to the desired width? Does it link in all required widths?

Reserved bits in Training Sequences:

- When the reserved bits are used in the TS1 and TS2 ordered sets (for example, Gen 2 uses some bits which were reserved in Gen 1), do the devices still train successfully?

Testing the reserved bits in Training Sequences

In the 1.1 base specification, there are several reserved bits in the TS1 ordered set. Some of these bits are now used in the 2.0 specification — mainly in relation to the speed change and capability, in the Data Rate Identifier field:

<table>
<thead>
<tr>
<th>1.1 Specification</th>
<th>2.0 Specification</th>
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<tbody>
<tr>
<td>Reserved Bit Values</td>
<td>Identified Values</td>
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<tr>
<td>0</td>
<td>Data Rate Identifier</td>
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<tr>
<td>1</td>
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<td>Data Rate Identifier</td>
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<td>31</td>
<td>Data Rate Identifier</td>
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Table 4-4: TS1 Ordered Set

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Description</th>
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<tbody>
<tr>
<td>0-7</td>
<td>Bit 0-7</td>
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<tr>
<td>8-15</td>
<td>Bit 8-15</td>
</tr>
<tr>
<td>16-23</td>
<td>Reserved Bits</td>
</tr>
<tr>
<td>24-31</td>
<td>Reserved Bits</td>
</tr>
</tbody>
</table>

- 0 = Reserved
- 1-7 = Bit values
- 8-15 = Reserved bits
- 16-31 = Reserved bits

In the 2.0 specification, the reserved bits are now used to indicate the speed change and capability.
Testing the reserved bits in Training Sequences

It has been observed that many cards built to the 1.1 specification do not in fact ignore the reserved bits when used by a 2.0 device. This can cause the link not to train and is a severe interoperability issue. The PCISIG has introduced an official test in the Link Layer test specification which ensures that devices can link when these reserved bits are used. This test can be done with the Agilent Gen 2 PTC card or any of the Agilent Gen 2 Exerciser products. Since official 1.1 testing will not change in the foreseeable future, this test can be run on 1.1 cards and is a very strong indicator whether the device will operate in a 2.0 system.

Link and Transaction Layer Testing for Gen 2 PCI-Express

Test descriptions are not changed for Gen 2 Link and Transaction Layer tests with the exception of the Reserved bits test—

1.1 devices:
- Testing to the 1.1 specification is still done on the Agilent E2969A PTC card

2.0 devices
- All Gen 2 devices will be tested at 2.5GT/s AND 5GT/s where appropriate
- Gen 2, 2.5G only devices will be tested using the Gen 2 PTC
Link Layer Testing – Test the data Link Layer

Link Layer tests are a subset of the compliance checklist – a cross section of tests which if the device is compliant would indicate a reasonable chance of interoperability.

Includes error checking, and dealing with Link stability problems

List of Link Layer and Transaction Layer Tests

- BadLCRC
- CorruptedDLLPs
- DuplicateTLPSeqNum
- LinkRetrainOnRetryFailNoAckNak
- LinkRetrainOnRetryFail
- ReXmitOnNak
- ReplayNumTest
- ReplayTLPOrder
- ReplayTimerTest
- RequestCompletion
- ReservedFieldsDLLPReceive
- UndefinedDLLPEncoding
- WrongSeqNumInAckDLLP

Example of Bad LCRC Behavior
Example of Link Retrain on Retry Fail

Transaction Layer Testing

Transaction Layer Testing includes checking advanced error reporting capabilities and also to check packets at the Transaction Layer.
New Challenges for Gen 2 – Speed Change!

Key features:

- Recovery state used for speed change from Gen 1 to Gen 2
- Specific tests available for testing the LTSSM
- Gen 2 capability is advertised in training sequences
- Example: What happens to a Gen 1 device if it sees Gen 2 advertised in training sequences? PCISIG are now running a test for this as FYI since it is a potential interoperability problem
- Gen 2 is backwards compatible with Gen 1

LTSSM Tests

- Recovery
  - Exerciser Initiates 5.0 GT/s Speed Change
  - DUT Initiates 5.0 GT/s Speed Change
  - Exerciser Initiates 2.5 GT/s Speed Change
  - DUT Initiates 2.5 GT/s Speed Change
  - Exerciser Initiates Transition to Recovery
  - Negotiated Data Rate Fails in Recovery.RcvrLock
  - Current Data Rate Fails in Recovery.RcvrLock
  - Exerciser Initiates Speed Change on Any Configured Lane
  - Force Transition from Recovery.RcvrLock to Configuration
  - Negotiated Data Rate Failed in Recovery.RcvrCfG
  - Current Data Rate Failed in Recovery.RcvrCfG
  - Force Transition from Recovery.RcvrLock to Detect
  - Force Transition from Recovery.RcvrCfG to Detect
  - Force Transition from Recovery.Idle to Detect
ASPM Testing

Challenges:
• Active State Power Management (ASPM) used to reduce power consumption in PCIE devices
• Many devices have problems going in and out of the electrical idle states L0s and L1.
• Windows Vista supports the low power states for medium power saving and high power saving modes
• The link is technically still active in these cases even although it is in Electrical idle.
• A Protocol Analyzer with fast locking time is required

Testing using N5309A Exerciser x16 for PCIe 5GT/s

A Gen2 Excerciser should have:
• Support for up to x16
• Usable form factor
• Compliance Test capabilities
• Error injection
• Stress testing
• Support LTSSM testing
• Power Management Test capabilities
For further information

<table>
<thead>
<tr>
<th>Website/Link</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><a href="http://www.agilent.com/find/pciexpress">www.agilent.com/find/pciexpress</a></td>
<td>Agilent tools to help you succeed with your PCI Express design such as the N5393B Compliance application.</td>
</tr>
<tr>
<td><a href="http://www.agilent.com/find/si">www.agilent.com/find/si</a></td>
<td>Agilent tools to help you master signal integrity challenges.</td>
</tr>
</tbody>
</table>