MOS Capacitor C-V Modeling Using IC-CAP

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- Approach to C-V Modeling
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- Summary
Metal-Oxide-Semiconductor: n-type MOS structure (p-type well)
MOS Capacitor Operation

Capacitance variation achieved by moving from the accumulation (max. C) to depletion/inversion (min. C) and Goal is to capture the changing capacitance by SPICE model in the simulation.

Charges under accumulation, depletion and inversion conditions.
Other Capacitors

**Polysilicon-Oxide-Metal (Poly-Metal)**
- Best possible capacitor for analog circuits
- Less parasitics
- Voltage independent

**Polysilicon-Oxide-Polysilicon (Poly-Poly)**

<table>
<thead>
<tr>
<th>Item</th>
<th>MOS Capacitor</th>
<th>Poly-Metal Capacitor</th>
<th>Poly-Poly Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tolerance</td>
<td>± 20%</td>
<td>± 10%</td>
<td>± 10%</td>
</tr>
<tr>
<td>TCC [ppm/°C]</td>
<td>50 ~ 100</td>
<td>20 ~ 50</td>
<td>10 ~ 30</td>
</tr>
<tr>
<td>VCC [ppm/ V]</td>
<td>50 ~ 200</td>
<td>10 ~ 100</td>
<td>5 ~ 50</td>
</tr>
<tr>
<td>Parasitic Cap.</td>
<td>Large</td>
<td>Small</td>
<td>Small</td>
</tr>
</tbody>
</table>
Approach to C-V Modeling

- **Polynomial Function in SPICE Built-in Capacitor Model**

  If the polynomial coefficients vector (coeffs=[c1 c2 ...]) is specified, the capacitor is nonlinear and the capacitance is

  \[ C(V) = C_{\text{inst}}(1 + c_1 V + c_2 V^2 + ...) \]

  The model example is

  ```
  model cog1s capacitor
  + tc1=1.145e-4          tc2=-2.494e-7
  + coeffs=[(1.13e-4+1.85e-5*(2*(l+w)/(l*w*1e6))) -1.77e-5  2.90e-7  6.09e-8]
  ```

- **PWL(Piecewise Linear) Method**

  PWL method is a subset in VCCS(Voltage Controlled Current Source) dependent source of SPICE simulator and we can define two dimensional C-V coordinates for C-V curves.

  ```
  COG1S ( plus minus plus minus ) vccs type=vccap scale=(w*l*ca+2*(w+l)*cb) tc1=1.450e-04 tc2=-2.494e-07
  + pwl=[ -10 1.1777E+00
         -9.9 1.1774E+00
         -9.8 1.1755E+00
         -9.7 1.1756E+00
         -9.6 1.1770E+00
         -9.5 1.1771E+00
  ```

  The step size could be adjustable in order to avoid the convergence problem.
Approach to C-V Modeling (Cont.)

- Numerical Formula from the Charge Conservation Analysis (VerilogA Model)

\[
\begin{align*}
\dot{q}(v) &= \int_0^v C(v)dv \\
\dot{i}(t) &= \frac{d(Cv(t))}{dt} \\
\dot{i}(t) &= C \frac{dv(t)}{dt}
\end{align*}
\]

Charge conservation becomes worse if \( C \) is replaced with \( C(v) \) and also if \( C \) is a strong function of \( v \) and \( v \) varies significantly with \( t \).

Capacitance is the derivative of charge with respect to voltage. Thus, the charge \( q \) is simply the integral of the capacitance \( C \) with respect to the voltage \( v \). Using this is both accurate and computationally efficient and also in the aspect of charge conservation problem.

```
`include "discipline.vams"
module varactor(p, n);
inout p, n;
electrical p, n;
parameter real c0 = 1p from (0:inf); // nominal capacitance (F)
parameter real c1 = 0.5p from [0:c0); // maximum capacitance change from
nominal (F)
parameter real v0 = 0; // voltage for nominal capacitance (V)
parameter real v1 = 1 from (0:inf); // voltage change for maximum capacitance (V)
real q, v;
analog begin
v = V(p,n);
q = c0*v + c1*v1*ln(cosh((v - v0)/v1));
i(p, n) <= ddt(q);
end
endmodule```

**Equivalent Circuit**

- Use intrinsic part model parameters in PROVEN BSIM3v3 capacitance model
- Cgg mode topology of MOSFET
- Higher Rs/Rd far from physics to invite Cgb mode
- Parasitic resistors for temp. modeling
- Model covers
  - accumulation, depletion and inversion regions
  - hot/cold temp variations
  - multiple geometries
IC-CAP Configuration

- **DUTs-Setups**

  DUT Parameters are important for the modeling of geometry scaling.

  Setup Variable is also important for the modeling of temperature variation.
**MULTI PLOT**

Useful in the interactive optimization
### Sub-Circuit Model for HSPICE

```verbatim
.subckt MOSCAP 1=PLUS 2=MINUS
# echo .param tcv1=$mpar(tcv1=-263.3m) tcv2=$mpar(tcv2=1.143m)
# echo mcap 3 4 3 3 mosmod w=$dpar(MOSCAP.w=320u) l=$dpar(MOSCAP.l=320u)  geometry information to netlist
rgate 1 4 r=10 tc1=1.2e-3 tc2=3.6e-6
rwell 3 2 r=0.02 tc1=1.2e-2 tc2=3.6e-5

.model mosmod nmos level=49
+ version=3.3 paramchk=1 tref=25
+ tox=5.647e-08 nch=2.476e+16 nsub=6e+16
+ vth0=1.0729 k1=1.50723 acde=1.425
+ moin=15 noff=1
+ dwc=5.164e-07 dlc=8.015e-07
cdsc=0 cdscb=0 cdscd=0
+ is=1e-18 js=0 jsw=0
cj=1e-15 cjsw=0
+ cgdo=1e-15 cgso=1e-15 cgbo=0
+ rs=1e+10 rd=1e+10
+ kt1=0.3131 kt2=0.022
# echo + voffcv=('(tcv2*temper*temper+tcv1*temper+13.16)'
# echo is used to transfer statement to SPICE simulator without considering the syntax conflict by IC-CAP parser.
.ends
```

- **process parameters**
  - to eliminate unnecessary current/capacitance for the equation and also to aid the convergence
  - parasitic drain/source resistance
  - temp. modeling for threshold voltage
  - temp. modeling for inversion region

- **temp. modeling for inversion region**
- **temp. modeling for threshold voltage**

- **geometry information to netlist**
- **# echo** is used to transfer statement to SPICE simulator without considering the syntax conflict by IC-CAP parser.
Link HSPICE for Piped Simulation

IC-CAP Reference Manual

Prior to IC-CAP 2006B Addon3, IC-CAP did not support the CANPIPE token for HSPICE in usersimulators. This token may now be used on local Linux and local Solaris HSPICE simulations with Hspice-2007.03-SP1. It is not a true piped mode (netlists and raw files are still written to disk), but provides substantial performance improvement by using an interactive mode that avoids restarting HSPICE for every simulation.

In general, piped simulations are faster than non-piped simulations for any given simulator because the simulator process does not have to be restarted for every simulation and less file activity is required.

Configuration in usersimulators file

```
hspace hspice /home/synopsys/B-2008.09-SP1/hspice/bin/hspice "device" CANPIPE
```

Great improvement on the optimization

HSPICE simulation speed is dramatically improved by the piped simulation mode and therefore it results great time saving during the device modeling. The improvement is above 10X, approximately.
- Demo. for Piped and Non-Piped Optimization

<Piped Simulation>

<Non-Piped Simulation>
# Model Parameters in BSIM3v3 Capacitance Models

<table>
<thead>
<tr>
<th>Name</th>
<th>Function</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>version</td>
<td>Model version selector</td>
<td>3.3</td>
</tr>
<tr>
<td>capmod</td>
<td>Capacitance model selector</td>
<td>capmod=2, Intrinsic charge model</td>
</tr>
<tr>
<td>vth0</td>
<td>Threshold voltage at zero body bias for long channel devices</td>
<td>It’s not matched with MOS if different substrate concentration.</td>
</tr>
<tr>
<td>kt1</td>
<td>Temperature coefficient for threshold voltage</td>
<td></td>
</tr>
<tr>
<td>tox</td>
<td>Oxide thickness</td>
<td>Refer to the manufactured values</td>
</tr>
<tr>
<td>nch</td>
<td>Peak channel doping concentration</td>
<td></td>
</tr>
<tr>
<td>k1</td>
<td>Body-effect coefficient</td>
<td>It’s not matched with MOS if different substrate concentration.</td>
</tr>
<tr>
<td>acde</td>
<td>Exponential coefficient for XDC for accumulation and depletion regions</td>
<td>From the charge thickness cap. model</td>
</tr>
<tr>
<td>moin</td>
<td>Coefficient for the surface potential</td>
<td>From the charge thickness cap. model</td>
</tr>
<tr>
<td>noff</td>
<td>CV parameter in $V_{gsteff,CV}$ for weak to strong inversion</td>
<td>Better transition above subthreshold region</td>
</tr>
<tr>
<td>voffcv</td>
<td>CV parameter in $V_{gsteff,CV}$ for weak to strong inversion</td>
<td>Better transition above subthreshold region</td>
</tr>
<tr>
<td>DWC</td>
<td>Long channel gate capacitance width offset</td>
<td>Same to $w_{int}$</td>
</tr>
<tr>
<td>DLC</td>
<td>Long channel gate capacitance length offset</td>
<td>Same to $l_{int}$</td>
</tr>
</tbody>
</table>
Parameter Extraction

tox, acde

dwc, dlc, rgate, rwell

vth0, nch, kt1

k1, moin, noff, voffcv(tcv1,tcv2)
Modeling Results

RMS error under 3%

< Scaling Modeling for Multiple Geometries >

< Temp. Modeling >
Model Verification

- Cadence PDK (Process Design Kit) environment with Spectre simulator.
- Use Calculator in order to plot C-V curve.

\[
C = \left| \frac{\text{imag}(I_{ac})}{2 \cdot \pi \cdot f \cdot V_{ac}} \right|
\]

- Use getAsciiWave to overlay the measured raw data onto the simulation curve. It's a function of Calculator.
Transient analysis is useful to verify the charging/discharging characteristic.

- Could detect abnormal non-linearity at hot temperatures during the discharging.
Circuit Correlation

- Correlation results show a reasonable and better improvement.
- The simulation was more closed to the measurement.
- Another correlation on Short Pulse Generate circuit, we got the same oscillation frequency to the measurement when we adopt the C-V model.

<table>
<thead>
<tr>
<th>Vcc=5V, Circuit=MV_DELAY2</th>
<th>Turn-On Delay (ns)</th>
<th>Turn-Off Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>mea sim error</td>
<td>mea sim error</td>
</tr>
<tr>
<td></td>
<td>Old Model New Model</td>
<td>Old Model New Model</td>
</tr>
<tr>
<td>#1</td>
<td>363.2 379.6 -4.5% 372.2 -2.5%</td>
<td>435.6 454.0 -4.2% 444.2 -2.0%</td>
</tr>
<tr>
<td>#2</td>
<td>361.9 379.6 -4.9% 372.2 -2.8%</td>
<td>441.5 454.0 -2.8% 444.2 -0.6%</td>
</tr>
</tbody>
</table>

< Correlation Results with Medium Voltage Delay Circuit >
We have successfully accomplished the modeling for C-V characteristic in terms of not only various sizes but also cold and hot temperatures.

We found out it’s useful for fitting MOS capacitor in terms of bias voltage.

The proposed macro model will overcome convergence/scaling issues because it adopted the proven compact model and also it resulted good correlation between the simulation and measurement for the analog delay circuit.

In IC-CAP, the multiple plot function, sub-circuit modeling environment and the piped simulation mode are accelerating to increase modeling productivity.

* Acknowledgement
  ➢ Appreciate Hyeongwoo Jang in Fairchild Korea and Heesuk Shin in Agilent Korea
Reference

[1] Department of Electrical Engineering and Computer Sciences
    University of California, Berkeley, "BSIM3v3.2.2 MOSFET Model Users’
    Manual", CHAPTER 4: Capacitance Modeling, p.69

