UWB Receiver Frontend Design with ADS

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Outline

• Introduction to IHP

• Motivation

• Impulse Radio Receiver Architectures

• Receiver Components Design

• Measurements

• Conclusion
Introduction to IHP: Facts & Figures

• German Research Institute
  Member of the Leibniz Association

• Located in Frankfurt (Oder) / Germany

• Founded 1983 / re-founded 1991
  Experience in silicon technology since the 1970th
  Pioneered SiGe:C technology in the 90’s

• About 220 employees from >20 countries

• Budget 28 Mio €
  Operating costs & investments
Introduction to IHP: Facts & Figures

1 h to Berlin

8" Pilot Line
Introduction to IHP: Vertical R&D Approach

Vertical approach = R&D spans microelectronic technology chain

Enables forward-looking application-oriented research

Focus on Si-based Technology

New Systems & Digital Circuits
- UWB
- 1Gb/s wireless
- radar sensor
- mobile appl.
- sensor networks

New Analog & HF - Circuits

Technologies / new embedded modules
- high k MIM
- piezo filter
- HBT
- 250/130nm CMOS
- p/n LDMOS
- NVM/DRAM/SRAM

New Materials
- Si
- SiGe
- high k
- piezo

Departments (# staff)
- System Design (40)
- Circuit Design (25)
- Technology (43)
- Pilot Line (60)
- Materials (9+5 ext.)

Introduction to IHP: Vertical R&D Approach
Motivation

• To reveal Agilent ADS Software capabilities for the design of the integrated circuits.

Impulse Radio UWB Receiver is chosen as an example.
Impulse Radio Receiver Architectures

• Impulse Detection Principles

**Non-coherent detection**

- Squaring the input signal
- Auto-Correlation
- Loosing phase information
- Easier to implement

**Coherent detection**

- Multiplication with template
- Cross-Correlation
- Phase detection (signal vs. template)
- Template generation required
Impulse Radio Receiver Architectures

- Placement of the squaring element (multiplier)

**Between LNA and VGA**

- Multiplier: full dynamic range
- Gain depends on input signal
- VGA operates on BB freq.
- DC offset issue

**After LNA and VGA**

- Multiplier: const. input level
- Gain almost independent
- VGA operates on RF freq.
- Stability issue
Impulse Radio Receiver Architectures

- Non-coherent Receiver
Receiver Components Design

• Simulation Techniques

AC Analysis

SP Analysis

Transient Analysis

Harmonic Balance Analysis
Receiver Components Design

- Passive Balun and Low Noise Amplifier

![Circuit Diagram](image)

- Passive Block
- Active Block

Lna_in → Passive Balun → LNA
Receiver Components Design

- Layout done in ADS: Passive Balun and Low Noise Amplifier

Open points concerning Layouting in ADS:
  - Easier to use GUI for layout drawing
  - DesignKit: User friendly device pins, update DRC rules
Receiver Components Design

- Passive Balun

![Diagram of Passive Balun and S-Parameters](image)
## Receiver Components Design

- **Investigating DC characteristic**

### DC Power Consumption versus Bias

![Graph showing DC power consumption versus bias](image_url)

**Move Marker m1 to update values below:**

<table>
<thead>
<tr>
<th>VCE</th>
<th>DC_power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.448</td>
<td>0.001</td>
</tr>
</tbody>
</table>

**Device Power Consumption at m1 bias point, Watts**

- VCE: 1.448
- DC_power: 0.001
Receiver Components Design

- **Investigating AC characteristic**

![AC characteristic graph]

- **SP_BJT**
  - **X1**
  - **IBB_start** = 2 uA
  - **IBB_stop** = 30 uA
  - **IBB_points** = 10
  - **VCE_start** = 0
  - **VCE_stop** = 1.5
  - **VCE_points** = 30
  - **AnalysisFreq** = 7.7 GHz
  - **Port1Z** = 50
  - **Port2Z** = 50

- **Forward Transmission, dB**
  - **m1**
  - **m2**

- **Device Power Consumption, Watts**
  - **VCE**
  - **IC.i[0]**
  - **X1.IBB**

Values at bias point indicated by marker **m1**. Move marker to update.
Receiver Components Design

- **Low Noise Amplifier**

  - **S-Parameters**
    - **S_Param**
      - Start=0.05 GHz
      - Stop=10.0 GHz
      - Step=0.05 GHz

  - **Parameter Sweep**
    - **ParamSweep**
      - **Sweep1**
        - **SweepVar="Cin"**
        - **SimInstanceName[1]="SP1"**
        - **SimInstanceName[2]=**
        - **SimInstanceName[3]=**
        - **SimInstanceName[4]=**
        - **SimInstanceName[5]=**
        - **SimInstanceName[6]=**
        - **Start=0.1**
        - **Stop=1**
        - **Step=0.1**

  - **Inductors**
    - **Linput=1.0**
    - **Kin=1.0**
    - **Lground=0.5**
    - **Kg=1.0**

  - **LNA Design**
    - **V_DC SRC1**
    - **Vdc=2.5V**
    - **L_Probe iSupply**
    - **Supply**
    - **LNA**
    - **X3**
      - **VAR VAR1**
      - **Cin=Cin**
      - **Cin=0.5**

  - **dB(S(2,1))**
    - **m5 freq=7.70GHz**
    - **nf(2)=4.708**
    - **m6 freq=7.25GHz**
    - **dB(S(2,1))=13.441 Peak**

  - **dB(S(1,1))**
    - **m1 freq=5.60GHz**
    - **dB(S(1,1))=-23.000 Cin=1.000000**
    - **m4 freq=8.000GHz**
    - **dB(S(1,1))=-13.946 Cin=0.400000**
Receiver Components Design

- Low Noise Amplifier

\[
\text{Eqn: } \begin{align*}
\text{Pin}_W & \text{dBm} = 10 \times \log(\text{Pin}_W) + 30 \\
\text{Pout}_W & \text{dBm} = 10 \times \log(\text{Pout}_W1) + 30
\end{align*}
\]

\[
\text{Gain} = \text{Pout}_W \text{dBm} - \text{Pin}_W \text{dBm}
\]

Output Power

Gain

Output Power vs Pin

\[\text{Pin} \text{dBm} = 10 \times \log(\text{Pin}) + 30\]

\[\text{Gain} = \text{Pout} \text{dBm} - \text{Pin} \text{dBm}\]

\[\text{Output Power} = \text{Pout} \text{dBm}\]
Receiver Components Design

- Variable Gain Amplifier (VGA)

![Variable Gain Amplifier (VGA)](image)

- Gain:
  - **m1**: Pin=20.500, Gain=12.405
  - **m2**: Pin=20.500, Gain=12.405
  - **m4**: Pin=20.500, Pout_dBm=-8.095
Receiver Components Design

- Multiplier
Receiver Components Design

• Low-Pass Filter (LPF)
  Differential 4th order Bessel Filter
Receiver Components Design

- **Low-Pass Filter (LPF)**
  - Differential 4\(^{th}\) order Bessel Filter

![LPF Diagram]

- \( R_{in} = 100 \text{ Ohm} \)
- \( L1 = 11.76 \text{ nH} \)
- \( L2 = 2.537 \text{ nH} \)
- \( L3 = 11.76 \text{ nH} \)
- \( L4 = 2.537 \text{ nH} \)
- \( C1 = 4.87 \text{ pF} \)
- \( C2 = 1.462 \text{ pF} \)
- \( R_{OUT} = 100 \text{ Ohm} \)

- \( m1 \):
  - \( \text{freq} = 760.0 \text{ MHz} \)
  - \( \text{dB}(S(2,1)) = -3.003 \)
Receiver Components Design

• Low-Pass Filter (LPF)
  Differential 7th order Bessel Filter

LPF layout. 700x500 um²
Receiver Components Design

- Low-Pass Filter (LPF)
  Differential 7\(^{th}\) order Bessel Filter
Receiver Components Design

- Low-Pass Filter (LPF)
  Differential 7th order Bessel Filter

LPF reflection coefficients. Simulation and measurements.

LPF layout. 700x500 um²
Receiver Components Design

- Low-Pass Filter (LPF)
  Differential 7th order Bessel Filter

Group delay of the LPF. Red is ideal components; green is inductors as S-parameters; blue is measured results.
Receiver Components Design

- Receiver Time Domain Simulation
Receiver Components Design

• Receiver Time Domain Simulation
Measurements

- **Non-coherent Receiver**
  
  Fabricated in IHP 0.25 µm SiGe:C BiCMOS technology

- **Key Specifications**
  
  - **Chip size [mm²]**: 2.5 x 1.5
  - **Operation frequency**: 7.68 GHz
  - **Maximum gain**: 55.6 dB
  - **Dynamic range**: 41 dB
  - **Noise figure**: 4.6 dB
  - **Power consumption**: 242 mW
Measurements

- Board Design
Conclusion

• Agilent ADS Software is powerful, easy in use and very flexible tool for the design of the integrated circuit components.

• Layout drawing and verification is possible, but needs layout improvements to fully address the SiGe IC challenges.