Introduction to EMI/EMC Challenges and Their Solution

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Current Solution

Put on a bandaid to stop the **Bleeding** (radiation..)

- Not optimal
- Does not always work
- Costly

Copper band-aid

R4N Suppressor band-aid
Complexity of EMI problem

I/Os can inject Common-mode Noise Or
Power-pins inject Noise into PDN
Badly routed traces generate EMI
High-speed connectors and cables *amplify* the EMI problems

**Minimize IC, PKG, and PCB EMI to Reduce Overall System EMI**

*From EM-Scan Measurement of GPU Board*
Mechanism of Noise Propagation

(1) Conductive Noise

Noise Source

(2) Radiation Noise

Equipment or device exposed to noise

(3) Conductive Noise

Noise Source

Radiation Noise

Equipment or device exposed to noise

(4) Radiation Noise

Noise Source

Equipment or device exposed to noise
Different types of Emission

- Trace-Emission
  - I/O-Buffers Injecting Signal

- GND Return-currents & Slots

- Power-Pins Injecting Noise

- Common-Mode noise travelling through Connectors
Introducing the concept of “Virtual-EMI Lab”

*Full-wave EM Simulation, What-if Analysis, Root-cause debugging

**Measurements to Isolate the problem and Correlate with Simulation
Radiated-emission on packages due to return-path-discontinuity
DDR3 Package Modeling using MOM DC to 20GHz
Data- (DQ-) nets major referencing to GND
Routing of DQ signals from Die-Bumps-Top to Layer-3 running as Symmetric-SL sandwiched between GND on Layers 2 & 4

DQ signals on Layer-3 as Symmetric-SL

DQ signals @ Die-Bumps
Moving from Layer-3 to Layer-6 through Signal-PTH to pickup the Balls

DQ signals on Layer-6 routed between GND on layers 5

DQ signals on Layer-3
Impact of GND-PTH stitching: Proximity & #

Original-Package:
With 15-GND-PTH

Cost-Reduced-Package:
with 3-GND-PTH
Comparison of Return-current on GND-L4

Original-Package: With 15-GND-PTH

Cost-Reduced-Package: With 3-GND-PTH

Larger NEXT by 10dB
Comparison of eye-diagram @ 1.33GBps

Original-Package:
With 15-GND-PTH

Cost-Reduced-Package:
With 3-GND-PTH

40ps loss of margin

+95ps worst Setup-Margin

+55ps worst Setup-Margin
PKG-Antenna-Parameters Comparison of 15-GND-PTH compared to 3-GND-PTH

Maximum Intensity: 5u-watts/Steradian → 40-uwatts/Steradian (8X)

Angle of U-max: 160-degrees vs. 140-degrees

Antenna-Gain
-19dB → -11dB (+8dB)

Radiated-Power
40-uWatts → 220-uWatts (6x)
Trade-off Low-cost & Performance

Reducing # of GND-Stitches $\rightarrow$ Medium-2-low-risk for 1.33GB/s operation with $+55\text{ps}$ worst-case Setup-margin but with $+8\text{dB}$ Antenna-Gain

Most probably we need to **Turn-ON Spread spectrum**.

What is the cost of PLL vs. Reduction of GND-Stitch?
Trace Emission on PCBs due to cost-reduction
Low-Layer count PCB

CASE: 1
Memory emission from MA/CMD lanes
Problem:
Investigate Emission problem at 1.25 times the memory clock frequency (1.623 GHz)

Notes:
Address/Command Nets are routed on bottom-layer
Referencing power plane (due to lack of real-estate)
EMI Simulation Methodology

Step-1: Simulate and Visualize Current-density plot*

Method-of-Moments (Momentum) Simulations showing current-density plots and hot-spot regions on the PCB

Emscan Measurements

*Using Agilent Momentum Field Solver

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Step-2: Isolate Problem
Observe hot-spot area closely, and identify root-cause

Root-cause:
There is small $\lambda/8$ power-plane patch that is radiating like patch-antenna

Use the Momentum-uwave EM-engine with Antenna-Gain parameter to measure the merit of the PCB as non-intended antenna

Develop EMI guidelines along with SI/PI Guidelines using Antenna-Gain Parameter to compare Layout guidelines
What is the remedy?

Instead of REF MA/CMD to a VddQ Patch on Bottom layer continue routing on Bottom Layer 3m Chamber at least 16dB Improvement
Trace Emission on PCBs due to cost-reduction
Low-Layer count PCB

CASE:2
TMDS Emissions
Problem Statement

TMDS Emission @ 770MHz on 4-layer PCB & Coupling to Neighbor Ethernet-Card
Which one is better

Copper band-aid

R4N Suppressor band-aid

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Metal-Shield Mounted on Bottom of the Card

No Major Change of Radiation Field
Total Power increased slightly 27uWatts
Max Radiation @ Bottom of PCB (157/161)
Intensity increased slightly: 6uWatts/Steradian
Antenna-Gain -47dB (**worse**)
NEC-TOKIN R4N EMI-Suppression Material

Major improvement of Radiation field from bottom of PCB:
Total PWR dropped to 13uWatts (50%)
Antenna-Gain dropped to -51.5dB (~3dB)
Intensity dropped to 2uWatts/Steradian (60%)

R4N Material placed on Bottom of the PCB
Is it E-coupling or H-coupling?

Solution:
Simulation shows that suppression material is improving EMI emission, whereas, metallic shield is making it worse

Choose Suppression material over metallic shield -> Improve both cost and performance 😊

*Lab data confirms simulation results
Near-field scan results

R4N Suppressor band-aid

Emscan measurements
Far-field scanning in 10m chamber
Far-field Radiation of Ferrite Suppressors

Original No-Ferrite

R4N Suppression
What is the Remedy?

Sometimes it is cheaper to dampen the receiver not Emitter because adding R4N suppression materials is more cost than using RJ45 shielded connector on the Ethernet-card.

Selected to change RJ45 Connector on Ethernet-card to shielded one to suppress the receiver
PCB Edge Emission due to Power delivery Noise
Simulation Challenges in EMI

- System level (source, coupling path, unintentional antenna)
- Full wave simulation is often needed
- Time and memory consuming
Combining Measured Icc(t) with FDTD simulations to study the critical on-board-decaps under the GPU

Power Delivery Network

Current Probe @ VddQ pins

Drivers  Channel  Receivers

• SSO current is obtained by a combined simulation of the power delivery network model and the memory IO channel model
Measured Dynamic-current profile \( I_{cc}(t) \)

- Time-domain noise pattern directly imported into FDTD solver

Steady-state frequencies: 0.5 GHz, 1.0 GHz
Importing PCB layout of the Memory Channel

Stackup

- Signal
- Ground
- Signal
- VDD
- Ground
- VDD

Board thickness: 1.57mm
SSO Noise Source on Top Layer
Decaps on Bottom Layer
Far-Field Radiation

at 0.5 GHz

at 1.0 GHz

Reduction of 3-4 dB
Current Density

At 0.5 GHz

With Decaps  Without Decaps

At 0.5 GHz

Anticipate  Accelerate  Achieve
What is the benefit of PCB decaps?

New method to optimize the PCB decaps:

1. Measure or simulate the Dynamic-current profile $I_{cc}(t)$ @ the VddQ-pins with maximum activity on the memory-channel

2. Import the $I_{cc}(t)$ into FDTD (wide-band-phenomena)

3. Study the critical PCB decaps to mitigate the SSO noise emission
Board + Connector + Mate
Combining CAD and Board Files

Precise landing of connector fingers on board signal pad
Near-Field Radiation:

Do we need **Shielded Connector**? ($0.15 more cost)
Do we need **copper-tape** under connector?

- Simulated with FDTD-solver (Agilent EMPro)
- Accelerated on GPU system
- Simulation time $\approx \frac{1}{2}$ day with 1-GPU card and 2-hrs with 3-GPU cards

Study if improved grounding & shielding of the connector improves EMI behavior.
Improved Grounding of the Connector:
What is the impact of a copper-tape under the connector

No copper tape

Extra copper tape
Improved Grounding: Far-field impact of CU-tape

Reduction of 5 dB for EMI emission
In direction of chassis
Conclusion

“Virtual-EMI” Lab is a MUST for Speed-of-Light Product-to-Market

Radiated/Conducted-Emission:

Packages Return-Path Discontinuity driving the need to turn ON SS

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