Large-signal FET Model with Multiple Time Scale Dynamics from Nonlinear Vector Network Analyzer Data

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Abstract — A non-quasi static large-signal FET model is presented incorporating self-heating and other multiple timescale dynamics necessary to describe the large-signal behavior of III-V FET technologies including GaAs and GaN. The model is unique in that it incorporates electro-thermal and trapping dynamics (gate lag and drain lag) into both the model current source and the model nonlinear output charge source, for the first time. The model is developed from large-signal waveform data obtained from a modern nonlinear vector network analyzer (NVNA), working in concert with an output tuner and bias supplies. The dependencies of $I_G$ and $Q_d$ on temperature, two trap states, and instantaneous terminal voltages are identified directly from NVNA data. Artificial neural networks are used to represent these constitutive relations for a compiled implementation into a commercial nonlinear circuit simulator (Agilent ADS). Detailed comparisons to large-signal measured data are presented.

Index Terms — Semiconductor device modeling, Microwave FETs, Neural networks, Nonlinear Vector Network Analyzer.

I. INTRODUCTION

The need to incorporate nonlinear dynamic effects into large-signal FET models has been demonstrated at length by multiple authors [1-3]. Signatures of these effects include frequency dispersion of small-signal characteristics, slow transient effects in response to pulsed gate or drain voltages, and “knee walkout” or power degradation under large-signal steady-state conditions. Some degree of frequency dispersion due to self-heating is common to all transistors, while “gate lag” and “drain lag” can be particularly significant in modern III-V FET technologies such as GaAs and GaN.

Modeling these effects requires the identification and self-consistent coupling of slowly varying dynamical variables, such as temperature, slow emission of traps, and rapidly varying dynamical variables such as the instantaneous intrinsic terminal voltages and fast capture processes.

This paper presents a non-quasi static large-signal FET model incorporating self-heating and other multiple timescale dynamics related to trapping. It is developed using a general measurement-based modeling infrastructure for exciting the relevant dynamical behavior, identifying the constitutive relations defined on the combined set of terminal and auxiliary variables, and implementing the model into a commercial nonlinear simulator. The particular FET model described here is developed from large-signal waveform data obtained from a nonlinear vector network analyzer (NVNA) [7], working in concert with an output tuner (and synthetically defined loads using the dual-source NVNA) and bias supplies. The model nonlinear constitutive relations are identified using artificial neural networks (ANN) [4] trained on datasets where temperature and trap dynamical variables take values “frozen” at their high-frequency steady-state values determined by the large-signal experimental conditions. The resulting model is validated with respect to independent large-signal and small-signal data.

II. DYNAMICAL EQUATIONS

The intrinsic model total time-dependent output current, given by equation (1.1), is postulated to be a sum of terms corresponding to current and charge sources, which are controlled by five time varying dynamical variables, including the instantaneous intrinsic gate-source and drain-source terminal voltages, $V_{gs}(t)$, $V_{ds}(t)$, and three other dynamical variables. They are $T_j(t)$, the dynamic “junction temperature”, and $\phi_1(t)$ and $\phi_2(t)$, trap states associated with gate-lag and drain-lag, respectively, where $f_1$ and $f_2$ functions represent capture processes similar to those proposed in [3].

$$I_G(t) = I_D(V_{gs}(t), V_{ds}(t), T_j(t), \phi_1(t), \phi_2(t))$$

$$+ \frac{d}{dt}Q_D(V_{gs}(t), V_{ds}(t), T_j(t), \phi_1(t), \phi_2(t))$$

$$\dot{T} = \frac{T_0 - T(t)}{\tau_{th}} + \frac{1}{C_{th}}\left\{I(t)V(t)\right\}$$

$$\dot{\phi_1} = f_1(V_{gs}(t) - \phi_1(t)) + \frac{V_{gs}(t) - \phi_1(t)}{\tau_{1,emit}}$$

$$\dot{\phi_2} = f_2(V_{ds}(t) - \phi_2(t)) + \frac{V_{ds}(t) - \phi_2(t)}{\tau_{2,emit}}$$

Here $\tau_{1,emit}$ and $\tau_{2,emit}$ are the emission time constants. $T_0$ is the ambient or case temperature, $\tau_{th}$ is the thermal time constant, $C_{th}$ is the thermal capacitance, and $\left\{ \right\}$ is the time average. A higher order differential equation can be used in place of (1.2) to better approximate the thermal diffusion partial differential equation. Alternatively, a linear transfer function for the thermal response with a sub-first-order dependence can be used [1].

The gate current does not include trapping effects and is:

$$I_G(t) = I_D(V_{gs}(t), V_{ds}(t), T_j(t)) + \frac{d}{dt}Q_D(V_{gs}(t), V_{ds}(t), T_j(t))$$

(1.5)
III. DEVICE CHARACTERIZATION

A comprehensive characterization of the device is accomplished using an automated nonlinear vector network analyzer (NVNA) [7], synchronized bias supplies, and a fundamental passive load tuner. Details of the HW and SW configuration appear in [5]. The data consists of dynamic trajectories from calibrated NVNA waveform measurements at different RF powers, DC biases, ambient temperatures and load conditions determined by the output tuner or synthetic load provided by the second NVNA source. The particular NVNA used has a bandwidth of 26.5 GHz. Waveforms are constructed from six complex harmonics (+DC) per measurement at fundamental frequencies of 2GHz and 4GHz. The total number of measured waveforms is 8542. Samples of measured dynamic trajectories are presented in Fig. 1.

![Sample 1: \( \Gamma = 0.12 \angle -87^\circ \), \( Pin = 8dBm \), Bias = [0-2.5], Freq = 2GHz, \( T_o = 25^\circ \), Sample 2: \( \Gamma = 0.62 \angle -125^\circ \), \( Pin = -3dBm \), Bias = [0-2.5], Freq = 4GHz, \( T_o = 25^\circ \), Sample 3: \( \Gamma = 0.65 \angle -56^\circ \), \( Pin = 6dBm \), Bias = [0-2.5], Freq = 4GHz, \( T_o = 25^\circ \)]

Fig. 1. Three samples of measured dynamic trajectories.

IV. MODEL IDENTIFICATION FROM LARGE-SIGNAL STEADY-STATE HIGH FREQUENCY DATA

The objective of the training procedure is to identify the functions \( I_D \) and \( Q_D \) in (1.1), from the NVNA data. The NVNA captures large-signal waveforms, calibrated to the device planes. The measurements are taken at several power levels from small-signal to over 8dB compression, at fundamental frequencies of 2GHz and 4GHz, at a variety of loads across the Smith chart. At these high frequencies, for fixed power and load, the \( T_o(t) \), \( \phi_1(t) \) and \( \phi_2(t) \) dynamical variables take on constant values indicative of their average over the RF trajectory corresponding to the large-signal steady-state operating point, such as those of Fig. 1. At steady-state we have therefore:

\[
I_{D_{\text{meas}}} = I_D(V_{gs}(t), V_{ds}(t), T_o, \phi_1(t), \phi_2(t))
\]

where \( T_o \), the ambient or case temperature, \( P_R \) the input RF power, \( Z_{in} \) the complex load impedance, and \( f \) the frequency of the large amplitude single-tone input signal incident into the gate of the transistor. For each waveform, we calculate the corresponding steady-state value of the dynamical variables in (1.6) by:

\[
T_o = T_0 + \left( I(t) V(t) \right) R_{th}
\]

\[
\phi_1 = \text{Min}(V_{gs}(t))
\]

\[
\phi_2 = \text{Max}(V_{ds}(t))
\]

Here \( \text{Min}/\text{Max} \) is the minimum/maximum taken over all points on the periodic large-signal measured waveform. Equations (1.7), (1.8) and (1.9) define particular values for each measured steady-state waveform. The consistency of (1.7), (1.8) and (1.9) with (1.2), (1.3) and (1.4) depends on the fact that the typical thermal and trap emission time constants can be considered long compared with the fundamental RF excitation frequency, and the form of the trap functions \( f_1 \) and \( f_2 \) in (1.3) and (1.4) are such that capture processes are faster than the RF signal whenever the instantaneous terminal voltages exceed the corresponding instantaneous trap state voltage [3]. \( R_{th} \) is the thermal resistance that needs to be independently extracted.

Artificial neural networks (ANN), i.e., \( I_D_{\text{ANN}} \), and \( Q_D_{\text{ANN}} \) are trained to learn the functions \( I_D \) and \( Q_D \) given the set of dynamical variables \( V_{gs}(t), V_{ds}(t) \), and the set of fixed values of junction temperature \( T_o \) and trap state values \( \phi_1 \) and \( \phi_2 \) from (1.7), (1.8) and (1.9), corresponding to each trajectory. Let \( \mathbf{w}_{ID} \) and \( \mathbf{w}_{QD} \) be defined as the neural network internal parameters of \( I_D_{\text{ANN}} \) and \( Q_D_{\text{ANN}} \), respectively. The training objective is to adjust \( \mathbf{w}_{ID} \) and \( \mathbf{w}_{QD} \) to minimize the error functions:

\[
E_k = \sum_{m=1}^{n_{\text{time points}}} \left| I_{D_{\text{meas}}}(m) - I_{D_{\text{meas}}}(m) \right|^2
\]

is the time domain error function and

\[
E_k = \sum_{n=0}^{n_{\text{harmonics}}} \left| I_{D_{\text{spectrum}}}(n) - I_{D_{\text{spectrum}}}(n) \right|^2
\]

is the frequency domain error function, for the \( k \)-th waveform, respectively. \( W_1 \) and \( W_2 \) are the weighting parameters used to balance the time domain and frequency domain error functions. \( I_{D_{\text{spectrum}}} \) and \( I_{D_{\text{spectrum}}} \) are the spectra of \( I_D \) and \( I_{D_{\text{meas}}} \), respectively. The training diagram is illustrated in Fig. 2. This produces the model functions, \( I_D \) and \( Q_D \), which are then evaluated at their time-varying arguments \( V_{gs}(t), V_{ds}(t) \), and \( T_o, \phi_1(t) \) and \( \phi_2(t) \) according to (1.2), (1.3) and (1.4).

The model identified and implemented in this work is therefore a time-domain model of the “compact” type suitable for conventional nonlinear simulators in all modes of simulation (e.g. transient analysis, harmonic balance, and circuit envelope). This is in contrast to X-parameter models, also identified from NVNA data, which constitute a complementary approach to device modeling in the frequency and envelope domains [5, 6].
Fig. 2. Training of $I_{D,ANN}$ and $Q_{D,ANN}$ from measured NVNA waveforms.

V. MODELING FLOW DIAGRAM

The proposed modeling flow is illustrated in Fig. 3.

![Diagram](image)

Fig. 3. The proposed modeling flow diagram.

VI. RESULTS

The device chosen for the model verification is a 300um total gate-width GaAs pHEMT for 50GHz broadband circuit applications. Due to the wide gate recess (to achieve high breakdown and power), this device is suitable to test a model with dynamic effects such as trapping (both gate and drain lags) as well as self-heating.

Results of the identified model function $I_D$ for two different values of the trap state are plotted in Fig. 4.

The model DC intrinsic iso-thermal characteristics are recovered along a submanifold where $\phi_1 = V_{gs}^{DC}$ and $\phi_2 = V_{ds}^{DC}$ in the $I_D$ function, namely $I_D(V_{gs}, V_{ds}, T_j, \phi_1 = V_{gs}, \phi_2 = V_{ds})$. Fig. 4a shows a “knee walk-out” effect compared to the iso-thermal static model predictions of Fig. 4b.

Fig. 5 shows the comparison of the modeled and measured DC curves, where excellent agreement is achieved.

The S-parameters at high frequency correspond to partial derivatives of both, $I_D$ and $Q_D$ functions evaluated at trap states corresponding to the DC operating point. The measured and simulated S-parameters are in excellent agreement over the entire frequency and bias range. This is demonstrated in Fig. 6. for two very different operating conditions.

Fig. 4. Model intrinsic channel current function at $T_j = 65^\circ C$.
(a) fixed trap state = [-2.0, 8.0] (b) along trap states corresponding to the DC operating points.

Fig. 5. Extrinsic DC curves: modeled (___) and measured ( o )

![Diagram](image)

Fig. 6. S-parameters: modeled (—) and measured ( o ), from 0.5 GHz to 50 GHz at two different bias points: (a) $V_{gs} = -0.2$ V, $V_{ds} = 5.0$ V and (b) $V_{gs} = -2.0$ V, $V_{ds} = 5.0$ V, respectively.
The excellent ability of the model to reproduce the device frequency dispersion is due to the extra degrees of freedom provided by both the trap variables as well as the junction temperature. Note that a model just including dynamic self-heating is unable to fit the actual dispersion between DC and RF well over the entire bias range.

Under large-signal conditions, the definitions (1.3) and (1.4) mean that the dynamical variables deviate from their values under small-signal or DC conditions. This changes the shape of the nonlinear model constitutive relations, as demonstrated in Fig. 4, and enables the detailed large-signal trajectories to be well-approximated over a wide range of loading conditions.

A comparison of the model large-signal predictions with respect to measured gain compression, bias current, and harmonic distortion is presented in Fig. 7. The model agrees to a very high level (11dB) of compression and does a good job modeling the non-ideal shape of the compression and harmonic distortion curves. The non-monotonic dependence of the bias current with power is a validation of the significance of the drain-lag mechanism [3] and present identification methodology.

Fig. 7. Measured (symbol) vs. simulated (line) (a) Gain vs. Pout and Bias current vs. Pout (b) Harmonics vs. Pin, where good agreements are achieved. The device is biased at [-0.2, 3], and Frequency=2GHz.

Fig. 8 shows the comparison of the modeled and measured Gain vs. Pout, at 38GHz. The model was identified from 2 GHz and 4 GHz data only, yet it is capable of accurately predicting the large-signal device characteristics at much higher frequencies. A comparison between Fig. 7 and Fig. 8 shows the significant reduction in saturated power at high-frequency (38GHz) compared to low frequency (2GHz) for this device. The ability of the present model to predict this effect is a direct consequence of the trap-dependence of the drain charge.

VII. CONCLUSIONS

A new nonlinear FET model, incorporating dynamics of self-heating and dynamic trapping phenomena in both the output current and charge functions, has been systematically identified from large-signal data obtained from automatically controlled NVNA load-dependent large-signal measurements. The model is implemented in a commercial nonlinear circuit simulator (Agilent ADS). Extensive large and small-signal validation measurements were used to validate the model. The model incorporates frequency dispersion, very accurately accounts for distortion effects from small-signal conditions to very large levels of compression at both low and high frequencies, accounts for “knee walkout,” frequency-dependent power saturation, and other large-signal dynamical effects common to GaAs and GaN FETs. The model and its identification methodology from large-signal NVNA data is therefore a significant advance beyond prior practice.

REFERENCES