Welcome

Innovations in EDA Webcast Series
August 2, 2012
IC, Laminate, Package Multi-Technology PA Module Design Methodology

Realizing the Multi-Technology Vision within a fully integrated design flow in ADS

Jack Sifri
MMIC Design Flow Specialist

August 2nd, 2012
IC, Laminate, Package Multi Technology PA Module Design

Agenda

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
IC, Laminate, Package Multi Technology PA Module Design

**Typical Example:**

Complex ICs in multi-chip RF modules:

**The New iPad**
IC, Laminate, Package Multi Technology PA Module Design

Typical Example:

Agilent’s X-Series 40 GHz Signal Analyzer Multi Technology Board
Multi Technology Example (Agilent EMG)

- Stripline Filter on PC Board
- Designs with SMT packages and bare die components (wire bonded)
- Integrated Circuits Designs and Thin Film Circuit Designs
- Shielding and Isolation walls
Zooming on the Thin Film IC Interface

Wide Band LO Distributing Amp
Thin Film Coupler / LO Distributing Amp Interface

- 6 Layers Rogers Board
- Octave wideband coupler
- GaAs LO distributing amp
- Bond wired and epoxy SMT Caps (DC)
- Blocking Capacitor - to Edge connector
  - available LO for testing mixers
  - Filtering DC Lines
Board / Laminate / IC/ SMT / Bondwires

A multi-technology module example requires Full 3D FEM Simulation

Wide band LO distributing amp swept for use at different bands

6 layers Rogers board

Wide band coupler

Bond wires / coupler / IC interface caused unleveled ripple in the wide band output signal
IC, Laminate, Package Multi Technology PA Module Design

Agenda

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   • Single chip module
   • Multi chip module
   • Flip chip /solder bumps module
   • Transceiver module
   • Electro thermal simulation
5. Conclusion
IC, Laminate, Package Multi Technology Module

Design Challenges

Design flows are not able to address multiple technology designs

- IC, laminate, package, and PCB need to be designed together
- EM interactions between substrates need to be modeled and accounted for
- The need to move from disjointed tools design flows to simplified integrated flows
EM Modeling Process in a Disjointed Design Flow

**START**

1. ADS Layout
2. Export GDS file
3. Import GDS file into other 3rd party EM tools
4. Re-Assign material information
5. Set up geometry & ports for simulation
6. Run EM simulation for S-parameters
7. Import S-parameters from EM tool into ADS

**Auto-generate Ports**
(For complex designs)

**REPEAT**

1. Export port locations to a .MSK file
2. Run custom program to create script file to auto-generate ports in 3rd party EM tools
3. Import GDS file

**END**

**Hours of Simulation**
- 10 min.
- 20 min.
- 30 min.
- 30 min.
- 10 min.

**Copyright © 2014 Keysight Technologies**
EM Modeling Process in an Integrated Design Flow

START

ADS Layout

Run EM simulation for S-parameters

ADS Tech file

Finish
IC, Laminate, Package Multi Technology PA Module Design

**Agenda**

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
Multi-Technology Design Methodology

- Discover coupling efforts prior to fabrication
- More effectively optimize design elements for final packaging
- More easily make design trade-offs
- Help diagnose and solve performance problems

Package + IC + IC = Multi-technology EM Simulation

3D view
Momentum
FEM
Fully Integrated Design Flow in ADS 2011 and 2012

System; Circuit; Physical; Thermal; Planar/3D EM; Wireless Verification

ADS Multi Technology Integrated Design Environment

- System Specs
- X-parameters
- Schematic
- Statistical
- Wireless Verification
- Layout
- Integrated 3D-Planar & FEM Tools
- Models and PDKs
- Electro Thermal Simulation
- LVS / DRC
- Final Verification
  - Package/ Bond Wires/ Module
  - Integrated 3D Planar & FEM
  - Wireless Standards
  - Electro Thermal

- Discover coupling effects prior to fabrication
- First Pass Success
- Consistent results / high yield
- Lower development & production costs
- Time to Market
- Lower Risk

No Walls and no loops in this design process; Fully Integrated Flow;
One designer completes and verifies the full design all in one design environment
Multi-Technology Design Methodology

Design IC #1 (IPD – Filter)

Design IC #2 (LNA)

Design Package/Laminate
Bring in all the libraries together and build the whole assembly
IC, Laminate, Package Multi Technology PA Module Design

**Agenda**

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
Example: Packaged LTE PA on Laminate

- Two Stage LTE PA built on a GaAs substrate
  - Placed onto a DFN package and mounted on a laminate board.
Packaged MMIC PA Design Example

Case 1: MMIC PA - Circuit models Simulation
Case 2: MMIC PA – Momentum Simulation
Case 3: Combine MMIC Momentum & FEM of Package
Case 4: FEM on the Whole Module
Input Matching Network is shown to exhibit coupling effects (freq shift)
Packaged MMIC PA - Results
Four different simulation results (case 1-4)

MMIC
Black: Circuit Model
Green: Momentum

MMIC + Package
Blue
IC_Mom + Pkg_FEM

Red
Whole Module_FEM

Freq Shift due to bond wires. Less gain due to mismatch loss & substrate coupling.

Cases: 1-4
Compare Module FEM Results with (Pkg_FEM + MMIC_Momentum) and with Circuit simulation results
Packaged MMIC PA Design Example Results

Pout

Circuit

Assembly_FEM

Pkg(FEM) + MMIC(Momentum)
QFN Designer in ADS
Predict Packaged Performance in Minutes

Configure QFN package

Accurately predict real performance

Quickly synthesize complex package, combine with IC & PCB data

Performance w/ & w/o package
Amkor Package Design Kit for ADS
Predict Packaged Performance in Minutes

Configure QFN package

Accurately predict real performance

Quickly synthesize complex package, combine with IC & PCB data

Performance w/ & w/o package

MMIC in Package and with bond wires

freq, GHz

Copyright © 2014
Keysight Technologies
Page 27
IC, Laminate, Package Multi Technology PA Module Design

**Agenda**

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
Bounding the IC within the Package/ Laminate Assembly
A Word on Bounding the IC using “Boundary Area Layer”

- Layout has no Bounding Area
- 3D view shows the MMIC substrate extending out through the bond wires (Results in inaccurate FEM simulation results)
Multi Technology Module Setup with Bounding the IC

- Bounding Area layer box has been added in the Layout as shown.
- 3D view (next page) shows the bounding of the MMIC for FEM simulation
Multi Technology Module Setup with Bounded IC

- 3D view shows how the use of “Bounding Area Layer” (last page) has resulted in bounding IC substrate (cookie cut) for FEM simulation
Multi Technology Module Setup
With and without Bounding area layer

Before adding Bounding Layer to the IC

After adding Bounding Layer to the IC
Multi Technology FEM Simulation Set up
Ku band LNA (PDK1) followed by Ku band Filter (PDK2)
Multi Technology Module Layers Stack up
Nested Technology substrates

IC #1 layer stack up

IC #2 (IPD) layer stack up

Mounted ICs
QFN Package layers
Laminate layers
Multi Technology 3D FEM Simulation in ADS 2012

Substrate stackup

IC#1

Package

Laminate

IC#2

Demo

Copyright © 2014
Keysight Technologies
IC, Laminate, Package Multi Technology PA Module Design

**Agenda**

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
Flip Chip / Flip Package onto Board

Flipped Package ready to mount onto a board

Flipped IC chip mounted inside package cavity
Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board
Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board

Flipped IC chip mounted inside package cavity
Flip Chip / Flip Package onto Board

Flipped Package mounted onto a board – side view
Flip Chip / Flip Package onto Board

Flipped IC chip to be mounted inside package cavity
Flip Chip / Flip Package onto Board

Flipped IC chip mounted inside package cavity
Flip Chip / Flip Package onto Board

Flipped Package and Chip onto a laminate board

laminate board
FR4 material

0.3 millimeter
IC, Laminate, Package Multi Technology PA Module Design

Agenda

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   • Single chip module
   • Multi chip module
   • Flip chip /solder bumps module
   • Transceiver module
   • Electro thermal simulation
5. Conclusion
Example: Transceiver using Multi Technology

- Transceiver consists of mainly seven major technologies:

1. Antenna: single layer C-band microstrip patch antenna
2. Power Amplifier - X-parameter file of MMIC power amplifier
3. LTCC BPF : 3 pole filter based on 6 layer LTCC technology
4. 3D SMA Connector from EMPro library
5. Standard QFN Package for LNA and switch
6. MMIC SPDT switch
7. MMIC LNA
Transceiver Parts and Technologies

- Total 12 equivalent layer board
- 7 different technologies
- 2 stack up + 4 side by side technologies
- EMPro design as lib component
- 3 different layout units

mm
( millimeter)

mil

um
IC, Laminate, Package Multi Technology PA Module Design

**Agenda**

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   - Single chip module
   - Multi chip module
   - Flip chip /solder bumps module
   - Transceiver module
   - Electro thermal simulation
5. Conclusion
New Electrothermal Solution in ADS2012

- Improves high power MMIC / RFIC designs
- Delivers ‘thermally aware’ circuit simulation results
- Includes effects of package and PCB
- Easy to set up and use from within ADS
- Works with all simulation types: DC, AC, SP, HB, Transient, Envelope
New Electrothermal Solution in ADS2012

Circuit Simulator

Thermal Simulator

Thermal technology files
New Electrothermal Solution in ADS2012

**Circuit Simulator**
- simulate to convergence
- write power dissipation

**Thermal Simulator**
- read power dissipation
- create heat sources
- solve thermal equation
- write temperatures

Thermal technology files

P$_{D\text{ISS}}$, T$_{\text{DEVICES}}$
New Electrothermal Solution in ADS2012

Circuit Simulator
- read temperatures
- use previous solution
- simulate to convergence
- write power dissipation

Thermal Simulator
- read power dissipation
- create heat sources
- solve thermal equation
- write temperatures

Iteration loop is
done automatically
until powers and
temperatures are
self-consistent
New Electrothermal Solution in ADS2012

Circuit Simulator
read temperatures
use previous solution
simulate to convergence
write power dissipation

T_{DEVICES}

P_{DISS}

Thermal Simulator
read power dissipation
create heat sources
solve thermal equation
write temperatures

Iteration loop is
done automatically
until powers and
temperatures are
self-consistent

Thermal technology files

Copyright © 2014
Keysight Technologies

Page 55
Temperature Profile – Active Base Region
### Output Results

<table>
<thead>
<tr>
<th>freq (GHz)</th>
<th>dBm(out_cold)</th>
<th>dBm(out_hot)</th>
<th>delta</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>-2.57</td>
<td>-2.57</td>
<td>7.15E-5</td>
</tr>
<tr>
<td>2.00</td>
<td>-42.06</td>
<td>-33.97</td>
<td>8.08</td>
</tr>
<tr>
<td>3.00</td>
<td>-28.48</td>
<td>-28.25</td>
<td>0.22</td>
</tr>
<tr>
<td>4.00</td>
<td>-50.03</td>
<td>-56.92</td>
<td>-6.88</td>
</tr>
<tr>
<td>5.00</td>
<td>-57.16</td>
<td>-54.84</td>
<td>2.32</td>
</tr>
<tr>
<td>6.00</td>
<td>-66.20</td>
<td>-66.84</td>
<td>-0.64</td>
</tr>
<tr>
<td>7.00</td>
<td>-75.86</td>
<td>-72.56</td>
<td>3.30</td>
</tr>
<tr>
<td>8.00</td>
<td>-84.32</td>
<td>-84.30</td>
<td>0.01</td>
</tr>
<tr>
<td>9.00</td>
<td>-94.32</td>
<td>-89.87</td>
<td>4.44</td>
</tr>
<tr>
<td>10.0</td>
<td>-100.54</td>
<td>-96.36</td>
<td>1.16</td>
</tr>
<tr>
<td>11.0</td>
<td>-113.14</td>
<td>-106.76</td>
<td>6.38</td>
</tr>
<tr>
<td>12.0</td>
<td>-117.11</td>
<td>-115.14</td>
<td>1.96</td>
</tr>
<tr>
<td>13.0</td>
<td>-128.54</td>
<td>-122.43</td>
<td>6.11</td>
</tr>
</tbody>
</table>

---

[Graphs and charts showing measurement data]
Time-Domain Results
Electro Thermal Simulation
2-Stage GaAs LTE PA

Layout with heat sources

schematic

Layout
Electro Thermal Simulation
2-Stage GaAs LTE PA
Electro Thermal Simulation – Heat Flux
2-Stage GaAs LTE PA
Electro Thermal Simulation Results

2-Stage GaAs LTE PA

Solid Lines: Electro Thermal Simulation ON
Dashed Lines: Electro Thermal Simulation OFF
Electro Thermal Simulation Results
HB DC current at Hot Vs Room Temp

HB DC current at "Hot" and at "Room Temp"
Electro Thermal Simulation Results

Harmonics at Hot Vs Room Temp

![Graph showing harmonic results with Electro Thermal Simulation OFF and ON at Pin=-1 dBm.](image-url)
IC, Laminate, Package Multi Technology PA Module Design

Agenda

1. Multi technology Examples
2. Design Challenges
3. Improved Design Methodology
4. Illustrate with few applications
   • Single chip module
   • Multi chip module
   • Flip chip /solder bumps module
   • Transceiver module
   • Electro thermal simulation
5. Conclusion
Integration Challenges with Multi-Technologies
The Ultimate “Device” Characterization Challenge

- Behavioral model for PA IC (X-parameters)
- Multiple IC's of different fabrication technologies
- Passive EM Simulation of Entire Laminate
- Model Package, solder bumps, bond wires
- Model connector
- Chip, module, board interactions

Amalfi AM7802
PA Front End Module
Summary

- RF design has moved to complex ICs in multi-chip RF modules
- Today’s design flows are not able to address multiple technology design
- The IC, laminate, package, and PCB need to be designed together
- Electro-magnetic interactions between substrates need to be modeled
- ADS 2012 EDA software is able to address these multi-technology design challenges
Hands-on Workshop Available

- A Hands-on Workshop is available for training
## Workshop Outline

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Section 1</td>
<td>Starting a New Workspace “Module”</td>
<td>5</td>
</tr>
<tr>
<td>Section 2</td>
<td>Adding Libraries to our Module Workspace</td>
<td>12</td>
</tr>
<tr>
<td>Section 3</td>
<td>Creating a new Cell for Module FEM simulation</td>
<td>21</td>
</tr>
<tr>
<td>Section 4</td>
<td>Nested Technology / View Specific Configuration</td>
<td>28</td>
</tr>
<tr>
<td>Section 5</td>
<td>Nested Technology Setup</td>
<td>31</td>
</tr>
<tr>
<td>Section 6</td>
<td>Building the Module Assembly</td>
<td>41</td>
</tr>
<tr>
<td>Section 7</td>
<td>Placing and Configuring the Bond Wires</td>
<td>46</td>
</tr>
<tr>
<td>Section 8</td>
<td>Creating the Module Layer Stack-up Substrate</td>
<td>52</td>
</tr>
<tr>
<td>Section 9</td>
<td>Defining the IC Bounding Area for FEM Simulation</td>
<td>63</td>
</tr>
<tr>
<td>Section 10</td>
<td>FEM Simulation Set-up and Results</td>
<td>76</td>
</tr>
</tbody>
</table>
You Are Invited

Innovations in EDA Webcast Series

Power Amplifier Design with X-Parameter Power Transistor Models

September 6 • 10 AM (Pacific Time)

Free 1-hour Webcast

www.keysight.com/find/eesof-innovations-in-eda

www.keysight.com/find/eesof-webcasts-recorded

Dr. Larry Dunleavy, President & CEO Modelithics Inc.