Taking the Mystery out of Signal Integrity

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Overview

“There are two kinds of design engineers, those that have signal integrity problems, and those that will”

• The four signal integrity problems
• Why signal integrity will get harder to solve
• The right design methodology
• The role of accurate, high bandwidth measurements
• Two case studies: switching noise, probing
What is Signal Integrity?

How the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips, and what to do about it.

General SI Problem #1:

• If the instantaneous impedance a signal sees ever changes, some of the signal will reflect and the rest will be distorted.

• Ringing is often due to multiple reflections between impedance discontinuities at the ends.
Signal Integrity Engineering is about Finding and Fixing Problems

3 inch long PCB Trace

3 inch long PCB Trace

Series termination (~40 Ohms)

A Guiding Principle

In order to solve a signal integrity problem you must first understand its root cause
Signal Integrity Initially Looks Confusing

The Four High Speed Problems

1. **Signal quality** of one net: reflections and distortions from impedance discontinuities in the signal or return path

2. **Cross talk** between multiple nets: mutual C and mutual L coupling with an ideal return path and without an ideal return path

3. **Rail collapse** in the power distribution system (PDS): voltage drops across impedance in the pwr/gnd network

4. **EMI** from a component or the system
Conceptual Origin of Simultaneous Switching Output (SSO) Noise

What influences SSO Noise:
- Mutual inductance between the loops
- Number of SSOs
- \( \frac{dI}{dt} \)

Projected Increase in Clock Frequencies

Source: SIA Roadmap

Microprocessor based products

Year

Source: SIA Roadmap
High Speed Serial Link Applications
Drive High Frequency

Hypertransport 1.6 Gbps (400 MHz- 1.6 GHz)
AGP8x 2.1 Gbps (533 MHz)
3GIO 2.5 Gbps (2 x 1.25 GHz)
Infiniband 2.5 Gbps (2.5 GHz)
OC-48 2.488 Gbps (2.5 GHz)
OC-192 9.953 Gbps (10 GHz)
RapidIO16 32 Gbps (1 GHz, 16 bit mode)
OC-768 39.81 Gbps (40 GHz)

A Scary Future

Smaller transistor channel lengths → shorter rise times, higher clock frequencies
Short rise times → signal integrity problems get worse
Shorter design cycle times → designs must work the first time

“There are two kinds of design engineers, those that have signal integrity problems, and those that will”

So what’s the right design methodology?
Example: Gold Dot Interconnect from Delphi

**General Construction**

Flexible Circuit Based Interconnect

Mezzanine and Backplane Configurations

Gold Dot Flexible Circuit Clamp Housing

Elastomer PCB Stiffener Jumper

Mezzanine and Backplane Configurations

Broad Connection System Applicability

Small, precisely shaped bump contacts on FPC footprint (Gold Dots™)

Applications

Courtesy of Laurie Taira-Griffin, Delphi

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The Old **Build it and Test it** Design/Manufacturing Cycle

Design of Circuit based on Performance of Previous Design 5 Days

Redesign 3 Days

One Cycle 9 Weeks Average 2 Cycles/Design

Manufacture (CAD 2 Days) 4 Weeks

Test (TDR, VNA, BERT) 1-2 Weeks

Cross Section Confirm Physical Layout 2 Days

SPICE Model 1 Week

Courtesy of Laurie Taira-Griffin, Delphi
Key Ingredient to the New Design Methodology: Predicting Signal Integrity Performance

- Critical processes for predicting signal integrity problems
  - Create equivalent circuit models for all components
  - Simulate performance of components, critical nets and the whole system

- The better we can predict performance:
  - find and fix problems as early in the design cycle as possible
  - reduce extra design margin required
  - reduce time to market
  - reduce risk
  - reduce development and production costs

Role of Measurements

**Verify** a model and simulation from a calculation (anchor to reality)

- Rules of thumb
- Analytic approximation
- Numerical tool: field solver, circuit simulation tool

**Create** a model from a real structure

- Directly from the front screen
- Iteration process: inverse scattering
Example: Implementing a Characterization Loop to Develop and Verify Modeling and Simulation Process at Delphi

![Image of VNA, BER TDR, and GigaTest Probe Station](image)

Measured OC-192

Simulated

Courtesy of Laurie Taira-Griffin, Delphi

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### Final Verification of Model and Performance Simulation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulation</th>
<th>Measured</th>
<th>Goal</th>
</tr>
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<tbody>
<tr>
<td>Single Ended Impedance</td>
<td>52.1 Ohms</td>
<td>53 Ohms</td>
<td>50 +/-10% Ohms</td>
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<tr>
<td>Differential Impedance</td>
<td>95.2 Ohms</td>
<td>98 Ohms</td>
<td>100 +/- 10% Ohms</td>
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<tr>
<td>Attenuation (5GHz)</td>
<td>&lt;.44 dB/inch</td>
<td>&lt;.44 dB/inch</td>
<td>&lt;.5 dB/inch</td>
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<td>Propagation Delay</td>
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<td>170 ps/inch</td>
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<tr>
<td>Single Ended NEXT</td>
<td>&lt;4.5%</td>
<td>&lt;4.5%</td>
<td>&lt;5%</td>
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<tr>
<td>Differential NEXT</td>
<td>&lt;.3%</td>
<td>&lt;.3%</td>
<td>&lt;.5%</td>
</tr>
<tr>
<td>Data Rate</td>
<td>&gt;5 Gbps</td>
<td>&gt;5 Gbps</td>
<td>5 Gbps</td>
</tr>
</tbody>
</table>

Courtesy of Laurie Taira-Griffin, Delphi
Cycle Time Reduction with Reliable Modeling and Simulation

**Was:** > 9 weeks to reach correct design

**Now:** 4 hours to reach correct design

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Role of Models

- **Accurate** models of interconnects
- **Accurate** models of the active devices
- **Robust** simulator

\[ \text{Prediction of performance} = \text{Accurate models of interconnects} + \text{Accurate models of the active devices} + \text{Robust simulator} \]

*The earlier in the design cycle problems are found and designed out, the shorter the cycle time, the lower the development costs*

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Courtesy of Laurie Taira-Griffin, Delphi
Two Case Studies: Measurement Based Model Extraction

- Modeling 2 SMT resistors and predicting switching noise
- Modeling an active scope probe and optimizing it for minimum artifacts

Important Elements to a Complete Measurement/Modeling Solution

Probes
- GigaTest Labs
- Probe stations

Instruments
- Infiniium DCA with TDR
- Vector Network Analyzer

Controlling software
- TDA Systems software
- Agilent Advanced Design System (ADS)
Measured $S_{11}$ of one 0805 SMT Resistor

Two, 0805 resistors, ~120 mils centers, far end shorted to return plane ~15 mils below surface

Smith Chart of Measured $S_{11}$

Measured with a Vector Network Analyzer (VNA)

Close up of typical probing method

$1^{st}$ and $2^{nd}$ Order Models, Created and Simulated with Agilent Advanced Design System (ADS)

$1^{st}$ order model

$R = 50$ Ohms
$L = 2$ nH

$2^{nd}$ order model

$R = 50$ Ohms
$L = 2$ nH
$C = 0.3$ pF

Non-optimized values

$f_{eq}$ (12.50MHz to 5.013GHz)
Using ADS to Optimize 2nd Order Model

Optimized values:
- R = 52 Ohms
- L = 1.85 nH
- C = 0.162 pF

Features of the Model

- A simple model matches the measured performance very well
- The interconnect model is very accurate
- Bandwidth of the model is at least 5 GHz—could be higher
- The precise parameter values will depend on the location of the return plane and the via structures
Measured Coupling: $S_{21}$

What does $-60$ dB coupling mean?

$$\frac{V_{\text{quiet}}}{V_{\text{active}}} = 10^{-60} = 10^{-3} = 0.1\%$$

How much coupling is too much?

Depending on the noise budget, $\sim -30$ dB ($\sim 3\%$)

Modeled Cross Talk

Topology for coupled resistors uses exactly the same circuit model for isolated resistors, with mutual inductance added

$$R = 51 \, \text{Ohms}$$
$$L = 1.85 \, \text{nH}$$
$$C = 0.162 \, \text{pF}$$
$$K = 0.152 \, (L_{12} = 0.28 \, \text{nH})$$

What does the switching noise look like in the time domain?

@ 3.5 GHz, coupling $\sim -25$ dB, $\sim 5\%$

With 100 psec rise time, expect $V_{\text{SSN}}$ $\sim 5\% \times 3.3\, \text{V} \sim 160 \, \text{mV}$
Simulating Switching Noise in the Time Domain with ADS

- Same model of the coupled resistors
- 5 Ohms source impedance of the driver
- Quiet line receiver in tri state
- Rise time of 100 psec, BW ~ 3.5 GHz, 500 MHz clock

Simulating Switching Noise

Active Line

Quiet receiver

Does this look familiar?
Measured Switching Noise in Graphics Processor Daughter Card

- Mutual inductance causes 90% of all switching noise problems

Is the “ringing” real or artifact?

Probing Signals in Active Circuits

- Agilent 1158A Active Probe, (not using recommended fixturing)
- Measured signal through probe
- What causes the ringing?
- Is it real or artifact?
- How can the artifacts be minimized?
What Impedance does the Signal See for the Probe?

- Features of the probe's input impedance
  - Really high impedance < 100 MHz
  - Capacitive > 500 MHz
  - As low as 10 Ohms @ 1 GHz!
  - Multiple resonances

Measured impedance looking into the probe tip
(measured using VNA)
(not using recommended fixturing)

Circuit Model of the Probe:
Simulated with Agilent ADS

- Simple model fits the measured impedance really well
- Ringing is due to the LC
- L due to the long lead (~ 5 cm x 10 nH/cm)
- Model can be used to evaluate impact on the circuit under test
All the Ringing is Due to the Artifact of the Probe Tip

Step 1: Optimize Probe Performance by Minimizing Tip Length

There is still some LC ringing from the tip!
Step 2: Damp out the Ringing with a Resistor

First order estimate of R based on Q

\[ Q = \frac{1}{\sqrt{\frac{L}{R}C}} \]

\[ R \sim 100 - 250 \Omega \]

- Role of the resistor:
  - Damps the ringing
  - Keeps loading of the circuit high
  - Optimizes the bandwidth of the transfer function

Performance Improvement from Damping Resistor: \( \tau_{in} = 200 \text{ psec} \)
Agilent 1158A with Integrated Damping Resistor Tips

Summary of Good Probe Techniques

1. Keep probe lengths as short as possible
2. Use integrated damping resistor
3. Select R value based on Agilent recommended table
4. Always consider the impact of the probe’s impedance on the circuit performance
The Critical Ingredients to Solving Signal Integrity Problems

- **Principles and Understanding**
- **Analysis:**
  - Rules of thumb
  - Approximations
  - Numerical simulation
- **Characterization:**
  - Vector Network Analyzer
  - Time Domain Reflectometer

Conclusions

1. **The bad news:**
   - Signal integrity problems will only get worse as rise times decrease
   - Design cycle times will only get shorter as the industry becomes more competitive
2. **The good news:**
   - Accurate modeling and simulation tools are critical to find and fix signal integrity problems as early as possible in the design cycle
   - Measurements are essential to verify and create accurate high bandwidth models
   - Understand the source of probing artifacts and optimize the probe design to minimize them
3. **Help is available:** GigaTest Labs (Agilent VAR) can assist you in:
   - providing a complete turn key measurement system
   - performing measurements and creating models for you
   - helping you move up the learning curve with signal integrity training