Signal Integrity: Problems and Solutions

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(copies of the presentation are available for download on the web site)

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Overview

• What is Signal Integrity?
• Why is it growing in importance?
• What can you do about it?
MYTHS
Signal Integrity and Interconnect Design

How the electrical properties of the interconnects screw up the beautiful, pristine signals from the chips.

The Confusing Mix of Signal Integrity Problems

- Terminations
- Emissions
- Attenuation
- Non-monotonic edges
- Ground bounce
- Skin depth
- Inductance
- Critical net
- Signal integrity
- Transmission lines
- Undershoot, overshoot
- Line delay
- Parasitics
- Capacitance
- EMI/EMC
- Susceptibility
- Loaded lines
- Power and ground distribution
- Lossy lines
- IR drop
- Crosstalk
- Stub lengths
- Gaps in planes
- Reflections
- Dispersion
- Delta I Noise
- RC delay
- Reflections
The Four High Speed Problems

1. Signal quality of one net: reflections and distortions from impedance discontinuities in the signal or return path

2. Cross talk between multiple nets: with ideal return paths, and without (SSO)

3. Rail collapse in the power and ground distribution network

4. EMI from a component or the system

Signal Quality on One Net: Distorted by the Interconnect

Simulated with Hyperlynx
**Cross Talk Between Two Adjacent Conductors - Ideal Return Path**

The far end noise is ~ 10x larger than the near end noise.

Rise time ~ 100 psec, TD ~ 1 nsec.

*HP 83480 High speed scope and TDR*

**Conceptual Origin of SSO Noise**

- **On-Chip**
- **Switching lines**
- **Quiet data line**
- **Inductance**
- **Power common lead**

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**Simple Example of Rail Collapse**

100 nF

**Source:** National Semiconductor

**Radiated Emissions and Power and Ground Routing**
Two Classes of High Speed Problems

- Timing: setup, hold, propagation delay, skew
  ✓ Scales with decreasing clock period

- Electrical Noise: signal integrity and EMI
  ✓ Scales with decreasing rise time
  \[
  \frac{dl}{dt} \frac{dV}{dt} \quad f, f^2
  \]

...it’s the rise time, ...

SSO noise ~ \( \frac{N \times L}{\tau} \)

- \( N \) = number of switching leads per ground leads
- \( L \) = lead inductance or lead length
- \( \tau \) = rise time
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Shorter Delays Mean Shorter Clock Periods, Higher Clock Frequencies

Digital Clock Frequencies are Increasing: doubling every 2 years!

1

10

100

1,000

10,000


Introduction Year

Clock Frequency (MHz)

Clock frequency of Intel Processors

High speed usually refers to increasing clock frequency

Increase in Clock Frequencies

Clock Frequency (MHz)

on-chip

on-board

Source: SIA Roadmap
Rise Times Are Loosely Related to Clock Frequency

\[ \tau \sim \frac{1}{10 F_{\text{clock}}} \]

What is the consequence of higher speed?

The Driving Force Fueling the Electronics Revolution: Gate Length Feature Size Reduction

50% reduction every 4 years
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Transistors Switch Faster As Channel Length Shrinks

Shorter channel length means:

- Shorter delay
- Shorter rise time

What can happen to the clock period and clock frequency?

Situation Analysis

- Clock frequency will get faster
- Rise times for every chip will get shorter
- SI problems will be more significant
- Design cycle times will be decreasing

Conclusion:
Getting new products to market on time will be harder.

Solution:
A new design methodology is needed.
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The Old Design Strategy

- Guess a design
- Hope it works
- Build it
- Test it
- Try to Fix it
- Ship it

Details of the Three Design Approaches

The earlier in the design cycle problems can be identified and solved, the lower the development cost and the faster time to market.

Design by correcting

Correct by design

Design by virtual iteration

Design by correcting

Source: G. Doyle, Mentor Graphics
**Two Critical Processes for Virtual Design and Test**

**Modeling:** Translating the physical world into an equivalent electrical circuit model (Schematic)

**Simulation:** Predicting voltage/current waveforms based on the circuit behavior

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**Where do Models Come From?**

- **Calculations:** (03, 06)
  - Rules of thumb
  - Analytic approximation
  - Parasitic extraction numerical tools: field solvers

- **Measurements:** (06)
  - Impedance analyzer (LCZ)
  - Network Analyzer (NA)
  - Time Domain Reflectometer (TDR)

*Courtesy of TDA Systems*
Two Tools for Simulating Circuits

- **SPICE**: Simulation Program with Integrated Circuit Emphasis
  - PSPICE from OrCAD/Cadence
  - IsSPICE from Intusoft
  - Advanced Design System (ADS) from HP Eesof
  - Maxwell SPICE from Ansoft
  - Micro-CAP from Spectrum
  - HSPICE from Avant!

- **IBIS** based simulators: Input/output Buffer Interface Specification
  - Hyperlynx (Pads)
  - Veribest/Mentor Graphics
  - Zukun Redac
  - Viewlogic
  - Interconnectix (Mentor Graphics)

Design Principles for Good SI

<table>
<thead>
<tr>
<th>Noise Categories</th>
<th>Design Principles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Quality</td>
<td>Signals should see the same impedance through all interconnects</td>
</tr>
<tr>
<td>Cross talk</td>
<td>Keep spacing of traces greater than a minimum value, minimize mutual inductance of non ideal returns</td>
</tr>
<tr>
<td>Rail Collapse</td>
<td>Minimize the impedance of the power and ground path</td>
</tr>
<tr>
<td>EMI</td>
<td>Minimize bandwidth, minimize ground impedance and shield</td>
</tr>
</tbody>
</table>

When are you done? How much reduction is enough?
**Every Design is a Custom Design!**

...just follow these RULES

Cost factors:
- money
- time
- risk

**Performance**

(meet specs)

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**Design Tradeoffs Are Negotiated With a Budget**

- Total voltage swing is 3.3v
- Within 500 mV, all the noise sources must be accounted for:

An example:

<table>
<thead>
<tr>
<th>Noise Source</th>
<th>Allocated Budget</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ringing/reflections</td>
<td>100mV</td>
</tr>
<tr>
<td>Discontinuities</td>
<td>40mV</td>
</tr>
<tr>
<td>Cross talk</td>
<td>90mV</td>
</tr>
<tr>
<td>SSO noise</td>
<td>120mV</td>
</tr>
<tr>
<td>Rail collapse</td>
<td>100mV</td>
</tr>
<tr>
<td>Total*</td>
<td>450mV</td>
</tr>
<tr>
<td>Margin</td>
<td>~50mV</td>
</tr>
</tbody>
</table>

*dynamic effects important

- In hi speed systems, keeping within the noise budget is HARD!
- The more accurately you can predict performance, the less margin needed and the higher the performance
**The Most Important General Design Principles**

1. Slow down edges
2. Minimize the length of all interconnects
3. Use low dielectric constant materials for signal layers
4. Use controlled impedance lines and terminate
5. Minimize loop mutual inductances between signal lines
6. Use continuous, closely spaced, adjacent power and ground planes

**#1 solution:**
slow down the edges

50 Ohm line

Top view

2 short stubs (capacitive discontinuity)
150 mils spacing

Longer the rise time, smaller the impact, or, the shorter the discontinuity, the smaller the impact

50 psec
**Minimize Bandwidth**

Avoid resonance and clock harmonics

AVX Z chip: integrated RC, with low stray C

Figure 28. Data from Ansoft HFSS showing the field distribution on and off resonance for a 208 lead QFP, excited at one lead.

**#2 solution: shorter is better**

- Reflections:
- Cross talk
- Rail collapse
- EMI

Mutual C, mutual L, scale with length
Series L scales with length
Radiated emission scales with length of current path
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Terminations will Minimize Reflected Noise from the Ends

Source: Analog Devices

Avoid Stubs and Branches

(for 0.5 nsec edges, stub length < 0.5 inches)
**MYTHS**

Thin Power and Ground Layers Reduce Switching Noise

Small daughtercard

Conventional, 10 mil thick spacing, 2 plane pairs

Thin layer, 2 mil thick, 4 plane pairs


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**Reduced Switching Noise**

![Graph showing reduced switching noise](image)

Reduces SSO noise

Improves effectiveness of the decoupling caps

Fig. 7. Dependence of $V_{pp}$ peak-noise amplitude on number of discrete capacitors mounted on sub-board.

Fig. 8. Relationship between number of simultaneous switching gates and $V_{pp}$ peak-noise amplitude.
Reducing Emissions:
Low Impedance Power and Ground Layers by
Thinner Dielectric

![Graph showing emission reduction with conventional separation vs. ZBC layers with small separation.]

*Figure 10-22.* Emission reductions by thinner dielectric in the power and ground distribution using the ZBC layers from Hadco. Also shown is a cross section of the board with two pairs of ZBC layers.

Avoid Splits in Return Path

![Graph showing comparison of emissions with and without split in ground reference plane.]

Archambault, Bruce; "Proper design of intentional splits in the ground reference plane of PC Boards to minimize emissions from I/O wires and cables", Proc. 1998 IEEE conf. on EMC, p. 768

*Avoid all splits in the return path!*
Unintentional Splits

Figure 9. How a via field for a connector can create a gap. By decreasing the clearance hole diameter in the ground plane, a continuous return path can be provided.

Figure 10. Data from [10]. Left is the emission from a board with gaps under via fields- failing the Class A test. Right: the exact same board, but with smaller clearance holes and no gaps under traces- passing Class A test.

The Design Strategy

1. Use design guidelines as design guidelines to shoot for
2. Estimate the magnitude of each effect and the benefit from a design or technology solution
3. Verify the models and simulations based on measurements of test vehicles and previous designs
4. Evaluate cost/performance trade offs
5. Keep optimizing until the noise budget is met
6. The earlier in the design cycle correct design decisions can be made, the shorter time to market and lower the development cost
MYTHS
SI Problems Apply Across ALL Interconnects

BOLData Corp

Courtesy of ICE

“There are two kinds of design engineers, those that have signal integrity problems, and those that will”

Good Luck!