Electrical-, protocol- and application layer validation of MIPI D-PHY and M-PHY designs

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Digital Test Division
Agilent Technologies
Agenda

Introduction, Smart Device Overview
MIPI Interfaces in Smart Devices
Validating MIPI Interfaces
Outlook
Smart Devices Overview

Many potential form factors!
Features of Smart Devices

Internet, eMail, Organizer, Phone

- Wireless (WLAN, UMTS, LTE, ...)

Imaging, Photo, Video, Movies

- High resolution Camera and Display

Audio, Music

- MP3, WMA, AAC, ...

Maps

- GPS, aGPS

Book Reading

Gaming
Mobile (Smart) Device Evolution

- CDMA EV-DO/WCDMA (~2.4Mbps) → HSDPA (~14.4Mbps) → LTE (~300Mbps)
- WiFi (~54Mbps) → WiMAX/WiBro (~70Mbps)

Source: Website (1Q'08)
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Technology Challenges in Mobile Computing

Too Many Interfaces, All Different

- Videophone camera
- Storage system
- Auxilary connectivity
- Megapixel camera
- Background microphone
- Primary microphone
- Analog
- Digital
- Main Display
- Caller ID Display
- Multi-band cellular transceiver
- Loudspeaker
- Earpiece speaker
- Power management functions
MIPI Interfaces in a Mobile Platform

This picture is only an illustrative example for several ways of integration with the purpose of demonstrating MIPI diversity on interfaces.

- **UniPort**
- **UniPro™ + D-PHY or M-PHY**

UniPro based IF technology are:
- UFS, CSI-3, DSI-2, GBT, UniPort

(*) Transferred to IEEE
(**) Liaison with JEDEC
## Physical / Protocol / Application Support

**MIPI**
Mobile industry processor Interface

### Application

<table>
<thead>
<tr>
<th>Protocol Standard</th>
<th>CSI camera Interface</th>
<th>DSI Display Interface</th>
<th>DigRF v3</th>
<th>DigRF v4</th>
<th>Next Gen CSI / DSI</th>
<th>UFS</th>
<th>LLI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical Standard</td>
<td>D-PHY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Next Gen CSI / DSI
Unipro

M-PHY
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What is MIPI D-PHY?

MIPI D-PHY is a Serial Bus

Mobile Display
Mobile Camera
Mobile Controller

Why use MIPI D-PHY?

- **Standard Bus**: Facilitates Integration and Interoperability
- **Performance**: up to 4Gbs for high resolution camera and displays
- **Low power and high Scalability**: Multilane architecture

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MIPI D-PHY Characteristics

Data Lanes

• High Speed Mode 80Mbps - 1Gbps
• May go up to 1.5 Gbps in the future
• Low Power Mode < 10Mbps
• Bidirectional

Lane Scalability

• Up to 4 Lanes + 1 clock lane

Power

• Low Operational power
• Very Low Standby power
Anatomy of a MIPI D-PHY link

A MIPI D-PHY Link includes:

- 1 clock lane
- 1 or multiple Data lanes (all lanes are differential)

2 data lanes MIPI D-PHY Link Example

*Master drives the clock*
MIPI D-PHY at the Physical Layer

Dual Signaling for high speed and low power transmission

Dynamic termination
MIPI D-PHY Signals
MIPI DPhy DSI/CSI-2 Short Packet Structure

**Note:** The packet structure is identical for DSI and CSI-2. The difference is the interpretation of the Data ID field.

**Data Identifier:** Contains the Data Type Information (Short vs. Long) denotes the format/content of the Payload Data.

**8-bit Correction Code:** 8-bit ECC code for the Packet Header. Allows 1-bit error correction and 2-bit error detection.
16-bit Word Count (WC): The receiver reads the next WC data words independent of value. The receiver uses the WC value to determine the End of Packet.

Application Specific Payload

32-bit PACKET HEADER (PH)

PACKET DATA: Length = Word Count (WC) * Data Word Width (8-bits). There are NO restrictions on the values of the data words

16-bit PACKET FOOTER (PF)
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- M-PHY Overview

Validating MIPI Interfaces

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## Main properties of M-PHY

<table>
<thead>
<tr>
<th>Main LANE characteristics</th>
<th>2 pins/wires, differential, unidirectional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum composition</td>
<td>Dual-simplex (4 wires)</td>
</tr>
<tr>
<td>Media</td>
<td>0-30 cm PCB, micro coax</td>
</tr>
<tr>
<td></td>
<td>&lt;1.2 m cable</td>
</tr>
<tr>
<td></td>
<td>optical waveguides</td>
</tr>
<tr>
<td>Clocking method</td>
<td></td>
</tr>
<tr>
<td>HS</td>
<td>Embedded clock (8b10b)</td>
</tr>
<tr>
<td></td>
<td>with or without shared RefClk</td>
</tr>
<tr>
<td>LS</td>
<td>PWM: Self-clocking</td>
</tr>
<tr>
<td></td>
<td>SYS: Synchronous to RefClk</td>
</tr>
<tr>
<td>Raw bitrates (8b10b coded)</td>
<td></td>
</tr>
<tr>
<td>HS</td>
<td>1¼ &amp; 1½, 2½ &amp; 3 , 5 &amp; 6 Gb/s</td>
</tr>
<tr>
<td>LS</td>
<td>PWM: 10 kb/s-600 Mb/s</td>
</tr>
<tr>
<td></td>
<td>SYS: RefClk rate</td>
</tr>
<tr>
<td>RefClk frequencies</td>
<td>19.2 / 26 / 38.4 / 52 MHz</td>
</tr>
<tr>
<td>Data BURST encoding</td>
<td>8b10b</td>
</tr>
<tr>
<td>Power efficiency (overall)</td>
<td>&lt;10pJ per payload-bit</td>
</tr>
<tr>
<td>CDR at receive side</td>
<td>Yes for HS, No for LS(-only)</td>
</tr>
<tr>
<td>TX pre-emphasis / RX equalization</td>
<td>No / Not specified</td>
</tr>
<tr>
<td>Signal levels (supply independent!)</td>
<td>0 - 200mV_{RT} - 400mV_{NT} (large drive)</td>
</tr>
<tr>
<td></td>
<td>0 - 100mV_{RT} - 200mV_{NT} (small drive)</td>
</tr>
<tr>
<td>Configuration</td>
<td>Using protocol &amp; PHY mechanisms</td>
</tr>
</tbody>
</table>
Layered Interface Standards

Applications:

- DigRF v4
- UniPRO
  - CSI / DSI / UFS / GBT
- LLI

M-PHY Scope

M-PHY

PHY-Adapter

Application Specific Protocol Part

Application Agnostic Protocol Part

M-PHY

M-TX M-RX

Di Do
Electrical signal characteristics

- Only low-swing differential signaling
- TX always provides LINE termination
- Switchable RX line termination: operation with or without termination
- RX can hold undriven LINE at ‘differential-zero’ with Z_{HI} impedances
- Two different TX drive strengths: Large & Small (=Large/2)
- Optional Slew-Rate Control for EMI reduction
Bit signaling schemes

NRZ
- Non-Return-to-Zero (Trivial)

PWM
- Pulse-Width-Modulation
- Self-Clocking
## Comparison of D-PHY with M-PHY

<table>
<thead>
<tr>
<th></th>
<th>D-PHY</th>
<th>M-PHY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. number of pins per direction</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Minimum configuration</td>
<td>only unidir or half-duplex</td>
<td>dual-simplex=full-duplex</td>
</tr>
<tr>
<td>Minimal UniPRO configuration</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Medium</td>
<td>&lt;30 cm PCB, flex, micro coax</td>
<td>&lt;30 cm PCB, flex, micro coax, &lt;1.2 m cable, optical</td>
</tr>
<tr>
<td>Data rate per lane</td>
<td>HS: &gt;80 Mb/s (Practical limit &lt;1Gb/s), &lt; 10 Mb/s</td>
<td>LP: ~ 1⅓, 2⅓, 5 Gb/s, ~ 1½, 3, 6 Gb/s, 10k-600Mb/s</td>
</tr>
<tr>
<td>Electrical signaling</td>
<td>HS: SLVS-200, LVCMOS1.2V</td>
<td>LP: SLVS-200 w/o RX-R_T</td>
</tr>
<tr>
<td>HS Clocking method</td>
<td>DDR Source-Sync Clk</td>
<td>Embedded Clk</td>
</tr>
<tr>
<td>HS Line coding</td>
<td>None or 8b9b</td>
<td>8b10b</td>
</tr>
<tr>
<td>Power – Energy/bit</td>
<td>Low</td>
<td>Lower</td>
</tr>
<tr>
<td>Receiver CDR required</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Suited for optical transmission</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>LP only PHY's</td>
<td>Disallowed</td>
<td>Allowed</td>
</tr>
</tbody>
</table>
DigRF V4 Overview

DigRF v4 is the next generation link between the BB-IC and RF-IC in a mobile device, enabling LTE and WiMAX data rates.

Bus between BB-IC and RF-IC must support high traffic flows.

4G standards (LTE, WiMAX) enable downlink speed of over 300 MBit/s.

DigRF V4 is an enabling technology for LTE and WiMAX Applications.
UniPro Overview

- D-PHY and M-PHY
- High Scalable Bandwidth with low pin-count
- Low power consumption
- Reliable packet based, latency-aware Traffic Classes
- Network architecture
- Connection management
- Device discovery
- Remote configuration
- Security

Layered Model of UniPro v1.5

*MIPI D-PHY or MIPI M-PHY
Low Latency Interface (LLI) Overview

The LLI interface allows sharing a DRAM memory between 2 chips for data and program. The main motivation for LLI is cost reduction.

The LLI specification defines several logical layers to help to make the specification more understandable:

• Transaction layer: exchanges memory mapped read/write transactions and signals between 2 chips.
• Data link layer: provides several independent virtual channels between the 2 chips.
• PHY adapter layer: provides an interface to the physical media. Focus first on serial MIPI M-PHY. Ensure reliability as necessary.
• Power management. Interface control for optimal power consumption; definition of the power states.
• Boot and reset
• Test
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Test Applications

Electrical Layer
• TX & RX Compliance (Scope & Generator (BERT))
• BringUp & Debug (Scope)

Protocol & Application Layer
• Protocol Compliance (Protocol Exerciser / Analyzer)
• BringUp & Debug (Protocol analyzer or Scope)
• Device Emulation (Protocol Exerciser)
• Performance Validation (Protocol Exerciser)
• Application testing (Software Add-ons for Protocol exerciser)
How to electrically test an RX

Bit Error Ratio Test Principle

Data Source Generator → RX → Expected Data

Compare → Errors

Data Analyzer Error Detector

Bit Error Ratio Tester (BERT)
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Agilent D-PHY Physical Layer Test Solution
Integrated Rx and Tx Test Setups
MIPI D-PHY Protocol Test System configuration

Protocol Stimulus and Analysis

N4851B Analysis Probe
- Speed: up to 1Gbps per lane
- 4 lanes support
- Flying leads or soft touch
- Full Protocol Triggering
- Real time error detection
- CSI & DSI packet viewer
- High Speed and Low power mode

N4861B Stimulus Probe
- Speed: 1Gbps per lane
- 3 lanes support
- CSI & DSI stimulus generation
- Error injection
- Voltage control
- Timing control
- High Speed and Low power mode

Notes:
- Loopback board orderable N4850-66402 for around $750.
- Dynamic termination board available from UNH-IOL.

All LA modules Except 16962A

16720A pattern Generator module

Logic analyzer pods

Pattern generator cables

SMA cables

DUT

E5381A differential flying lead probe

N4851B acquisition probe

N4861B stimulus probe

Samtec probes

Pattern generator cables

All LA modules Except 16962A

16720A pattern Generator module

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Test Model #1: Camera Sensor Test

**Functional Analysis**

- Capture Traffic in real-time
- Protocol Level Trigger and Display
- Real-time Errors detection
- Compliance test

**Notes:**
- Analyzer operates in high impedance mode
- Dynamic Termination required on target System
- Camera= bus Master
Test Model #2: Display Module Evaluation

Functional Stimulus and Analysis

- DSI Packet & Image View
- Logic Analyzer
- Real-time capture of Bus activity

Initialization Commands
Data File

Send Stimulus to Display Device

N4861B
MIPI D-PHY DSI

N4851B
Display

Notes:
- Dynamic Impedance required on target system if bus-turn around
Test model #3: Camera Emulation

Functional Analysis

Challenge: simulating various CSI devices
Generate Real-time CSI traffic
1Gbps on 3 lanes
Capture and replay
Test model #4 : Controller, Display & Camera Integration

Oscilloscope
Logic Analyzer
Packet View

ViewScope for cross triggering and time correlated measurement
Protocol Analysis

Initialization commands
Sync Events
Delta Time critical
Data Traffic
Long packets (Pixel Stream)

Low Level view of the packets
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Various knowledge/techniques are required for DigRF analysis. In particular there are new high speed digital physical layer and protocol level testing and validation required.
Receiver Test With BERT Generator and BERT Error Detector

Focus on receiver characterization and R&D level debugging

Utilizes the line loopback mode

Test pattern: all kinds of test pattern supported
Receiver Test With BERT Generator and DigRFv4 Exerciser

Receiver characterization and system timing stress test

Utilizes the logic loopback mode with additional limited support for line loopback

Test pattern:
DigRF4 commands with payload and checksum in logic loopback mode, and PRBS 7 and PRBS 15 in line loopback mode
Digital Signal Integrity Evaluation

DigRF evaluation begins with the digital physical layer evaluation. Digital quality is tied directly to the final RF quality.

Preliminary Compliance test with UDA
DigRF v3/v4 RF-IC Unit Testing Environment

Signal Studio Software

Signal Generator

N5343A Exerciser

Vector Signal Analysis

Spectrum Analyzer

Modulation Analysis and C/N Measurement
RF-IC, BB-IC, Integration Testing Environment

- DigRF
- Signal Generator
- Signal Studio Software
- Vector Signal Analysis

Diagram:
- RF-IC
- BB-IC
- DSP
- uC
- Digital
- Vis Port
- RF-IC
- DigRF v3.xx
- RF
- Oscilloscope
- Signal Analyzer
- Vector Signal Analysis
- DigRF Packet Analysis

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What will happen in 2011 / 2012?

D-PHY evolving towards 1.3 .. 1.5 Gbit/s bandwidth
M-PHY Gear 2 followed by Gear 3
3D support for Display and Camera
CSI-3, DSI-2 and UFS on UniPro 1.4 / M-PHY Gear 2
Low Latency Interface 1.0

- UniPro based applications and LLI will require protocol aware stimulus as both protocols are implementing real-time handshaking.
- Agilent will ensure appropriate test equipment availability at the right time.
Do you have any questions?