Advanced Techniques for Validating PCI Express® 4.0 Transmitters and Receivers

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Principal PCIe Tools Planner
Keysight Technologies
Agenda

– PCIe 4.0 Ecosystem and Timeline
– PCIe 4.0 TX Testing and Tools
– RX Testing and Link/EQ
– PCIe Gen5
PCle Ecosystem

PCISIG Board of Directors

Intel, AMD, IBM, Synopsys, Qualcomm, Dell, HP, NVIDIA, Lenovo

- Electrical Work Group
  - Electrical Spec
    - AMD, Intel

- Protocol Work Group
  - Protocol Spec
    - AMD, Intel

- Card Electromechanical Work Group
  - CEM Spec
    - Intel

- Serial Enabling Work Group
  - Test Specification & Plugfests
    - Intel, Synopsys

PCI Express 4.0

Deliverables:

Group Chairs:

- Electrical Work Group: AMD, Intel
- Protocol Work Group: AMD, Intel
- Card Electromechanical Work Group: Intel
- Serial Enabling Work Group: Intel, Synopsys
PCle Ecosystem

Intel, AMD, IBM, Synopsys, Qualcomm, Dell, HP, NVIDIA, Lenovo

Electrical Spec
AMD, Intel

Protocol Spec
AMD, Intel

CEM Spec
Intel

Test Specification & Plugfests
Intel, Synopsys

PCI Express 4.0

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Group Chairs:

- AMD, Intel
- AMD, Intel
- Intel
- Intel, Synopsys

PCISIG Owned
- Oculink
- Cabled PCIe
- mPCI (MIPI.org)

Non-PCISIG Owned
- CCIX
- SATA Express
- NVMe

M.2 (SATA, USB, PCI-E)

U.2 (SFF-8639)

PCISIG Owned FFs

Keysight Technologies 2018
PCI Express Specifications and Scope

Select the specifications that relate to your need

- **Base Specification**
  - Contains all the system knowledge
  - Can directly be applied to Chip Test

- **Card Electromechanical (CEM) Spec**
  - Applies to Add-In Cards and Mother Boards
  - Mitigates card manufacturer’s need to study the base specification
  - Increases reproducibility through PCI-SIG supplied test tools CBB and CLB (compliance base and load board)

- **Phy Test Specification**
  - Defines compliance tests of CEM spec in detail
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Now Released at v1.0
PCIe 4.0 New Features
Based on PCIe v0.7 BASE specification

- New data rate: 16GT/s
  - Requires an output stages capable of providing pre-shoot and de-emphasis with fast enough rise-times.

- Link Equalization protocol similar to PCIe 3.0
  - TxEQ P0-P10
  - RxEQ CTLE (2 pole 1 zero) + 2tap DFE

- Max Channel Length -28dB @ 8GHz & 1 connector
  - Re-timers used for longer channels or for channels with >1 connector

- RX clocking architectures: CC and IR
  - CC -> Common RefClock -> synchronous RX and TX w/ or w/o SSC
  - IR -> Independent RefClock -> asynchronous RX and TX w/ or w/o SSC

- Initial LinkEQ speed selection: 2.5GT/s -> 8GT/s with link equalization
  - if successful -> Then transitions to 16GT/s with another round of link equalization

- TX Jitter Analysis: Similar to PCIe 3.0

- Lane Margining added.
PCI Express® 4.0 – Keysight Total Solution

Physical layer – interconnect design
- ADS design software
- 86100D DCA-X/TDR
- E5071C ENA option TDR

Physical layer-transmitter test
- V-Series, Z-Series Real-Time Oscilloscopes
- N5393F PCI Express 4.0 TX Electrical compliance software
- 86100CU-400 PLL and Jitter Spectrum Measurement SW

Physical layer-receiver test
- M8020A J-BERT High Performance, Protocol Aware BERT
- N5990A automated compliance and device characterization test software
- DSA V-series & Z-Series Real-Time Oscilloscopes
- Automated RX Test software - Accurate, Efficient - Comprehensive RX Testing

Verify PCIe 4.0 Compliant Channels
Verify Return Loss Compliance

Keysight 2018
CEM 4.0 and Compliance Testing

- CEM 4.0 currently at v0.7.
  - V0.7 (Latest doc Oct 2, 2017)
- PCIe 4.0 Compliance Requirements
  - CEM Spec completion at v0.7 (v0.9 optimal)
  - Completion of Test Specifications
    - Config Test Spec
    - Link Transaction Test Spec
    - System Firmware (BIOS) Test Spec
    - Electrical Test Spec
    - Retimer Test Spec
- Availability of Gen4 Compliance Test Fixtures for Purchase
  - Preliminary PCIe 4.0 Test Fixtures tested at April & Aug 2017 Workshops
- Estimated Schedule
  - First Gen4 FYI testing commenced April 2017
  - Official FYI Testing to begin in 2018
  - Official Integrators list to follow.
PCle 4.0 TX Testing
9.3.5.2 De-embedding

Direct probing at a transmitter’s pins is not generally feasible, so data is instead measured at TP1 of the breakout channel. By means of the replica channel it is possible to determine the loss vs. frequency characteristics of the breakout channel and de-embed this channel, resulting in measurements that are effectively referenced to the DUT’s pins. Note that since de-embedding amplifies HF noise, there is a practical frequency cutoff limit to de-embedding. As de-embedding amplifies HF channel and measurement noise, an HF cutoff limit of 8GHz-12GHz and 20 GHz (3dB point) must be applied to de-embedding, depending on data rate. See the table below.

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>HF Cutoff limit for de-embedding</th>
</tr>
</thead>
<tbody>
<tr>
<td>8GT/s</td>
<td>8GHz-12 GHz</td>
</tr>
<tr>
<td>16GT/s</td>
<td>20GHz</td>
</tr>
</tbody>
</table>

Jitter is decomposed into data dependent and uncorrelated terms. This separation process effectively separates the jitter caused by package effects from that caused by signal integrity effects. As a result the uncorrelated jitter terms define jitter as it would appear at the die pad.

9.4.2.1 Procedure for Calibrating a Stressed EH/EW Eye

Note: As the calibration procedure of the signal generator is connected directly to measurement instrumentation, the output waveform can be very fast. Therefore, it is important that the bandwidth be matched appropriately to the edge rate of the generator output. This specification requires the use of a generator whose outputs have a rise time of 17ps-19ps (80% / 20%) which also requires a minimum oscilloscope bandwidth of 25GHz. This oscilloscope bandwidth is also the minimum required bandwidth for transmitter measurements.
PCI Express 4.0 TX Measurement Basic Test Setup
BASE Spec (v0.7)

PCIe 4.0 ASIC/IC Custom Breakout Board

Keysight Z-Series Real Time Oscilloscope

S-Parameters of Replica Ch. Used to de-embed to pin or Ref CTLE can be used (12dB).
N5393F/G New Features

- Supports PCIe 4.0 BASE TX Testing at 2.5G, 5G, 8G and 16GT/s (v0.7 BASE)
- Supports PCIe 4.0 Reference Clock tests (2.5G, 5G, 8G, 16G)
- Supports U.2 (SFF-8639) CEM tests for endpoints and root complexes (2.5G, 5G, 8G).
- Automated DUT control using an 81150/60A Pulse Generator ARB.
- Enhanced Switch Matrix supporting arbitrary lane mapping
- New “Workshop Compliance Mode” for rapid PCISIG official compliance testing.
New Test Plan Setup

Select Standard Version to Test

Automatic DUT control for toggle signal

Select Speeds of Gen4 Device to Test
Select a complete Gen4 TX test plan.
Use InfiniiSim for de-embedding with optional N5465A

Select InfiniiSim under “Tools”

Choose your de-embed transfer function

Fine-tune your de-embed filter (bandwidth, etc)
### Consolidated Jitter Parameters for ALL data rates

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter description</th>
<th>2.5 GT/s</th>
<th>5.0 GT/s</th>
<th>8.0 GT/s</th>
<th>16.0 GT/s</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTX-BOOST-RS</td>
<td>Maximum nominal Tx boost ratio for reduced swing</td>
<td>N/A</td>
<td>N/A</td>
<td>2.5</td>
<td>~2.5 (min)</td>
<td>dB</td>
<td>Assumes ±1.0 dB tolerance from diagonal elements in Table 9-3.</td>
</tr>
<tr>
<td>EQ-TX-COEFF-RES</td>
<td>Tx coefficient resolution</td>
<td>N/A</td>
<td>N/A</td>
<td>1/24 (max)</td>
<td>1/63 (min)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTX-DE-RATIO-3.6G</td>
<td>Tx de-emphasis ratio for 2.5 and 5 G</td>
<td>3.0 (min)</td>
<td>3.0 (min)</td>
<td>N/A</td>
<td>N/A</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>VTX-DE-RATIO-6G</td>
<td>Tx de-emphasis ratio for 5 G</td>
<td>5.5 (min)</td>
<td>6.5 (max)</td>
<td>N/A</td>
<td>N/A</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>TTX-UTJ</td>
<td>Tx uncorrelated total jitter</td>
<td>100 (max)</td>
<td>50 (max)</td>
<td>31.25 (max)</td>
<td>12.5 (max)</td>
<td>ps PP at 10-12</td>
<td>See Sec 9.3.5.8 for details.</td>
</tr>
<tr>
<td>TTX-UTJ-SRIS</td>
<td>Tx uncorrelated total jitter when testing for the IR clock mode with SSC</td>
<td>100 (max)</td>
<td>66.51 (max)</td>
<td>33.83 (max)</td>
<td>15.85 (max)</td>
<td>ps PP at 10-12</td>
<td>See Sec 9.3.5.8 for details.</td>
</tr>
<tr>
<td>TTX-UDJDD</td>
<td>Tx uncorrelated Dj for non-embedded Refclk</td>
<td>100 (max)</td>
<td>30 (max)</td>
<td>12 (max)</td>
<td>6.25 (max)</td>
<td>ps PP</td>
<td>See Sec 9.3.5.8 for details.</td>
</tr>
<tr>
<td>TTX-UPW-TJ</td>
<td>Total uncorrelated pulse width jitter</td>
<td>N/A</td>
<td>40 (max)</td>
<td>24 (max)</td>
<td>12.5 (max)</td>
<td>ps PP at 10-12</td>
<td>See Sec 9.3.5.9 for details</td>
</tr>
<tr>
<td>TTX-UPWDJDD</td>
<td>Deterministic DjDD uncorrelated pulse width jitter</td>
<td>N/A</td>
<td>40 (max)</td>
<td>10 (max)</td>
<td>5 (max)</td>
<td>ps PP</td>
<td>See Sec 9.3.5.9 for details</td>
</tr>
<tr>
<td>TTX-RJ</td>
<td>Tx Random jitter</td>
<td>N/A</td>
<td>1.4 - 3.6</td>
<td>1.4 - 2.2</td>
<td>.45 - .89</td>
<td>ps RMS</td>
<td>Informative parameter only. Range of Rj possible with zero to maximum allowed TTX-UDJDD.</td>
</tr>
<tr>
<td>LTX-SKEW</td>
<td>Lane-to-Lane Output Skew</td>
<td>2.5 (max)</td>
<td>2.0 (max)</td>
<td>1.5 (max)</td>
<td>1.25 (max)</td>
<td>ns</td>
<td>Between any two Lanes within a single Transmitter.</td>
</tr>
<tr>
<td>RL-TX-DIFF</td>
<td>Tx package plus die differential return loss</td>
<td>See Figure 9-19</td>
<td>See Figure 9-19</td>
<td>See Figure 9-19</td>
<td>See Figure 9-19</td>
<td>dB</td>
<td>Note 6</td>
</tr>
<tr>
<td>RL-TX-CM</td>
<td>Tx package plus die common mode return loss</td>
<td>See Figure 9-20</td>
<td>See Figure 9-20</td>
<td>See Figure 9-20</td>
<td>See Figure 9-20</td>
<td>dB</td>
<td>Note 6</td>
</tr>
</tbody>
</table>

**Note Gen1, Gen2 Jitter now has same measurement parameter as Gen3/4 but different values.**
PCle 4.0 Reference Clock Testing
### PCIe 4.0 Reference Clock AC Parameters

#### Table 2-1: REFCLK DC Specifications and AC Timing Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>100 MHz Input</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td></td>
</tr>
<tr>
<td>Rising Edge Rate</td>
<td>Rising Edge Rate</td>
<td>0.6</td>
<td>4.0</td>
<td>V/ns</td>
</tr>
<tr>
<td>Falling Edge Rate</td>
<td>Falling Edge Rate</td>
<td>0.6</td>
<td>4.0</td>
<td>V/ns</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>Differential Input High Voltage</td>
<td>+150</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Differential Input Low Voltage</td>
<td>-150</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>V\text{CROSS}</td>
<td>Absolute crossing point voltage</td>
<td>+250</td>
<td>+550</td>
<td>mV</td>
</tr>
<tr>
<td>V\text{CROSS DELTA}</td>
<td>Variation of V\text{CROSS} over all rising clock edges</td>
<td>+140</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>V_{RB}</td>
<td>Ring-back Voltage Margin</td>
<td>-100</td>
<td>+100</td>
<td>mV</td>
</tr>
<tr>
<td>T\text{STABLE}</td>
<td>Time before V_{RB} is allowed</td>
<td>500</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>T\text{PERIOD AVG}</td>
<td>Average Clock Period Accuracy</td>
<td>-300</td>
<td>+2800</td>
<td>ppm</td>
</tr>
<tr>
<td>T\text{PERIOD ABS}</td>
<td>Absolute Period (including Jitter and Spread Spectrum modulation)</td>
<td>9.847</td>
<td>10.203</td>
<td>ns</td>
</tr>
<tr>
<td>T\text{CJITTER}</td>
<td>Cycle to Cycle jitter</td>
<td>150</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>V\text{MAX}</td>
<td>Absolute Max input voltage</td>
<td>+1.15</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V\text{MIN}</td>
<td>Absolute Min input voltage</td>
<td>-0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>Duty Cycle</td>
<td>40</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>Rise-Fall Matching</td>
<td>Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching</td>
<td>20</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Z_{DC}</td>
<td>Clock source DC impedance</td>
<td>40</td>
<td>60</td>
<td></td>
</tr>
</tbody>
</table>

**Diagram:**

-15dB loss at 4 GHz

DUT

Refclk Generator

Differential PCB trace Z_{DIFF} = 100Ω ±10%

2.0pF

Refclk Margins
9.6.7 Jitter Limits for Refclk Architectures

Table 9-18 lists the jitter limits for the CC Refclk architecture at each of the four data rates. Jitter at 2.5 GT/s is measured as a peak to peak jitter value, because a substantial proportion of the jitter is SSC harmonics which appears at the receiver as Dj. The combination of the 2.5 GT/s PLL and CDR bandwidths passes a significant amount of SSC residual, where it appears Dj. The 108 ps number is the same as that specified in the 3.0 CEM spec.

For 5.0, 8.0, and 16.0 GT/s jitter is specified as an RMS (Rj) value. These signaling speeds utilize a lower PLL BW and a higher CDR BW, and the effect is to suppress SSC harmonics such that almost all the jitter appears as Rj.

Table 9-18: Jitter Limits for CC Architecture

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>CC Jitter Limit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5G</td>
<td>108 ps pp</td>
<td>1, 2</td>
</tr>
<tr>
<td>5.0G</td>
<td>3.1 ps RMS</td>
<td>1, 2</td>
</tr>
<tr>
<td>8.0G</td>
<td>1.0 ps RMS</td>
<td>1, 2</td>
</tr>
<tr>
<td>16G</td>
<td>0.5 ps RMS</td>
<td>1, 2</td>
</tr>
</tbody>
</table>

Note that .7 ps RMS is to be used in channel simulations to account for additional noise in a real system.

Note:
1. The Refclk jitter is measured after applying the filter function in Figure 9-45.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real time oscilloscope with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement.
## Reference Clock for Gen4

### Table 9-17: Common Refclk PLL and CDR Characteristics for 8.0 and 16.0 GT/s

<table>
<thead>
<tr>
<th>PLL #1</th>
<th>0.01 dB peaking</th>
<th>1.0 dB peaking</th>
<th>PLL #2</th>
<th>0.01 dB peaking</th>
<th>3.0 dB peaking</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW&lt;sub&gt;PLL(min)&lt;/sub&gt; = 5.0 MHz</td>
<td>(\omega_n = 1.12) Mrad/s (\zeta_1 = 14)</td>
<td>(\omega_n = 11.01) Mrad/s (\zeta_1 = 1.16)</td>
<td>BW&lt;sub&gt;PLL(min)&lt;/sub&gt; = 8.0 MHz</td>
<td>(\omega_n = 1.79) Mrad/s (\zeta_2 = 14)</td>
<td>(\omega_n = 26.86) Mrad/s (\zeta_2 = 0.54)</td>
</tr>
<tr>
<td>BW&lt;sub&gt;PLL(max)&lt;/sub&gt; = 16 MHz</td>
<td>(\omega_n = 3.58) Mrad/s (\zeta_1 = 14)</td>
<td>(\omega_n = 35.26) Mrad/s (\zeta_1 = 1.16)</td>
<td>BW&lt;sub&gt;PLL(max)&lt;/sub&gt; = 16 MHz</td>
<td>(\omega_n = 3.58) Mrad/s (\zeta_2 = 14)</td>
<td>(\omega_n = 53.73) Mrad/s (\zeta_2 = 0.54)</td>
</tr>
</tbody>
</table>

**BW<sub>CDR(min)</sub>** = 5 MHz, **1st order**

64 combinations

### REF Clock 8G TX Phase Jitter

<table>
<thead>
<tr>
<th>PLL1</th>
<th>PLL2</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATX</td>
<td>ATX</td>
</tr>
<tr>
<td>BTX</td>
<td>BTX</td>
</tr>
<tr>
<td>CTX</td>
<td>CTX</td>
</tr>
<tr>
<td>DTX</td>
<td>DTX</td>
</tr>
<tr>
<td>ARX</td>
<td>ARX</td>
</tr>
<tr>
<td>BRX</td>
<td>BRX</td>
</tr>
<tr>
<td>CRX</td>
<td>CRX</td>
</tr>
<tr>
<td>DRX</td>
<td>DRX</td>
</tr>
</tbody>
</table>

- 0.3 ps
- 7.9 ps
- 0.99 ps

If user right clicks on a curve, pop up menu shows curves related to the calculation of that value.

Color code fields for PASS/Fail/Margin

Report Results in a Matrix

Show Spec in Report
Gen4 Reference Clock Tests

- Common 100MHz AC Parameters
- Phase Jitter tests for 2.5G, 5G, 8G, and 16G
- SSC Clock Tests
Speeding up Testing

▪ Automated DUT Control
▪ Enhanced Switch Matrix Lane Mapping
▪ Workshop Compliance Mode
For use with PCIe 3.0 and below.

Keysight PCIe 4.0 (Gen4) TX N5393F Test Application

Use and 81150A or 81160A to generate the CBB Compliance Toggle signal to toggle your DUT between the different compliance states.

Control DUT automatically to switch compliance toggle modes.

Workshop compliance mode is used for PCISIG compliance testing and uses Sigtest to test your DUT as well as to create PCISIG Compliance test reports.

You specify what directory to use for your Workshop Compliance Mode (Sigtest generated) HTML reports along with data files.
Transmitter Test at 16 GT/s

Implications for testing

- PCIe @ 2.5GT/s
  - ✓ -3.5dB

- PCIe @ 5GT/s
  - ✓ -3.5dB
  - ✓ -6 dB

- PCIe @ 8GT/s
  - ✓ De-emphasis Presets P0-P10 (11)
    - ✓ De-emphasis, preshoot, boost for each preset
  - ✓ Signal Quality for at least 1 preset must pass

- PCIe @ 16 GT/s
  - ✓ De-emphasis Presets P0-P10 (11)
    - ✓ De-emphasis, preshoot, boost for each preset
  - ✓ Signal Quality for at least 1 preset must pass

- X16 lanes (592 test cases possible)
Choose from available switch matrix options for multi-lane testing.

Lanes to test can be chosen arbitrarily.

If you don’t have a switch, you can test using all four scope channels to test two lanes with one setup.

Select Lanes to map to your switch network setup.
Keysight PCIe 4.0 (Gen4) TX N5393F Test Application

Test Automation and Connection Example

81150A used for DUT control (toggle pulse to switch compliance states)

Scope configured for Root Complex Testing

Root Complex DUT being tested for PCISIG Compliance

Keysight U3020A Switch Matrix
PCle 4.0 CEM Testing
CEM AIC Modifications

– Support of 16GT/s is possible with legacy PCIe 3.0 CEM Connector

– Modifications are required in order to ensure optimal signal integrity of the combined CEM Edge Finger and CEM Connector system.

– Add-in Card Edge Modifications for PCIe 4.0
  • Lower ground vias
  • Tie double grounds together
  • Resistive Termination of Side-band signals on AIC (required)

– System Board Modifications
  • Sentry vias per sideband pin (minimum of 2)
Example of Sideband Termination

AC Sideband Termination per 4.0 CEM Spec are ~43 ohms and 1pF

Sideband termination on root complex side is optional.
Note: This TX test proposal utilizes an external variable ISI board to ensure consistent insertion loss of the test setup.
CEM TX Test Setups

**PCle 4.0 (Add-in Card)**
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - Add-in Card plugs into CBB
  - 20dB at 8GHz of additional loss (including package embedding)
- **Power on CBB**
- **Scope bandwidth is 25GHz**
- **5dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Scope BW is set to 25GHz for CEM compliance**
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Time Domain CDR algorithm used to recover clock
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)

**PCle 4.0 (System)**
Tx Signal Quality Test at 16 GT/s

- **Channel Setup**
  - CLB plugs into system
  - 8dB at 8GHz of additional loss (including package embedding)
- **Power on System**
- **Scope bandwidth = 25GHz**
- **3dB package model embedded on scope**
- **Toggle DUT to transmit 16GT/s Compliance Pattern**
  - 1ms pulse of 100MHz clock signal into Rx Lane0
- **Scope BW is set to 25GHz for CEM compliance**
- **Capture 2.0M UI waveform for every Tx EQ Preset**
- **Waveforms post processed using SigTest**
  - Ref clock captured with data waveform and used for clock recovery
  - Behavioral Rx Equalization applied
  - Eye width & Eye height @ E-12
  - Each lane must pass SigTest analysis for at least one Tx EQ Preset
    - EW > 0.3UI (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
    - EH > 15mV (with TBD adjustment due to lack of cross-talk, etc. in test fixtures)
CEM TX Test Setups

CBB4 Fixture

RX Lanes

Toggle Button

Toggle Circuit Output

TX Output for DUT
CEM TX Test Setups

CLB4 x4-x8 Fixture

- Toggle Button
- TX Output for X8
- Toggle Circuit
- TX Output for X4
CEM TX Test Setups

ISI Fixture
## CEM TX Test Setups
### AIC and Motherboard Test Channels

<table>
<thead>
<tr>
<th>Serial #</th>
<th>Configuration</th>
<th>Full Channel Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td>12</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td>22</td>
<td>System Tx</td>
<td>System DUT -&gt; CLB Tx -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
<tr>
<td></td>
<td>AIC Tx</td>
<td>AIC DUT -&gt; CBB Tx -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable</td>
</tr>
</tbody>
</table>
# CEM TX Test Setups

## AIC and Motherboard Test Channels Loss Calculation

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>1</th>
<th>12</th>
<th>22</th>
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</thead>
<tbody>
<tr>
<td>Short Trace</td>
<td>1.27</td>
<td>1.09</td>
<td>1.2</td>
</tr>
<tr>
<td>Long Trace</td>
<td>11.84</td>
<td>11.8</td>
<td>11.73</td>
</tr>
<tr>
<td>Loss/inch</td>
<td>1.057</td>
<td>1.071</td>
<td>1.053</td>
</tr>
<tr>
<td>SMA Female to SMP Female Cable</td>
<td>0.2225</td>
<td>0.2225</td>
<td>0.2225</td>
</tr>
<tr>
<td>Coaxial Launch 2x</td>
<td>0.825</td>
<td>0.645</td>
<td>0.755</td>
</tr>
<tr>
<td>CBB Tx &lt;-&gt; CLB Rx</td>
<td>9.78</td>
<td>10.05</td>
<td>10.08</td>
</tr>
<tr>
<td>Mated CEM Connector Loss</td>
<td>1.111</td>
<td>1.463</td>
<td>1.509</td>
</tr>
<tr>
<td>CBB Tx Loss</td>
<td>4.6945</td>
<td>4.9985</td>
<td>5.0455</td>
</tr>
<tr>
<td>CLB Tx Loss</td>
<td>2.5265</td>
<td>2.4645</td>
<td>2.4835</td>
</tr>
<tr>
<td><strong>AIC Tx</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CBB ISI (Desired)</td>
<td>10.3055</td>
<td>10.0015</td>
<td>9.9545</td>
</tr>
<tr>
<td>CBB ISI (Measured)</td>
<td>10.21</td>
<td>9.97</td>
<td>10.16</td>
</tr>
<tr>
<td>CBB ISI Pair</td>
<td>Pair 16</td>
<td>Pair 16</td>
<td>Pair 16</td>
</tr>
<tr>
<td><strong>System Tx</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLB ISI (Desired)</td>
<td>2.4735</td>
<td>2.5355</td>
<td>2.5165</td>
</tr>
<tr>
<td>CLB ISI (Measured)</td>
<td>2.5</td>
<td>2.51</td>
<td>2.51</td>
</tr>
<tr>
<td>CLB ISI Pair</td>
<td>Pair 0</td>
<td>Pair 0</td>
<td>Pair 0</td>
</tr>
</tbody>
</table>
CEM AIC TX Test Setup

Cabling from CBB4 to ISI Channel

Physical ISI Channel to achieve -17dB
PCle 4.0 Cable Suggestions

2.92 (SMA Compatible) Cables:
Huber-Suhner 85064115
INT SF104PE/11PC35/11PC35/1
Matched pair +/-1ps, ~1M length

12” SMP Cables:
80345501
Minibend L2SR-12PM±1PS
Minibend L SMP to SMP 12” length Delay matched 1ps

2.5” SMP to SMA cable:
80350960
32024E-29573CR29092CR-2.5PM±1PS
Minibend L SMP to SMA female 2.5” length Delay matched 1ps
Receiver Testing at 16 Gbps

>16 Gbps BERT

Link Equalization

Jitter and De-emphasis
# Differences between PCIe 3 and PCIe 4
## Relevant changes with PCIe 4.0 rev 0.5 and 0.7

<table>
<thead>
<tr>
<th>Feature</th>
<th>PCIe 3.0/3.1</th>
<th>PCIe 4.0 rev 0.5</th>
<th>PCIe 4.0 rev 0.7</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Added Transfer Rate</strong></td>
<td>8 GT/s</td>
<td>16 GT/s</td>
<td></td>
</tr>
<tr>
<td><strong>Coding</strong></td>
<td>128B/130B</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Block Alignment &amp; Scrambler Reset</strong></td>
<td>EIEOS for block alignment</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EIEOS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EIEOS</td>
<td>10 00FF 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 500 MHz</td>
<td>10 00FF 00FF 00FF 00FF 00FF 00FF 00FF ➔ 1 GHz</td>
<td>10 0000 FFFF 0000 FFFF 0000 FFFF ➔ 500 MHz</td>
</tr>
</tbody>
</table>

### Link EQ gets more important
- **Adaptable TX Link Equalization**: yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful
- **RX Tests**: one RX stress test
- **rSSC for Common Reference Clock**: no
  - **BER of 10⁻¹²**: 0.3 UI, 15 mV (RX eye spec. is actually 14 mV), BER of 10⁻¹²
  - **Stress Signal Adjustment**: coarse: ISI
    - fine: DM-SI + SJ or DM-SI + V_{diff}
- **Channel for RX Test**: PCIe 4.0 CEM connector required as part of RX test channel

### Different Cal Procedure
- **Reference CTLE Changes**: pole 1 frequency
  - 2 GHz
  - 4 GHz
  - 2 GHz

### Special Cal Channel Fixture Required
- **Channel for RX Test**: No connector required
## Differences between PCIe 3 and PCIe 4

### Relevant changes between PCIe 4.0 rev 0.5 to rev 0.7

<table>
<thead>
<tr>
<th></th>
<th>PCIe 3.0/3.1</th>
<th>PCIe 4.0 rev 0.5</th>
<th>PCIe 4.0 rev 0.7</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>added transfer rate</strong></td>
<td>8 GT/s</td>
<td>16 GT/s</td>
<td></td>
</tr>
<tr>
<td><strong>EIEOS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Scrambler reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Scrambling</td>
<td>control: no (partially), data: always</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PRBS 2³³⁻¹ scrambler reset through EIEOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>yes, two step process: first 8G link eq followed by 16G link eq if 8G link eq is successful</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>one RX stress test</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>rSSC for common reference clock</strong></td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Reference CTLE changes:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pole 1 frequency</td>
<td>2 GHz</td>
<td>4 GHz</td>
<td>2 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel for RX test</strong></td>
<td>No connector required</td>
<td>PCIe 4.0 CEM connector required as part of RX test channel</td>
<td></td>
</tr>
</tbody>
</table>
Dynamic Link Equalization Handshake 8G

The four phases of the Link Equalization Protocol

Phase 0:
- 2.5 Gb/s
- Downstream port tells upstream port which initial preset to use after the speed change will have been done.

Phase 1:
- 8 Gb/s
- Link partners settle on 8 GT/s speed.
- Exchange FS/LF values.

Phase 2:
- 8 Gb/s
- Add-in Card sets up the de-emphasis of the System Board’s transmitter.

Phase 3:
- 8 Gb/s
- System Board sets up the de-emphasis of the Add-in Card’s transmitter.

EQ starts
- Phase 0
  - TS1, [P2]
    - EC = 00b, PV = P2

- Phase 1
  - TS1, [P1]
    - EC = 01b, PV = P1, Use_Preset = 0

- Phase 2
  - TS1, [P2]
    - EC = 10b, PV = P3, Use_Preset = 1
  - BER < 10^{-12}
  - TS1, [P4]
    - EC = 10b, PV = P4, Use_Preset = 0

- Phase 3
  - TS1, [P3]
    - EC = 10b, PV = P3, Use_Preset = 0
  - TS1, [P6]
    - EC = 11b, PV = P6, Use_Preset = 1

EQ complete
- Phase 3
  - TS1, [P4]
    - EC = 11b, PV = P6, Use_Preset = 1

PV  Preset Value
EC  Equalization Control
Dynamic Link Equalization Handshake 16G

The four phases of the Link Equalization Protocol

<table>
<thead>
<tr>
<th>Phase 0</th>
<th>2.5 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Downstream port tells upstream port which initial preset to use after the speed change will have been done.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase 1</th>
<th>8 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link partners settle on 8 GT/s speed.</td>
<td></td>
</tr>
<tr>
<td>Exchange FS/LF values.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase 2</th>
<th>8 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add-in Card sets up the de-emphasis of the System Board’s transmitter.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Phase 3</th>
<th>8 Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Board sets up the de-emphasis of the Add-in Card’s transmitter.</td>
<td></td>
</tr>
</tbody>
</table>

**Phase 1:**
- 16 Gb/s
- Link partners settle on 16 GT/s speed.
- Exchange FS/LF values.

**Phase 2:**
- 16 Gb/s
- Add-in Card sets up the de-emphasis of the System Board’s transmitter.

**Phase 3:**
- 16 Gb/s
- System Board sets up the de-emphasis of the Add-in Card’s transmitter.

**IF SUCCESSFUL**

---

**PV** Preset Value
**EC** Equalization Control
- EIEOS needs to be set to PCIe3 for PCI Express Base Specification 4.0 rev 0.5. But for PCIe Base Specification 4.0 rev 0.7 and higher it needs to be set PCIe4!
- Generation needs to be set to PCIe Gen 4
- Select DUT type:
  - Any endpoint device ➔ Add In Card
  - Any root complex device ➔ System Board
- Two sets of phase 0 through phase 3 parameters
  - 2.5GT/s to 8GT/s
    - DUT Target Preset can be presets only
  - 8GT/s to 16GT/s
    - DUT Target Preset 4 can be presets or coefficients
- Speed Change Control:
  - While the root complex usually is responsible for initiating the speed change, most root complex today need the RX test equipment to take control of the speed change.
J-BERT M8020A Setup – PCIe 4.0

LTSSM Log – Example for End Point Change Requests to BERT

<table>
<thead>
<tr>
<th>Accept Speed</th>
<th>Preset</th>
<th>PreCursor</th>
<th>MainCursor</th>
<th>PostCursor</th>
<th>FullSwing</th>
</tr>
</thead>
<tbody>
<tr>
<td>True Gen3</td>
<td>P8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P3</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P4</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P5</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P6</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P7</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P9</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>False Gen3</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P6</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen3</td>
<td>P9</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P7</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P0</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P1</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P3</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P4</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P5</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P6</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P7</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P8</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P9</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>False Gen4</td>
<td>10</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
<tr>
<td>True Gen4</td>
<td>P9</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>24 8</td>
</tr>
</tbody>
</table>
PCIe 4.0 RX Tests

16 GT/s Base Specification – RX Test Setup

- PCIe 4.0 Base Spec requires a CEM connector to be part of the test channel!
- All other impairments are provided by J-BERT M8020A
- A built-in reference clock multiplier enables J-BERT M8020A to operate on a DUT’s reference clock if required
- No ref clock connection in case of IR / SRIS
The frequency deviation can be calculated as:

\[ \text{phase modulation amplitude} \times 2 \times \pi \times \text{phase modulation frequency} \]

For a phase modulation amplitude of 25ns and a phase modulation frequency of 33kHz this would be

\[ 25 \times 2 \times \pi \times 33 = 516.25 \text{ppm} \]

The respective settings would be:
J-BERT M8020A Setup – PCIe 4.0

Data Output

- Data Output with integrated de-emphasis
- Pre-defined preset registers allow easy and quick switching between presets
- Pre-shoot and de-emphasis values can be changed by user allowing compensation and calibration at connection point
J-BERT M8020A Setup – PCIe 4.0
Data Output – Internally Generated ISI (optional on M8020A)
J-BERT M8020A Setup – PCIe 4.0

Impairments

- LF-PJ & HF-PJ1 for jitter tolerance measurement
- rSSC for CC RX testing
- Internally generated ISI, HF-PJ2 and DM-SI for RX eye calibration
- RJ and CM-SI are fixed impairments
J-BERT M8020A Setup – PCIe 4.0

RX Test Setup

- Data input with integrated CDR and CTLE
- PCIe 16Gb/s and USB 10Gb/s settings available for M8041A with SN >= DE55300700 or >= MY55300800
PCIe 4.0 RX Tests

Test Automation

- Support for CC as well as IR
- End point as well as root complex
- 2.5 GT/s, 5 GT/s, 8 GT/s and 16 GT/s

PCIe 4.0 support for the N5990A products is planned for Jan 2018.
PCIe 4.0 – 16 GT/s CEM Test Setup

Calibration Setup for 16 GT/s RX

- CBB 4.0 as well as CLB 4.0 need to be combined with ISI trace boards
- CEM calibration procedure is very similar to base spec calibration but SIGTEST instead of SEASIM is mandatory
- J-BERT M8020A successfully tested most of the 16 GT/s AICs and systems at PCIe WS 101
- Many AICs and systems could be trained to loopback using the new LTSSM
### CEM RX Test Setups

AIC and Motherboard Test Channels

#### Gen 4 System Rx Calibration

<table>
<thead>
<tr>
<th>Serial #</th>
<th>Configuration</th>
<th>Full Channel Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>System (27dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 0 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
</tr>
<tr>
<td></td>
<td>System (28dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 3 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
</tr>
<tr>
<td></td>
<td>System (30dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 7 -&gt; SMP Cable -&gt; CLB Rx Lane 0 -&gt; CBB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 16 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (5dB embedding)</td>
</tr>
</tbody>
</table>

#### Gen 4 Add-in Card Rx Calibration

<table>
<thead>
<tr>
<th>Serial #</th>
<th>Configuration</th>
<th>Full Channel Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>AIC (27dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 25 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CLB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
<tr>
<td></td>
<td>AIC (28dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 27 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CLB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
<tr>
<td></td>
<td>AIC (30dB Channel)</td>
<td>BERT -&gt; SMA Cable -&gt; SMA/SMP Adaptor -&gt; ISI Pair 31 -&gt; SMP Cable -&gt; CBB Rx Lane 0 -&gt; CLB Tx Lane 0 -&gt; SMP Cable -&gt; ISI Pair 0 -&gt; SMP/SMA Adaptor -&gt; SMA Cable -&gt; Scope (3dB embedding)</td>
</tr>
</tbody>
</table>
## CEM RX Test Setups

### AIC and Motherboard Test Channels Loss Calculation

<table>
<thead>
<tr>
<th>Serial # of CEM Kit</th>
<th>10</th>
<th>16</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Trace</td>
<td>1.17</td>
<td>1.43</td>
<td>1.09</td>
</tr>
<tr>
<td>Long Trace</td>
<td>11.69</td>
<td>11.77</td>
<td>11.75</td>
</tr>
<tr>
<td>Loss/inch</td>
<td>1.052</td>
<td>1.034</td>
<td>1.066</td>
</tr>
<tr>
<td>SMA Female to SMP Female Cab</td>
<td>0.2225</td>
<td>0.2225</td>
<td>0.2225</td>
</tr>
<tr>
<td>Coaxial Launch 2x</td>
<td>0.725</td>
<td>0.985</td>
<td>0.645</td>
</tr>
<tr>
<td>CBB Tx &lt;-&gt; CLB Rx</td>
<td>9.69</td>
<td>10.32</td>
<td>9.71</td>
</tr>
</tbody>
</table>

| Mated CEM Connector Loss | 1.156| 1.652| 1.158|

| CBB Tx Loss | 4.6745| 5.2465| 4.6785|
| CLB Tx Loss | 2.4665| 2.5605| 2.4545|

### System Rx CAL

| CBB ISI (Desired) | 10.3255| 9.7535| 10.3215|
| CBB ISI (Measured) | 10.13| 9.55| 10.16|
| CBB ISI Pair       | Pair 16| Pair 15| Pair 16|
| 27dB (Measured)    | 21.87| 21.87| 22.14|
| 27dB CLB ISI Pair  | Pair 0| Pair 0| Pair 0|
| 28dB (Measured)    | 23.17| 23.28| 23.01|
| 28dB CLB ISI Pair  | Pair 3| Pair 3| Pair 2|
| 30dB (Measured)    | 25.11| 25.15| 25.05|
| 30dB CLB ISI Pair  | Pair 7| Pair 7| Pair 6|

### AIC Rx CAL

| CLB ISI (Desired) | 2.5335| 2.4395| 2.5455|
| CLB ISI (Measured) | 3| 2.47| 2.53|
| CLB ISI Pair       | Pair 0| Pair 0| Pair 0|
| 27dB (Measured)    | 24.25| 24.2| 24.32|
| 27dB CLB ISI Pair  | Pair 25| Pair 24| Pair 25|
| 28dB (Measured)    | 25.16| 25.26| 25.25|
| 28dB CLB ISI Pair  | Pair 27| Pair 26| Pair 27|
| 30dB (Measured)    | 26.9| 26.94| 27.18|
| 30dB CLB ISI Pair  | Pair 31| Pair 30| Pair 31|
PCle 4.0 RX Stress Signal Calibration
16 GT/s Receiver Stress Signal Calibration Setup – 2

PCle Base Specification 4.0 requires a CEM connector to part of the test channel!

- PCIe 4.0 Base Spec requires a CEM connector to be part of the test channel
- Channel calibration with preset selection to get as close to target eye height and eye width as possible. J-BERT M8020A's internal ISI can be used to calibrate channel. Preset is selected on optimal RX eye area
- DM-SI and CM-SI are calibrated through the channel
- Compliance eye calibration is done by adjusting DM-SI, SJ or $V_{\text{diff}}$
- If SJ was changed from 100 mUI during the compliance eye calibration, the SJ portion >100 mUI is applied as a secondary SJ tone @ 210 MHz during the RX test. This allows to follow the jitter tolerance compliance curve
Workshop 104 Gen4 RX Testing Suite
PCIe 4.0 RX Stress Signal Calibration

Compliance Eye Calibration

Channel determined by the channel calibration is applied

DM-SI, SJ and $V_{\text{diff}}$ are adjusted to find correct combination for a compliant eye of the reference RX
PCle Gen5

Preliminary Goals

- Signaling rate: 32GT/s NRZ (no PAM4)
- Channel loss target is: -35dB @ 16GHz (Nyquist)
- BER target is 10e-12
- TX Presets P0-P10 to remain the same
- Backward compatibility with previous PCle Gen1/2/3/4
- Same approach for TX and RX testing used for Gen4
  - Similar method for TX testing via de-embedding of breakout board traces
  - Similar method for calibrating the eye width and eye height as used with PCle 4.0 (ISI based, fixed RJ)
- Same TX Voltage parameters as Gen4
Conclusions

1. Gen4 v1.0 is released (BASE)

2. Official statement on scope BW required for TX and RX calibration is in the v0.9 spec. The official requirement is a minimum scope bandwidth of 25GHz due to the need to match edge BW of JBERT during calibration. This also is required for TX testing.

3. PCIe 4.0 Reference Clock Phase Jitter requirements have expanded significantly since PCIe 3.0.

4. PCIe 4.0 to include lane margining.

5. Receiver Calibration Channel is to have a CEM connector EIEOS changes to 16 1’s and 16 0’s at v0.7.

6. PCIe 4.0 informal FYI testing (CEM) began with the August 2017 workshops in Milpitas.

7. Tools for full PCIe 4.0 TX and RX BASE testing are available today.
PCI Express® 4.0 – Keysight Total Solution

Physical layer – interconnect design
- ADS design software
- 86100D DCA-X/TDR
- E5071C ENA option TDR
- Verify PCIe 4.0 Compliant Channels
- Verify Return Loss Compliance

Physical layer-transmitter test
- V-Series, Z-Series Real-Time Oscilloscopes
- N5393F PCI Express 4.0 TX Electrical compliance software
- 86100CU-400 PLL and Jitter Spectrum Measurement SW

Physical layer-receiver test
- M8020A J-BERT High Performance, Protocol Aware BERT
- N5990A automated compliance and device characterization test software
- Automated RX Test software
  - Accurate, Efficient
  - Comprehensive RX Testing
For more Information...

You will find more information on PCI Express and Keysight test solutions at:

www.pci-sig.com

www.keysight.com/find/pciexpress


www.keysight.com/find/PCIe_receiver_test

PCI-SIG Website, Specification, S/W Tools, Keysight Test Procedure

Keysight tools to help you succeed with your PCI Express design such as the N5393F Compliance application.

Keysight digital webcast registration page.

PCle 4.0 Rx Test Detailed Information

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