Introduction to DisplayPort and DisplayPort Compliance Testing
A Quick Look at the Web....

VESA approves DisplayPort 1.1: kiss those DVI and VGA ports goodbye— engadget April 4, 2007

...when it comes to PCs and notebooks, it rather looks like DVI and VGA could be replaced by DisplayPort over the next few years
-the Inquirer Sept 18, 2007

Displayport is worth watching as it appears to be the only potential spoiler. Andrew Schmitt Jan 12, 2007

"I was just about to lay out for a new monitor. I guess I'll hold off for another year then?"

"Geeks want bigger displays. Consumers want to get rid of cable clutter. So guess who wins?"

"The PC and monitor industries have failed to unite behind a single digital interface standard. The result - yet another standards battle that is sure to baffle consumers and lead to higher costs for manufacturers in the long run."

Tom Mainelli, senior research analyst, IDC Displays and Projectors
Presentation Topics

- Introduction to DisplayPort
- Testing Considerations in DisplayPort
- Compliance Program
- Validation Tools and Leverage in the Design and DeBug Process
Introduction to DisplayPort

1. High Level View of the world:
   PC vs Consumer Electronics

2. Physical interface

3. Benefits
Introduction: Display Technologies Overview

- **Personal Computer**
  - DVI 1.0
  - HDMI 1.1
  - HDMI 1.2
  - UDI 1.3
  - UDI 1.4
  - Wireless HDMI
  - Wireless HD
  - DisplayPort

- **Consumer Electronics**
  - DisplayPort

Today
DisplayPort Technology Overview

1 to 4 high speed lanes (1.62, 2.7Gb/s) – Source to Sink only
  – Fixed data rate independent of display refresh
Auxiliary channel for bidirectional link communication (1Mb/s)
Auto detect of cable plug/unplug
DisplayPort Technology (Main Link Lanes)

DisplayPort Signal Parameters

- 400, 600, 800, 1200 mVolts pk-pk. 1200 is optional
- 0, 3.5, 6, 9.5 dB pre-emphasis. 9.5dB is optional
- No combination of voltage and pre-emphasis can exceed 1200mVolts pp
- Spread Spectrum Clocking (30-33KHz spreading frequency, downspread)
- Rise time not to be below 75ps
- Total Jitter and Non-ISI jitter is specified
- Data Rate fixed at 1.62 or 2.7Gbs
- PLL BW at 10 MHz effective
- Each lane is Differential, 100Ω.
- ANSI standard 8b/10b
- Each lane has separate clock recovery
- Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.
DisplayPort Technology (AUX Channel)

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex

- The Transmitter is the master
- Receiver gains attention by pulling down on the Hot Plug Detect Line
- Manchester II coding
## DisplayPort and HDMI Technologies

<table>
<thead>
<tr>
<th></th>
<th>HDMI</th>
<th>DisplayPort</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Market</strong></td>
<td>HDTV/Gaming</td>
<td>PCs</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>TMDS (8B/10B)</td>
<td>PCI-E (ANSI 8B/10B)</td>
</tr>
<tr>
<td><strong>Configuration</strong></td>
<td>4 lanes (3 Data, 1 Ck) Differential, DC</td>
<td>1, 2, or 4 lanes (Embedded Clock) Differential, AC coupled</td>
</tr>
<tr>
<td></td>
<td>coupled</td>
<td></td>
</tr>
<tr>
<td><strong>Bit Rate</strong></td>
<td>250Mbs to 3.4Gbs per lane</td>
<td>1.62 or 2.7Gbs</td>
</tr>
<tr>
<td><strong>Tx/Rx Negotiation</strong></td>
<td>EDID/DDC</td>
<td>AUX Channel</td>
</tr>
<tr>
<td><strong>Compliance</strong></td>
<td>Authorized Test Centers</td>
<td>Qualified Test Houses</td>
</tr>
<tr>
<td><strong>Ownership</strong></td>
<td>HDMI.org</td>
<td>VESA</td>
</tr>
<tr>
<td><strong>Std/Royalty</strong></td>
<td>Closed/Yes</td>
<td>Open/No</td>
</tr>
<tr>
<td><strong>Driving Need</strong></td>
<td>HDTV and HDCP</td>
<td>Margin</td>
</tr>
<tr>
<td><strong>Models</strong></td>
<td>External</td>
<td>External and Embedded</td>
</tr>
</tbody>
</table>
What does DisplayPort mean?

- Fewer Connectors
- Fewer ICs

- Cheaper
- Less Power
- More Available Pins
- Has Headroom

Looks like a margin play
Scalable benefits vs resolution
DisplayPort Applications

- Computer Graphics Controller
- Computer Display
- Multimedia monitor
- Device concentrator
- Device replicator
- Repeater
- Display controller
- Multimedia / AV selector (e.g. Home theater receiver)
- Legacy converter / Protocol Bridge (e.g. DP <-> HDMI/VGA/DVI)
- Handheld Video
- Chip-chip communications
- Cables
Testing Considerations for DisplayPort

Familiar Measurement and Development Problems

Phy Layer Test Points

Content → Video Transmitter → Media → Video Receiver → Display

Link Layer/Protocol/HDCP Test and Control Points
Testpoints

Physical Layer
Testpoints

Link Layer

Source

Sink
Types of Devices

Sources
Sinks

Cables
Branch Devices

- Repeaters
Types of Devices

Branch Devices

- Replicator
- Concentrator
- DisplayPort to Legacy
  Legacy to DisplayPort
Types of Test Devices

**Signal Analyzer**
- Analyzes Waveform Parameters of DisplayPort Source signals

**Signal Generator**
- Generates DisplayPort Data with controllable jitter and level

**Reference Sink**
- Receives DisplayPort signals and Data and has controllable state

**Reference Source**
- Generates DisplayPort signals and has controllable Data and state
Testing Configurations

Source

- Source Device
  - Video Source
  - DP Tx
- Analyzer
- Ref Sink

Sink

- Generator
- Ref Source
- Sink Device
  - DP Rx w/ DPCD
  - Rendering Function w/ EDID
- Ref Source
- Generator
- Analyzer

Cable

(different generator and analyzer needs)
Testing Configurations

Branch Devices

...and similar treatment for the other Branch Devices
DisplayPort Compliance (My Version)

DisplayPort Compliance Checklists

Link Layer CTS
- Test 1
- Test 2
- Test 3

Phy Layer CTS
- Test 1
- Test 2
- Test 3

VESATM approved Test Center

Adopter’s Product

Adopter

DisplayPort Logo License Agreement

Logo Granted

Compliant Product List
Compliance Flow (Official Compliance Process)
Checklists

1. Not available explicitly currently, but comprehended easily

2. Rules
   - if device has a source, tests include source physical and link layer tests
   - if device has a sink, sink physical and link layer tests.
   - if device is a branch, link and physical layer tests appropriate for upstream source device and downstream sink device, and AUX transactions conducted ‘through’ the device.
Compliance Tests (Phy Layer)

1. Source Tests
   - Eye Diagram Test
   - Non-PreEmphasis Level
   - Pre-Emphasis Accuracy
   - Intra pair skew
   - Inter pair skew
   - Frequency Accuracy
   - Non-ISI Jitter
   - Total Jitter
   - AC Common Mode noise
   - Unit Interval
   - Frequency Long Term Stability
   - Spread Spectrum Modulation Frequency
   - Spread Spectrum Modulation Deviation accuracy

2. Sink Tests
   - Jitter Tolerance

3. Cable Tests
   - Intra Pair Skew
   - Far End Noise
   - Cable and Connector Impedance
   - Insertion Loss
   - Near End Noise
   - Return Loss
Compliance Tests (Link Layer)

Source Tests
- AUX Read after Hot Plug Connect
- EDID Reads
- DPCD Reads
- Link Training
- Link Maintenance
- Main Stream Data Mapping
- Maximum Pixel Rate
- Main Video Stream Format Change Handling

Sink Tests
- AUX Channel Protocol
- EDID Reads
- DPCD Reads
- Link Training
- Link Maintenance
- Main video Reconstruction
- Maximum Pixel Rate
- Main Video Stream Format Change Handling
DisplayPort Compliance Summary
A lot like USB…

<table>
<thead>
<tr>
<th>Plugfests</th>
<th>Focus to facilitate interoperability by exposure and by test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logo</td>
<td>Yes</td>
</tr>
<tr>
<td>Certification</td>
<td>VESA approved independent Test centers: Allion, ETC, NTS, Contech Research</td>
</tr>
<tr>
<td>Product Change Criteria</td>
<td>Re-certification required at Test House if Critical or Significant changes are made</td>
</tr>
<tr>
<td>Self Certification</td>
<td>No</td>
</tr>
</tbody>
</table>

Compliance maturity obviously is low at this point:
- **VTM will administer the compliance testing at Plugtests.**
- **No official statement on interoperability test regimen like USB.**
- No official mechanisms for cooperation between test vendors, test labs, plugfests and VESA to assure ‘conscious interoperability’.
DisplayPort Source Testing

DSO80000B Infiniium Oscilloscopes

U7232A DisplayPort Compliance Test SW

Fixture
What a Test setup might look like…

With Probe Amp and N5380A probe head

Direct A-B connection: no probe Amp or probe head
Leverage to the Design and Debug Process

Equalization of cable end signal.

Degraded Eye due to 5m cable

Equalized Eye

Useful for Receiver Equalization evaluation or Sanity check
Leverage to Debug Process: Jitter Analysis
Leverage to Debug: Eye Diagram Analysis

Alternating Pattern

w/PRBS7 Pattern
Pre-Emphasis and Qualified Triggering

Analyzing Pre-emphasis in DisplayPort

Histogram of last half of first transition bit

Zone 'Keep Out' for qualifying trigger

Zone 'Keep Out' for qualifying trigger

<table>
<thead>
<tr>
<th>Histogram</th>
<th>Color Grade</th>
<th>Scales</th>
</tr>
</thead>
<tbody>
<tr>
<td>X Scale</td>
<td>34 hits/</td>
<td></td>
</tr>
<tr>
<td>X Offset</td>
<td>0 hits</td>
<td></td>
</tr>
<tr>
<td>Mean</td>
<td>224.7067 mV</td>
<td></td>
</tr>
<tr>
<td>Std Dev</td>
<td>7.0128 mV</td>
<td></td>
</tr>
<tr>
<td>μ±1σ</td>
<td>66.8%</td>
<td></td>
</tr>
<tr>
<td>μ±2σ</td>
<td>99.0%</td>
<td></td>
</tr>
<tr>
<td>μ±3σ</td>
<td>100%</td>
<td></td>
</tr>
<tr>
<td>Median</td>
<td>223.2 mV</td>
<td></td>
</tr>
<tr>
<td>Mode</td>
<td>226.7 mV</td>
<td></td>
</tr>
<tr>
<td>p-p</td>
<td>32.7 mV</td>
<td></td>
</tr>
<tr>
<td>Min</td>
<td>209.4 mV</td>
<td></td>
</tr>
<tr>
<td>Max</td>
<td>242.1 mV</td>
<td></td>
</tr>
<tr>
<td>Hits</td>
<td>1.519 khits</td>
<td></td>
</tr>
<tr>
<td>Peak</td>
<td>134 hits</td>
<td></td>
</tr>
</tbody>
</table>
DisplayPort Sink Testing

Requires manual control of DUT and probing of DisplayPort Configuration Registers

GUI of N4903A
Table of CTS
Sink Testing w/N4903A

Pattern Setup

Jitter Setup
DisplayPort Support Overview

Compliance Test
  • Source Test

DSO80804B
Realtime Oscilloscope

• Sink Test

N4903A J-BERT

• Cable/Connector/Interconnect Test

86100C
Digital Communications Analyzer

81250A
Par-BERT

U7232A
Compliance Software

E5701A
Vector Network Analyzer
Summary

✓ DisplayPort is definitely on its way!
✓ DisplayPort enables better margins.
✓ DisplayPort links are dynamic.
✓ Compliance Testing is beginning to show a rigorous posture.

✓ Agilent has broad product offering to support development and validation of DisplayPort designs.
Additional Resources

DisplayPort information
www.agilent.com/find/displayport

Signal Integrity information:
www.agilent.com/find/si