Keysight D9040DPPC DisplayPort Compliance Test Application

KEYSIGHT TECHNOLOGIES

Programmer's Reference

Notices

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WARNING

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In This Book

This book is your guide to programming the Keysight Technologies D9040DPPC DisplayPort Compliance Test Application.

- Chapter 1, “Introduction to Programming,” starting on page 7, describes compliance application programming basics.
- Chapter 2, “Configuration Variables and Values,” starting on page 9, Chapter 3, “Test Names and IDs,” starting on page 83, Chapter 4, “Instruments,” starting on page 167, and Chapter 5, “Message IDs,” starting on page 169 provide information specific to programming the D9040DPPC DisplayPort Compliance Test Application.

How to Use This Book

Programmers who are new to compliance application programming should read all of the chapters in order. Programmers who are already familiar with this may review chapters 2, 3, 4, and 5 for changes.

Contents

1 Introduction to Programming

This chapter introduces the basics for remote programming a compliance application. The programming commands provide the means of remote control. Basic operations that you can do remotely with a computer and a compliance app running on an oscilloscope include:

- Launching and closing the application.
- Configuring the options.
- Running tests.
- Getting results.
- Controlling when and were dialogs get displayed
- Saving and loading projects.

You can accomplish other tasks by combining these functions.

Remote Programming Toolkit

The majority of remote interface features are common across all the Keysight Technologies, Inc. family of compliance applications. Information on those features is provided in the N5452A Compliance Application Remote Programming Toolkit available for download from Keysight here: www.keysight.com/find/rpi. The D9040DPPC DisplayPort Compliance Test Application uses Remote Interface Revision 6.12. The help files provided with the toolkit indicate which features are supported in this version.

In the toolkit, various documents refer to "application-specific configuration variables, test information, and instrument information". These are provided in Chapters 2, 3, and 4 of this document, and are also available directly from the application's user interface when the remote interface is enabled (View>Preferences::Remote tab::Show remote interface hints). See the toolkit for more information.

2 Configuration Variables and Values

The following table contains a description of each of the D9040DPPC DisplayPort Compliance Test Application options that you may query or set remotely using the appropriate remote interface method. The columns contain this information:

- GUI Location – Describes which graphical user interface tab contains the control used to change the value.
- Label – Describes which graphical user interface control is used to change the value.
- Variable – The name to use with the SetConfig method.
- Values – The values to use with the SetConfig method.
- Description – The purpose or function of the variable.

For example, if the graphical user interface contains this control on the **Set Up** tab:

- Enable Advanced Features

then you would expect to see something like this in the table below:

Table 1 Example Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Set Up	Enable Advanced Features	EnableAdvanced	True, False	Enables a set of optional features.

and you would set the variable remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SetConfig 'EnableAdvanced' 'True'"

C# syntax
```

```
---------
remoteAte.SetConfig("EnableAdvanced", "True");
```

Here are the actual configuration variables and values used by this application:

NOTE Some of the values presented in the table below may not be available in certain configurations. Always perform a "test run" of your remote script using the application's graphical user interface to ensure the combinations of values in your program are valid.

NOTE The file, "ConfigInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 2 Configuration Variables and Values

GUI Location	Label	Variable	Values	Description
Configure	AC Common Mode Cutoff Frequency	CutOffFrequency	(Accepts user-defined text), 1000 MHz, 500 MHz, 50 MHz	Set the 3dB cutoff frequency of the filter used for AC Common Mode Tests. This configuration only applicable when the [Filter] configuration variable is set to either [High Pass Filter] or [Low Pass Filter]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	AC Common Mode Edges	ACCommonEdge	(Accepts user-defined text), 100, 1000, 10000, 100000	Set the number of edges measured for the AC common mode test.
Configure	AC Common Mode Filter	Filter	None, HighPassFilter, LowPassFilter	Select the filter used for AC Common Mode Tests, either a high pass filter, low pass filter or no filter is applied on the signal before AC common mode measurement. Note: Interpolation will be turned off if either high pass filter or low pass filter is selected.
Configure	AC Gain (CTLE With AC Gain) - HBR2 (dB)	ACGainCTLE_HBR2	(Accepts user-defined text), 3.5	Set the AC gain of the CTLE with AC gain (USB 3.1) used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	AC Gain (CTLE With AC Gain) - HBR2 No Cable Model (dB)	ACGainCTLE_HBR2NoCable	(Accepts user-defined text), 3.5	Set the AC gain of the CTLE with AC gain (USB 3.1) used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	AC Gain (CTLE With AC Gain) - HBR3 (dB)	ACGainCTLE_HBR3	(Accepts user-defined text), 3.5	Set the AC gain of the CTLE with AC gain (USB 3.1) used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	AC Gain (CTLE With AC Gain) - HBR3 No Cable Model (dB)	ACGainCTLE_HBR3NoCable	(Accepts user-defined text), 3.5	Set the AC gain of the CTLE with AC gain (USB 3.1) used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	AUX Channel Filter	AUXFilterType	Auto, None, LowPassFilter, HighPassFilter, BandPassFilter	Select the filter used for AUX Channel Eye Tests. For [Auto], band pass filter will be used for DisplayPort 1.4a, DPoC 1.4a and later test specification while no filter will be used for test specification earlier than DisplayPort 1.4a and DPoC 1.4a.
Configure	AUX Channel Filter Order	AUXFilterOrder	1, 2, 3	Select the filter order used for AUX Channel Eye Tests.
Configure	AUX Channel High Pass Filter Cutoff Frequency	AUXHighPassFilterCutOffFrequency	(Accepts user-defined text), 1000 kHz, 500 kHz, 400 kHz, 300 kHz, 200 kHz, 100 kHz, 50 kHz	Set the 3dB cutoff frequency of the high pass filter used for AUX Channel Eye Tests. This configuration only applicable when the [Filter] configuration variable is set to either [High Pass Filter] or [Band Pass Filter]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	AUX Channel Idle DC Offset	AUXIdleDCOffset	True, False	Select whether or not to remove the AUX channel idle DC offset for AUX Channel Tests.
Configure	AUX Channel Low Pass Filter Cutoff Frequency	AUXFilterCutOffFrequency	(Accepts user-defined text), 1000 MHz, 500 MHz, 400 MHz, 300 MHz, 200 MHz, 100 MHz	Set the 3dB cutoff frequency of the low pass filter used for AUX Channel Eye Tests. This configuration only applicable when the [Filter] configuration variable is set to either [Low Pass Filter] or [Band Pass Filter]. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	AUX Channel Traffic Decode Count	AUXTrafficDecodeCount	(Accepts user-defined text), 10, 20, 50, 100, 200, 500, 1000	Set the total amount of AUX Channel traffic required for AUX Channel Sensitivity Test. This configuration only applicable when the [Test Method] configuration variable is set to oscilloscope decode method [Scope Method].
Configure	AUX Channel Traffic Prompt	PromptForAUXTraffic	true, false	Select whether or not to prompt the user to initiate AUX Channel traffic for AUX Channel Tests.
Configure	AUX Channel Voltage Swing Maximum Limit (V)	AUXSensitivityMaxVSwing	(Accepts user-defined text), 0.28, 0.26	Set the calibrated AUX Channel voltage swing maximum limit for AUX Channel Calibration Test. Unit: V.
Configure	AUX Channel Voltage Swing Minimum Limit (V)	AUXSensitivityMinVSwing	(Accepts user-defined text), 0.28, 0.24	Set the calibrated AUX Channel voltage swing minimum limit for AUX Channel Calibration Test. Unit: V.
Configure	Bandwidth Correction Mode	BandwidthCorrectionMode	True, False	Select whether to apply correction to the bandwidth of the second order PLL clock recovery. This configuration only applicable when the [Clock Recovery Order] configuration variable is set to second order PLL clock recovery.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Bandwidth Reduction	bwreduction	STAND, AUTO, MAX, 4E9, 6E9, 8E9, 13E9, 16E9, 20E9, 32E9	Set the acquisition bandwidth reduction of the oscilloscope. This configuration is only available when either Enhance Bandwidth or Noise Reduction option is installed on the oscilloscope. For [Standard], 13GHz acquisition bandwidth reduction is set for RBR, HBR, HBR2 while 16GHz acquisition bandwidth reduction is set for HBR3. For [Automatic], no bandwidth reduction.
Configure	CTLE Model - HBR2	CTLEModelHBR2	Normal, USB3.1	Select the CTLE model used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable for DP 1.4 and above Test Specification.
Configure	CTLE Model - HBR2 No Cable Model	CTLEModelHBR2NoCable	Normal, USB3.1	Select the CTLE model used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable for DP 1.4 and above Test Specification.
Configure	CTLE Model - HBR3	CTLEModelHBR3	Normal, USB3.1	Select the CTLE model used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable for DP 1.4 and above Test Specification.
Configure	CTLE Model - HBR3 No Cable Model	CTLEModelHBR3NoCable	Normal, USB3.1	Select the CTLE model used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable for DP 1.4 and above Test Specification.
Configure	Cable Construction	CableConstruction	CAT1, CAT2, Hybrid	Select the Cable Construction used.
Configure	Cable Equalizer	CableEqualizater	Off, 2, 5, 10, Manual	Selects the Type of Equalizer of the cable test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Cable Mask	CableMask	TP2, TP3	Selects the type of mask to use for the eye test. (TP2 for Source; TP3 for Sink)
Configure	Cable Mask Movement	CableMaskMovement	Fixed, FindPass, FindMargin	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Configure	Cable Model Embedding	CableEmbedding	True, False	Select whether to include cable model embedding when running tests at TP3_EQ test point. This configuration only applicable when the [Custom Transfer Function] configuration variable is set to [False].
Configure	Cable Model Type	CableModelType	Auto, Standard DP/mDP, USB Type-C	Select the type of cable model to be embedded when running tests at TP3_EQ test point. This configuration is only applicable when the [Custom Transfer Function] configuration variable is set to [False] and the [Cable Model Embedding] configuration variable is set to [True]. For [Auto], the cable model will be selected based on the connector type.
Configure	Clock Recovery Damping Factor - HBR2 (Second Order PLL Only)	DampingFactorHBR2	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used in the second order PLL to recover the clock for HBR2. This configuration only applicable when the [Clock Recovery Order] configuration variable is set to second order PLL clock recovery.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Damping Factor - HBR25 (Second Order PLL Only)	DampingFactorHBR25	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used in the second order PLL to recover the clock for HBR25. This configuration only applicable when the [Clock Recovery Order] configuration variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - HBR3 (Second Order PLL Only)	DampingFactor_HBR3	(Accepts user-defined text), 1.0, 1.43, 1.51, 1.6, N/A	Set the damping factor used in the second order PLL to recover the clock for HBR3. This configuration only applicable when the [Clock Recovery Order] configuration variable is set to second order PLL clock recovery.
Configure	Clock Recovery Damping Factor - RBR/HBR (Second Order PLL Only)	DampingFactor	(Accepts user-defined text), 1.43, 1.51, 1.6, N/A	Set the damping factor used in the second order PLL to recover the clock for RBR and HBR. This configuration only applicable when the [Clock Recovery Order] configuration variable is set to second order PLL clock recovery.
Configure	Clock Recovery Filter	AUXClockRecoveryFilter	true, false	Select whether or not to apply low pass filter on the AUX Channel signal before recover the clock signal.
Configure	Clock Recovery Loop Bandwidth (Arbitrary Pattern) - HBR2	CRUBandWidthArbitraryPattern_HBR2	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when Arbitrary Pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (Arbitrary Pattern) - HBR25	CRUBandWidthArbitraryPattern_HBR25	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when Arbitrary Pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (Arbitrary Pattern) - HBR3	CRUBandWidthArbitraryPattern_HBR3	(Accepts user-defined text), 30 MHz, 15 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when Arbitrary Pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Loop Bandwidth (Arbitrary Pattern)-HBR	CRUBandWidthArbitraryPattern_HBR	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when Arbitrary Pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (Arbitrary Pattern)-RBR	CRUBandWidthArbitraryPattern_RBR	(Accepts user-defined text), 10.8 MHz, 5.4 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when Arbitrary Pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (D10.2) - HBR	CRUBandWidthHighBitRate	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (D10.2) - HBR2	CRUBandWidthHBR2	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (D10.2) - HBR25	CRUBandWidthHBR25	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (D10.2) - HBR3	CRUBandWidth_HBR3	(Accepts user-defined text), 30 MHz, 15 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (D10.2) - RBR	CRUBandWidthLowBitRate	(Accepts user-defined text), 10.8 MHz, 5.4 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Loop Bandwidth (HBR2CPAT) - HBR2	CRUBandWidthHBR2CPATHBR2	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when HBR2CPAT pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (HBR2CPAT) - HBR25	CRUBandWidthHBR2CPATHBR25	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when HBR2CPAT pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (HBR2CPAT) - HBR3	CRUBandWidthHBR2CPAT_HBR3	(Accepts user-defined text), 30 MHz, 15 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when HBR2CPAT pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (PRBS 7) - HBR	CRUBandWidthPRBS7High	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (PRBS 7) - HBR2	CRUBandWidthPRBS7HBR2	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (PRBS 7) - HBR25	CRUBandWidthPRBS7HBR25	(Accepts user-defined text), 20 MHz, 10 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Loop Bandwidth (PRBS 7) - HBR3	CRUBandWidthPRBS7_HBR3	(Accepts user-defined text), 30 MHz, 15 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Clock Recovery Loop Bandwidth (PRBS 7) - RBR	CRUBandWidthPRBS7LowBitRate	(Accepts user-defined text), 10.8 MHz, 5.4 MHz	Set the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Clock Recovery Method (Low Frequency Uncorrelated Deterministic Jitter)	UDJ_LF_ClockRecoveryMethod	ConstantClock, Auto	Select the clock recovery method used for Low Frequency Uncorrelated Deterministic Jitter Test. For [Auto] mode, the clock recovery method defined in Clock Recovery Settings will be used.
Configure	Clock Recovery Order	ClockRecoveryOrder	1st, 2nd	Select the clock recovery order to either first order PLL clock recovery method or second order PLL clock rcovery method to recover the clock from the data.
Configure	Custom Eye Mask	CustomEyeMask	False, True	Select to enable or disable the use of custom eye mask for Eye Diagram Test and Eye Diagram Test (TP3_EQ).
Configure	Custom Transfer Function	CustomTransferFunction	True, False	Select whether to use custom transfer function for embedding and de-embedding when running tests at TP3_EQ test point. The [Cable Model Embedding] and [Cable Model Type] configuration variables are not applicable if the [Custom Transfer Function] configuration variable is set to [True].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Custom Transfer Function File Name	CustomTFFileName	(Accepts user-defined text), CustomEmbedded	Set the custom transfer function file name for embedding and de-embedding when running tests at TP3_EQ test point. This configuration only applicable when the [Custom Transfer Function] configuration variable is set to [True]. The custom transfer function file must located at the following directory: C:\Program Files\Keysight\Infiniium\Apps\DisplayPortTest\app\config\TransferFunction\RBR_HBR_HBR2\Custom\ and C:\Program Files\Keysight\Infiniium\Apps\DisplayPortTest\app\config\TransferFunction\HBR3\Custom\.
Configure	DC Gain (CTLE With AC Gain) - HBR2 (dB)	DCGainCTLE_HBR2	(Accepts user-defined text), 0	Set the DC gain of the CTLE with AC gain (USB 3.1) used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	DC Gain (CTLE With AC Gain) - HBR2 No Cable Model (dB)	DCGainCTLE_HBR2NoCable	(Accepts user-defined text), 0	Set the DC gain of the CTLE with AC gain (USB 3.1) used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	DC Gain (CTLE With AC Gain) - HBR3 (dB)	DCGainCTLE_HBR3	(Accepts user-defined text), 0, -1, -2, -3, -4, -5, -6, -7, -8	Set the DC gain of the CTLE with AC gain (USB 3.1) used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	DC Gain (CTLE With AC Gain) - HBR3 No Cable Model (dB)	DCGainCTLE_HBR3NoCable	(Accepts user-defined text), 0, -1, -2, -3, -4, -5, -6, -7, -8	Set the DC gain of the CTLE with AC gain (USB 3.1) used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: dB.
Configure	DC Gain (CTLE Without AC Gain) - HBR	GainHBR	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR No Cable Model	GainHBRNoCable	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR2	GainHBR2	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR2 No Cable Model	GainHBR2NoCable	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR25	GainHBR25	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR25 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	DC Gain (CTLE Without AC Gain) - HBR25 No Cable Model	GainHBR25NoCable	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR25 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR3	GainHBR3	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - HBR3 No Cable Model	GainHBR3NoCable	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DC Gain (CTLE Without AC Gain) - RBR	GainRBR	(Accepts user-defined text), 0.5, 1	Set the DC gain of the 2/3 Poles CTLE used for RBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal].
Configure	DFE Eye Analysis Method	DFE_EyeAnalysisMethod	Infiniium, VESA Eye Test Tool	Select the DFE eye analysis method to used when running tests at TP3_EQ test point.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	DFE Setup - HBR2	DFE_Setup_HBR2	Auto, PartialAuto, Manual	Select whether to automatically setup or manually setup the DFE for HBR2 when running tests at TP3_EQ test point. For [Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. For [Partial Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. Then, override the gain and delay. For [Manual], the user need to specify the tap value, upper target voltage, lower target voltage, gain and delay.
Configure	DFE Setup - HBR3	DFE_Setup_HBR3	Auto, PartialAuto, Manual	Select whether to automatically setup or manually setup the DFE for HBR3 when running tests at TP3_DFE test point. For [Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. For [Partial Auto], the Infiniium will perform optimization based on the eye width, minimum and maximum tap value. Then, override the gain and delay. For [Manual], the user need to specify the tap value, upper target voltage, lower target voltage, gain and delay.
Configure	DFE State - HBR2	DFE_State_HBR2	true, false	Select whether to enable or disable the DFE for HBR2 when running tests at TP3_EQ test point.
Configure	DFE State - HBR3	DFE_State_HBR3	true, false	Select whether to enable or disable the DFE for HBR3 when running tests at TP3_DFE test point.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	DFE VESA Eye Test Tool Executable Path	DFE_VESAEyeTestToolExecutablePath	(Accepts user-defined text), C:\Program Files\VESA\DPEyeTest\application\DPEyeTest.exe	Set the path where the VESA Eye Test Tool executable file installed. This configuration only applicable when the [DFE Eye Analysis Method] configuration variable is set to [VESA Eye Test Tool].
Configure	De-Embed with Delay	DeEmbedDelay	(Accepts user-defined text), True, False	Select whether to include or exclude delay for fixture de-embedding.
Configure	Decode Filter	AUXDecodeFilter	true, false	Select whether or not to apply filter before AUX Channel traffic decode for AUX Channel Sensitivity Test.
Configure	Delay - HBR2	DFE_Delay_HBR2	(Accepts user-defined text), Auto, InfiniiumAuto, 0	Set the delay to be used to amplify the eye back to the original size in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. For [Auto], the DisplayPort application will set the delay to center the eye based on the histogram. For [Infiniium Auto], the Infiniium application will set the delay to center the eye. Unit: ps.
Configure	Delay - HBR3	DFE_Delay_HBR3	(Accepts user-defined text), Auto, InfiniiumAuto, 0	Set the delay to be used to amplify the eye back to the original size in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. For [Auto], the DisplayPort application will set the delay to center the eye based on the histogram. For [Infiniium Auto], the Infiniium application will set the delay to center the eye. Unit: ps.
Configure	Differential Vertical Offset (mV)	FixedDifferentialVerticalOffset	(Accepts user-defined text), 0	Set the fixed value used for the vertical offset of differential signal for RBR, HBR, HBR2 and HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Differential Vertical Range (Level 0) (mV)	FixedDifferentialVerticalRange0	(Accepts user-defined text), 500, 560, 600	Set the fixed value used for the vertical range of [Swing 0, Pre-emphasis 0] differential signal for RBR, HBR, HBR2 while only 90% of the fixed value is used for HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.
Configure	Differential Vertical Range (Level 1) (mV)	FixedDifferentialVerticalRange1	(Accepts user-defined text), 700, 720, 800	Set the fixed value used for the vertical range of [Swing 0, Pre-emphasis 1] or [Swing 1, Pre-emphasis 0] differential signal for RBR, HBR, HBR2 while only 90% of the fixed value is used for HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.
Configure	Differential Vertical Range (Level 2) (mV)	FixedDifferentialVerticalRange2	(Accepts user-defined text), 900, 960, 1000	Set the fixed value used for the vertical range of [Swing 0, Pre-emphasis 2], [Swing 1, Pre-emphasis 1] or [Swing 2, Pre-emphasis 0] differential signal for RBR, HBR, HBR2 while only 90% of the fixed value is used for HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Differential Vertical Range (Level 3) (mV)	FixedDifferentialVerticalRange3	(Accepts user-defined text), 1300, 1400, 1500	Set the fixed value used for the vertical range of [Swing 0, Pre-emphasis 3], [Swing 1, Pre-emphasis 2], [Swing 2, Pre-emphasis 1] or [Swing 3, Pre-emphasis 0] differential signal for RBR, HBR, HBR2 while only 90% of the fixed value is used for HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.
Configure	Dual Mode Clock Frequency Validation	DualModeClockFrequencyValidation	true, false	Select to enable or disable clock frequency validation for Dual Mode Test.
Configure	Dual Mode Clock Jitter Multiplier	DMClkJitterMultiplier	AUTO, 1, 5	Select the type of multiplier method used in recover clock for Dual Mode Clock Jitter Test.
Configure	Dual Mode Clock Jitter UI Count	DMClockJitterUICount	(Accepts user-defined text), 100000, 400000	Set the number of UI required for Dual Mode Clock Jitter Test.
Configure	Dual Mode Clock Jitter Window Offset	DMClockJitterWindowOffset	(Accepts user-defined text), 0, 5, 10, 15, 20	Set the vertical offset location used to measure Dual Mode Clock Jitter Test. The value must be in range from 0 to 20. Unit: mV.
Configure	Dual Mode Duty Cycle Edges	DMDutyCycleEdges	(Accepts user-defined text), 1000, 10000	Set the number of edges used for Dual Mode TMDS Clock Duty Cycle Test.
Configure	Dual Mode Eye Height Window End (%)	DualModeEyeHeightEnd	60, 70	Set the ending point of eye height measurement for Dual Mode Test. Unit: %.
Configure	Dual Mode Eye Height Window Start (%)	DualModeEyeHeightStart	40, 30	Set the ending point of eye height measurement for Dual Mode Test. Unit: %.
Configure	Dual Mode Mask File	DualModeMaskFile	Auto, Custom, Above 165 Mhz, Below 165 Mhz	Select the mask file being used for Dual Mode Eye Diagram Test.
Configure	Dual Mode Software Clock Recovery	DMClockRecovery	First, Second	Select the order of Software Clock Recovery for Dual Mode Tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Dual Mode Threshold Mode	DMThresholdMode	Min Max, Top Base, Absolute Zero	Select the threshold mode for Dual Mode Tests, either by VMax/VMin, VTop/VBase or fixed at absolute zero.
Configure	Edges Number (Dual Mode Inter Pair Skew Test)	DMInterPairSkewEdgesNumber	(Accepts user-defined text), 1, 10, 100, 200	Set the number of edges measured for the Dual Mode Inter Pair Skew Test.
Configure	Edges Number (Dual Mode Intra Pair Skew Test)	DMIntraPairSkewEdgesNumber	(Accepts user-defined text), 100, 1000	Set the number of edges measured for the Dual Mode Intra Pair Skew Test.
Configure	Exclude Random Jitter and Noise Derate (TP3_EQ)	ExcludeRandomNoise	False, True	Select to include or exclude random jitter and noise derate of the eye mask used in Eye Diagram Test (TP3_EQ). This configuration only applicable when the [Eye Mask Type (TP3_EQ)] configuration variable is set to [Dynamic]. For [False], random jitter and noise derate will be included in the eye mask generation. For [True], random jitter and noise derate will be excluded in the eye mask generation.
Configure	Expert Mode	ExpertMode	Off, On	Select to enable or disable the expert mode for looser pre-requisite checkers.
Configure	External Scaling	ExternalScaling	Disable, Enable	Select to enable or disable probe external scaling. For [Disable], the probe system external scaling will be defaulted to Gain = 1.0:1 and Offset = 0.0 before start of each test. For [Enable], the probe system external scaling will be remain as the gain and offset set before the run. This configuration is only applicable when the [Connection Type] in Test Setup Dialog is set to [Single-Ended (A-B)].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Eye Diagram (TP3_EQ) UI	TP3EQEyeDiagramUI	(Accepts user-defined text), 1, 10000, 50000, 100000, 256000, 500000, 1000000, 2000000, 10000000	Set the number of UI measured for Eye Diagram Test (TP3_EQ). For [Auto], the DisplayPort application will set the number of edges based on Test Specification selected.
Configure	Eye Diagram UI	EyeDiagramEdge	(Accepts user-defined text), 1, 10000, 50000, 100000, 256000, 500000, 1000000, 2000000, 10000000	Set the number of UI measured for Eye Diagram Test. For [Auto], the DisplayPort application will set the number of edges based on Test Specification selected.
Configure	Eye Mask Center Vertical Position	AUXEyeMaskCenter	0 V, AutoOffset	Select the vertical position of the eye mask center for AUX Channel Tests.
Configure	Eye Mask Movement	EyeDiagramMaskMovement	Fixed, FindPass, FindMargin, AlignAndFindPass, ManualAdjust	Select the eye mask movement type in Eye Diagram Test and Eye Diagram Test (TP3_EQ). For [Fixed] mask movement, the eye diagram mask will not be moved. The test only report Pass or Fail. For [Find Pass] mask movement, the test will search +/-0.5 UI horizontally until no mask violation occurs. For [Find Margin] mask movement, the test will search +/-0.5 UI horizontally to find the maximum margin of no mask violation.
Configure	Eye Mask Scale	MaskScale	Absolute, Normalized, Relative	Select the type of scale to be performed on the eye mask for Eye Diagram Test and Eye Diagram Test (TP3_EQ). Select [Absolute] if absolute voltage eye mask is used. Select [Normalized] if absolute voltage eye mask is used and the eye mask need to be normalized to the offset of the signal. Select [Relative] if relative voltage eye mask is used and the eye mask need to be normalized to the offset of the signal.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Eye Mask Type (TP3_EQ)	EyeMaskTypeTP3EQ	Dynamic, Fixed	Select the type of eye mask used for Eye Diagram Test (TP3_EQ). For [Dynamic], eye mask generated dynamically by placing the eye height at optimum location is used. For [Fixed], fixed eye mask is used.
Configure	Eye Mask Width Reference	AUXEyeMaskWidthReference	Nominal, Average	Select the eye width reference of the eye mask for AUX Channel Tests to either based on nominal data rate (Nominal) or measured data rate (Average).
Configure	Eye Width - HBR2	DFE_EyeWidth_HBR2	(Accepts user-defined text), 0	Set the eye width to be used for the optimization of the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto]. Unit: UI.
Configure	Eye Width - HBR3	DFE_EyeWidth_HBR3	(Accepts user-defined text), 0	Set the eye width to be used for the optimization of the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto]. Unit: UI.
Configure	FFT 1st Harmonic Channel Power Measurement Bandwdith (Hz)	FFT_1stHarmonicChannelPowerMeasBandwdith	(Accepts user-defined text), 500E+3	Set the 1st harmonic channel power measurement bandwidth of the FFT function used for the Level and Equalization Verification Testing. This configuration only applicable when the [FFT Peak Search Mode] configuration variable is set to [Channel Power]. Unit: Hz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	FFT 5th Harmonic Channel Power Measurement Bandwdith (Hz)	FFT_5thHarmonicChannelPowerMeasBandwdith	(Accepts user-defined text), 3E+6	Set the 5th harmonic channel power measurement bandwidth of the FFT function used for the Level and Equalization Verification Testing. This configuration only applicable when the [FFT Peak Search Mode] configuration variable is set to [Channel Power]. Unit: Hz.
Configure	FFT Detector Point	FFT_DetectorPoint	(Accepts user-defined text), 1001	Set the number of detector point of the FFT function used for the Level and Equalization Verification Testing. This configuration only applicable when the [FFT Detector Type] configuration variable is set to value other than [Off].
Configure	FFT Detector Type	FFT_DetectorType	Off, Normal, Sample, Positive Peak, Negative Peak, Average, RMS	Select the detector type of the FFT function used for the Level and Equalization Verification Testing.
Configure	FFT Peak Search Mode	FFT_PeakSearchMode	Infiniium Peak Search, Channel Power	Select the peak search mode of the FFT function used for the Level and Equalization Verification Testing.
Configure	FFT Peak Search Threshold (dBm)	FFT_PeakSearchThreshold	(Accepts user-defined text), 0	Set the peak search threshold of the FFT function used for the Level and Equalization Verification Testing. For auto threshold, set the [FFT Peak Search Threshold] configuration variable to 0. For auto threshold, the DisplayPort application will set the threshold to the half of the maximum FFT magnitude measured. This configuration only applicable when the [FFT Peak Search Mode] configuration variable is set to [Infiniium Peak Search]. Unit: dBm.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	FFT Resolution (kHz)	FFT_RBW	(Accepts user-defined text), 1, 10, 100, 300	Set the resolution of the FFT function used for the Level and Equalization Verification Testing. Note: The [Resolution Bandwidth] configuration variable will affect the memory depth used for the Level and Equalization Verification Testing. Unit: kHz.
Configure	FFT Start Frequency (MHz)	FFT_StartFrequency	(Accepts user-defined text), 500	Set the start frequency of the FFT function used for the Level and Equalization Verification Testing. Unit: MHz.
Configure	FFT Stop Frequency (MHz)	FFT_StopFrequency	(Accepts user-defined text), 4500	Set the stop frequency of the FFT function used for the Level and Equalization Verification Testing. Unit: MHz.
Configure	FFT Window	FFT_Window	Hanning, Rectangular, Flattop, Blackman-Harris, Hamming	Select the window type of the FFT function used for the Level and Equalization Verification Testing.
Configure	Gain - HBR2	DFE_Gain_HBR2	(Accepts user-defined text), 1	Set the gain to be used to amplify the eye back to the original size in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Partial Auto] or [Manual].
Configure	Gain - HBR3	DFE_Gain_HBR3	(Accepts user-defined text), 1	Set the gain to be used to amplify the eye back to the original size in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Partial Auto] or [Manual].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Identical Vertical Scale Mode	IdenticalVerticalScaleMode	Off, On, Fixed	Select either the identical vertical scale or use fixed vertical scale for better consistency in vertical scale setting for Physical Layer Tests. For [Fixed] mode, the fixed value of [Differential Vertical Range] and [Differential Vertical Offset] configuration variables will be used for the vertical range and offset of the differential signal while the half of the fixed value of [Differential Vertical Range] and [Single-Ended Vertical Offset] configuration variables will be used for the vertical range and offset of the single-ended signal if single-ended connection is used.
Configure	Include Crosstalk Derate (TP3_EQ) (HBR2)	IncludeCrosstalkDerate	Auto, True, False	Select to include or exclude crosstalk derate of the eye mask used in Eye Diagram Test (TP3_EQ) for HBR2. This configuration only applicable when the [Eye Mask Type (TP3_EQ)] configuration variable is set to [Dynamic]. For [Auto], crosstalk derate will be included in the eye mask generation only if more than one lane selected (2 Lanes or 4 Lanes). For [True], crosstalk derate will be included in the eye mask generation regardless the lane setting. For [False], crosstalk derate will be excluded in the eye mask generation regardless the lane setting.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Include Crosstalk Derate (TP3_EQ) (HBR3)	IncludeCrosstalkDerate_HBR3	Auto, True, False	Select to include or exclude crosstalk derate of the eye mask used in Eye Diagram Test (TP3_EQ) for HBR3. This configuration only applicable when the [Eye Mask Type (TP3_EQ)] configuration variable is set to [Dynamic]. For [Auto], crosstalk derate will be included in the eye mask generation only if more than one lane selected (2 Lanes or 4 Lanes). For [True], crosstalk derate will be included in the eye mask generation regardless the lane setting. For [False], crosstalk derate will be excluded in the eye mask generation regardless the lane setting.
Configure	Inter Pair Skew Edges	InterPairSkewEdges	(Accepts user-defined text), 1, 10, 100, 200	Set the number of edges measured in Inter Pair Skew Test.
Configure	Inter Pair Skew Maximum Retries	MaxRetries	20, 50, 100	Set the number of retries allowed in Inter Pair Skew Test.
Configure	Inter Pair Skew Pattern Search Method	InterPairSkewSearchMethod	1, 2	Select the pattern search method used in Inter Pair Skew Test. For [Method 1], InfiniiScan Generic Serial Trigger and waveform data is used to decode for serial data pattern. For [Method 2], waveform data is used to decode for serial data pattern.
Configure	Inter Pair Skew Test Pattern	InterPairSkewTestPattern	PRBS 7, Arbitrary Pattern	Select the test pattern used in Inter Pair Skew Test.
Configure	Inter Pair Skew Trigger Pattern - Arbitrary Pattern	InterPairSkewTriggerPattern_ArbitraryPattern	(Accepts user-defined text), 0000001, 0000111	Set the serial pattern trigger for Arbitrary Pattern used in Inter Pair Skew Test.
Configure	Inter Pair Skew Trigger Pattern - PRBS 7	AdditionalTriggerPattern	(Accepts user-defined text), 0000001, 0000111	Set the serial pattern trigger for PRBS 7 used in Inter Pair Skew Test.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Interpolation (AC Common Mode Test)	Interpolation	ON, OFF	Specify whether to turn on or off Sin(x)/x interpolation for AC Common Mode Test. Turning on interpolation may cause more peak-to-peak jitter.
Configure	Interpolation (Eye Diagram)	EyeDiagram_Interpolation	OFF, ON, INT2, INT4, INT8, INT16	Specify whether to turn on or off Sin(x)/x interpolation for CTLE Calibration and Eye Diagram Test. Turning on interpolation may cause more peak-to-peak jitter.
Configure	Intra Pair Skew Edges	IntraPairEdge	(Accepts user-defined text), 100, 1000	Set the number of edges measured for Intra Pair Skew Test.
Configure	Intra Pair Skew Test Pattern	TransmitPattern	D10.2, PRBS 7	Select the test pattern used for Intra Pair Skew Test.
Configure	Intra Pair Skew Trigger Pattern - Arbitrary Pattern	SkewTriggerPattern_ArbitraryPattern	(Accepts user-defined text), 10101	Set the trigger pattern for intra pair skew measurement in Intra Pair Skew Test.
Configure	Intra Pair Skew Trigger Pattern - PRBS 7	SkewTriggerPattern	0000001, 000111, 0011, 01, 0101010, 10101, 010	Set the trigger pattern for intra pair skew measurement in Intra Pair Skew Test. This configuration only applicable when the [Intra Pair Skew Test Pattern] configuration variable is set to PRBS 7.
Configure	Jitter Bit Error Rate Level - HBR3	BER_HBR3	Auto, E6, E9, E10, E11, E12, E13, E14	Set the Bit Error Rate (BER) level used for jitter separation measurements for HBR3. For [Auto], the DisplayPort application will set the BER level based on Test Specification selected.
Configure	Jitter Bit Error Rate Level - RBR, HBR, HBR2	BER	E9, E10, E11, E12, E13, E14	Set the Bit Error Rate (BER) level used for jitter separation measurements for RBR, HBR, HBR2.
Configure	Jitter ISI Filter Lag	JitterISIFilterLag	(Accepts user-defined text), 2, 3, 4, 5, 6, 7, 8, 9, 10	Set the ISI filter lag used for jitter separation measurements. This configuration only applicable when the [Jitter Pattern Length] configuration variable is set to [Arbitrary].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Jitter ISI Filter Lead	JitterISIFilterLead	(Accepts user-defined text), -2, -3, -4, -5, -6, -7, -8, -9, -10	Set the ISI filter lead used for jitter separation measurements. This configuration only applicable when the [Jitter Pattern Length] configuration variable is set to [Arbitrary].
Configure	Jitter Pattern Pattern	JitterWaveformPattern	Auto, Periodic, Arbitrary	Select the waveform pattern length used for jitter separation measurements. For [Auto], [Periodic] pattern length will be used for non arbitrary pattern (PRBS 7, D10.2, HBR2CPAT and other repeating pattern) and [Arbitrary] pattern length will be used for Arbitrary Pattern. [Periodic] pattern length should be used on waveforms with repeating data patterns. [Arbitrary] pattern length should be used on waveforms with non-repeating patterns.
Configure	Jitter RJ (ps)	JitterRJ	(Accepts user-defined text), 0.2	Set the RJ rms for jitter separation measurements when the [Jitter RJ Mode] config variable is set to [Specify RJ]. Unit: ps.
Configure	Jitter RJ Mode	JitterRJMode	Off, Remove Scope RJ (Auto), Remove Scope RJ, Specify RJ	Set the RJ mode used for jitter separation measurements to either [Off], [Remove Scope RJ (Auto)], [Remove Scope RJ] or [Specify RJ]. For [Remove Scope RJ (Auto)] mode, the calculated oscilloscope random jitter is removed from the reported RJ. This option cannot be selected until the scope jitter calibration has been run.
Configure	Jitter Scope RJ (ps)	JitterScopeRJ	(Accepts user-defined text), 0.2	Set the scope RJ rms to be removed for jitter separation measurements when the [Jitter RJ Mode] configuration variable is set to [Remove Scope RJ]. Unit: ps.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Jitter Separation Edges	JitterSeparationEdge	(Accepts user-defined text), 1, 10000, 50000, 100000, 256000, 500000, 1000000, 2000000	Set the number of edges measured for jitter separation measurement. For [Auto], the DisplayPort application will set the number of edges based on Test Specification selected.
Configure	Level Threshold	LevelThreshold	Standard: 10%, 50%, 90%, Percent: 20%, 50%, 80%, Hysteresis: 0.10, Hysteresis: 0.05	Select the threshold level used for serial pattern eye folding in voltage level measurements and pre-emphasis level measurement.
Configure	Low Pass Filter Cutoff Frequency (MHz)	InrushTestLowPassFilter	(Accepts user-defined text), 10, 50	Set the cutoff frequency of the low pass filter apply on the Vd for Inrush Tests. Unit: MHz.
Configure	Low Pass Filter Shape (Low Frequency Uncorrelated Deterministic Jitter)	UDJ_LF_LowPassFilterShape	DB20, DB40	Select the TIE low pass filter shape used for Low Frequency Uncorrelated Deterministic Jitter Test.
Configure	Low Pass Filter Stop Frequency (Low Frequency Uncorrelated Deterministic Jitter)	UDJ_LF_LowPassFilterStopFrequency	(Accepts user-defined text), 500 kHz, 1 MHz, 2 MHz	Set the stop frequency of the TIE low pass filter used for Low Frequency Uncorrelated Deterministic Jitter Test. Please specify the value in following format: "XMHz", "XkHz" or "XHz", where X is an integer.
Configure	Lower Target - HBR2	DFE_LowerTarget_HBR2	(Accepts user-defined text), -1.00	Set the low value to be used in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual]. Unit: V.
Configure	Lower Target - HBR3	DFE_LowerTarget_HBR3	(Accepts user-defined text), -1.00	Set the lower target value to be used in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual]. Unit: V.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Mask Type	MaskType	TP2, TP3	Select the type of mask to use for the Eye Diagram Test. (TP2 for Source; TP3 for Sink)
Configure	Max Tap Value - HBR2	DFE_MaxTapValue_HBR2	(Accepts user-defined text), 1.000	Set the maximum tap value to be used for the optimization of the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto].
Configure	Max Tap Value - HBR3	DFE_MaxTapValue_HBR3	(Accepts user-defined text), 1.000	Set the maximum tap value to be used for the optimization of the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto].
Configure	Maximum Memory Depth (M Points)	MaximumMemoryDepth	(Accepts user-defined text), 2.05, 8.00, 20.0, 30.0, 3.28, 12.8, 32.0, 48.0	Set the maximum acquisition memory depth of the oscilloscope for Physical Layer Tests. Unit: M Points.
Configure	Maximum Retries (Dual Mode Inter Pair Skew Test)	DMInterPairSkewMaxRetries	20, 50, 100	Set the number of re-tries for the Dual Mode Inter Pair Skew Test.
Configure	Maximum Sampling Rate (GSa/s)	MaximumSRate	20, 40, 80, 32, 64, 128	Set the maximum acquisition sampling rate of the oscilloscope for Physical Layer Tests, except Low Frequency Uncorrelated Deterministic Jitter Tests. Note: If the selected sampling rate is not available in the oscilloscope, the DisplayPort application will use the highest sampling rate available in the oscilloscope. Unit: GSa/s.
Configure	Memory Depth (Points)	MemoryDepth	3000000, 5000000, 4800000, 8000000	Set the acquisition memory depth of the oscilloscope for Physical Layer Tests, except Low Frequency Uncorrelated Deterministic Jitter Tests. Unit: Points.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Memory Depth (Points) (AUX Channel Sensitivity Test)	AUXSensitivityMemDepth	(Accepts user-defined text), 2000000, 5000000, 10000000, 20000000, 3200000, 8000000, 16000000, 32000000	Set the acquisition memory depth of the oscilloscope for AUX Channel Sensitivity Test. Unit: Points.
Configure	Memory Depth (Points) (AUX Channel Tests)	AUXMemDepth	(Accepts user-defined text), 200000, 500000, 1000000, 2000000, 4000000, 5000000, 10000000, 20000000, 40000000, 80000000, 320000, 800000, 1600000, 3200000, 6400000, 8000000, 16000000, 32000000, 64000000	Set the acquisition memory depth of the oscilloscope for AUX Channel Tests. Unit: Points.
Configure	Memory Depth (Points) (Dual Mode Tests)	DualModeMemoryPoints	(Accepts user-defined text), 200000, 500000, 1000000, 2000000, 4000000, 320000, 800000, 1600000, 3200000, 6400000	Set the acquisition memory depth of the oscilloscope for Dual Mode Tests. Unit: Points.
Configure	Memory Depth (Points) (Inrush Tests)	InrushTestMemoryPoints	(Accepts user-defined text), 200000, 500000, 1000000, 2000000, 4000000	Set the acquisition memory depth of the oscilloscope for Inrush Tests. Unit: Points.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Memory Depth (Points) (Low Frequency Uncorrelated Deterministic Jitter)	UDJ_LF_MemoryDepth	(Accepts user-defined text), 10000000, 20000000, 27000000, 40000000, 16000000, 32000000, 43200000, 64000000	Set the acquisition memory depth of the oscilloscope for Low Frequency Uncorrelated Deterministic Jitter Tests. Unit: Points.
Configure	Min Tap Value - HBR2	DFE_MinTapValue_HBR2	(Accepts user-defined text), 0	Set the minimum tap value to be used for the optimization of the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto].
Configure	Min Tap Value - HBR3	DFE_MinTapValue_HBR3	(Accepts user-defined text), 0	Set the minimum tap value to be used for the optimization of the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Auto].
Configure	Minimum Failure Required	AUXMaxFailAcquisition	(Accepts user-defined text), 10, 100, 1000	Set the minimum number of acquisition to be analyze before test exit if AUX Channel Sensitivity Test fail. This configuration allows the user to stop the AUX Channel traffic decode immediately after the test fail to save test time.
Configure	Multi Standard USB Type-C Switch Matrix	MultiStandardUSBTypeCSwitchMatrixEnabled	True, False	Select to enable or disable multi standard USB Type-C Switch Matrix.
Configure	Noise Bit Error Rate Level	Noise_BER	E9, E10, E11, E12, E13, E14	Select the Bit Error Rate (BER) level used for noise separation measurements.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Noise ISI Filter Lag	Noise_ISIFilterLag	(Accepts user-defined text), 2, 3, 4, 5, 6, 7, 8, 9, 10	Set the ISI filter lag used for noise separation measurements. This configuration only applicable when the [Noise Pattern Length] configuration variable is set to [Arbitrary].
Configure	Noise ISI Filter Lead	Noise_ISIFilterLead	(Accepts user-defined text), -2, -3, -4, -5, -6, -7, -8, -9, -10	Set the ISI filter lead used for noise separation measurements. This configuration only applicable when the [Noise Pattern Length] configuration variable is set to [Arbitrary].
Configure	Noise Pattern Length	Noise_PatternLength	AUTO, ARBitrary	Select the waveform pattern length used for noise separation measurements. [Periodic] should be used on waveforms with repeating data patterns. [Arbitrary] should be used on waveforms with non-repeating patterns.
Configure	Non Pre-Emphasis Level Edges	LevelEdge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges used for the Non Pre-Emphasis Level Test.
Configure	Number of Acquisition (AUX Channel Calibration Test)	AUXSensitivityCalibrationAcquisition	(Accepts user-defined text), 1, 3, 5, 10	Set the number of acquisition for AUX Channel Calibration Test.
Configure	Number of Acquisition (AUX Channel Tests)	AUXEyeAcquisition	(Accepts user-defined text), 1, 2, 5, 10	Set the number of acquisition needed for AUX Channel Tests.
Configure	Number of Acquisition (Inrush Tests)	InrushTestCount	(Accepts user-defined text), 1, 10	Set the number of acquisition for Inrush Tests.
Configure	Number of Taps - HBR2	DFE_TapNumber_HBR2	1	Set the number of taps to be used in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE State] configuration variable is set to [Enable].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Number of Taps - HBR3	DFE_TapNumber_HBR3	1	Set the number of taps to be used in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE State] configuration variable is set to [Enable].
Configure	PRBS Pattern Checker Rules	PRBSChecker	Strict, Loose	Select the rules applied for PRBS 7 pattern checker. For [Strict], test can only be proceed with correct PRBS 7 pattern. For [Loose], test can be proceed even without correct PRBS 7 pattern.
Configure	Pattern Check	PatternCheckEnable	True, False	Select to enable or disable pattern check for all tests.
Configure	Pattern Decode Method	PattrenDecodeMethod	1, 2	Set the number of edges required when making the VTop and VBase measurements.
Configure	Pattern Search Method (Dual Mode Inter Pair Skew Test)	DMInterPairSkewSearchMethod	1, 2	Define pattern search method for the Dual Mode Inter Pair Skew Test. For [1], the application will use Edge trigger. For [2], the application will use InfiniiScan Serial trigger.
Configure	Pole 1 Frequency (CTLE With AC Gain) - HBR2 (MHz)	Pole1CTLE_HBR2	(Accepts user-defined text), 2700, 3030, 3750, 4050	Set the pole 1 frequency of the CTLE with AC gain (USB 3.1) used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE With AC Gain) - HBR2 No Cable Model (MHz)	Pole1CTLE_HBR2NoCable	(Accepts user-defined text), 2700, 3030, 3750, 4050	Set the pole 1 frequency of the CTLE with AC gain (USB 3.1) used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 1 Frequency (CTLE With AC Gain) - HBR3 (MHz)	Pole1CTLE_HBR3	(Accepts user-defined text), 2700, 3030, 3750, 4050	Set the pole 1 frequency of the CTLE with AC gain (USB 3.1) used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE With AC Gain) - HBR3 No Cable Model (MHz) (CTLE with AC gain (USB 3.1))	Pole1CTLE_HBR3NoCable	(Accepts user-defined text), 2700, 3030, 3750, 4050	Set the pole 1 frequency of the CTLE with AC gain (USB 3.1) used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR (MHz)	Pole1HBR	(Accepts user-defined text), 1350	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR No Cable Model (MHz)	Pole1HBRNoCable	(Accepts user-defined text), 1350	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR2 (MHz)	Pole1HBR2	(Accepts user-defined text), 2700	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR2 No Cable Model (MHz)	Pole1HBR2NoCable	(Accepts user-defined text), 2700	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR25 (MHz)	Pole1HBR25	(Accepts user-defined text), 2700, 3750, 5625	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR25 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR25 No Cable Model (MHz)	Pole1HBR25NoCable	(Accepts user-defined text), 2700, 3375, 3750, 5625	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR25 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR3 (MHz)	Pole1HBR3	(Accepts user-defined text), 2700, 3033, 3750, 4050, 5625	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 1 Frequency (CTLE Without AC Gain) - HBR3 No Cable Model (MHz)	Pole1HBR3NoCable	(Accepts user-defined text), 2700, 3033, 3750, 4050, 5625	Set the pole 1 frequency of the 2/3 Poles CTLE used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 1 Frequency (CTLE Without AC Gain) - RBR (MHz)	Pole1RBR	(Accepts user-defined text), 700	Set the pole 1 frequency of the 2/3 Poles CTLE used for RBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE With AC Gain) - HBR2 (MHz)	Pole2CTLE_HBR2	(Accepts user-defined text), 3000, 4500, 5600, 6000, 10000, 13500	Set the pole 2 frequency of the CTLE with AC gain (USB 3.1) used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE With AC Gain) - HBR2 No Cable Model (MHz)	Pole2CTLE_HBR2NoCable	(Accepts user-defined text), 3000, 4500, 5600, 6000, 10000, 13500	Set the pole 2 frequency of the CTLE with AC gain (USB 3.1) used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE With AC Gain) - HBR3 (MHz)	Pole2CTLE_HBR3	(Accepts user-defined text), 3000, 4500, 5600, 6000, 10000, 13500	Set the pole 2 frequency of the CTLE with AC gain (USB 3.1) used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE With AC Gain) - HBR3 No Cable Model (MHz) (CTLE with AC gain (USB 3.1))	Pole2CTLE_HBR3NoCable	(Accepts user-defined text), 3000, 4500, 5600, 6000, 10000, 13500	Set the pole 2 frequency of the CTLE with AC gain (USB 3.1) used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [USB 3.1]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR (MHz)	Pole2HBR	(Accepts user-defined text), 2500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR No Cable Model (MHz)	Pole2HBRNoCable	(Accepts user-defined text), 2500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR2 (MHz)	Pole2HBR2	(Accepts user-defined text), 3000, 4500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR2 No Cable Model (MHz)	Pole2HBR2NoCable	(Accepts user-defined text), 3000, 4500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR25 (MHz)	Pole2HBR25	(Accepts user-defined text), 3000, 4500, 13500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR25 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR25 No Cable Model (MHz)	Pole2HBR25NoCable	(Accepts user-defined text), 3000, 4500, 5625, 13500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR25 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR3 (MHz)	Pole2HBR3	(Accepts user-defined text), 3000, 4500, 6000, 10000, 13500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - HBR3 No Cable Model (MHz)	Pole2HBR3NoCable	(Accepts user-defined text), 3000, 4500, 6000, 10000, 13500	Set the pole 2 frequency of the 2/3 Poles CTLE used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 2 Frequency (CTLE Without AC Gain) - RBR (MHz)	Pole2RBR	(Accepts user-defined text), 20000	Set the pole 2 frequency of the 2/3 Poles CTLE used for RBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 3 Frequency (CTLE Without AC Gain) - HBR2 (MHz)	Pole3HBR2	(Accepts user-defined text), 5000, 13500	Set the pole 3 frequency of the 2/3 Poles CTLE used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Pole 3 Frequency (CTLE Without AC Gain) - HBR2 No Cable Model (MHz)	Pole3HBR2NoCable	(Accepts user-defined text), 5000, 13500	Set the pole 3 frequency of the 2/3 Poles CTLE used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 3 Frequency (CTLE Without AC Gain) - HBR25 (MHz)	Pole3HBR25	(Accepts user-defined text), 5000, 13500	Set the pole 3 frequency of the 2/3 Poles CTLE used for HBR25 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Pole 3 Frequency (CTLE Without AC Gain) - HBR25 No Cable Model (MHz)	Pole3HBR25NoCable	(Accepts user-defined text), 5000, 13500, 15600	Set the pole 3 frequency of the 2/3 Poles CTLE used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	PostCursor2 Edges	PostCursor2Edge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges measured for the PostCursor2 verification test.
Configure	Pre-Emphasis Level Edges	PreEmphasisEdge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges used for the Pre-Emphasis Level Test.
Configure	Probe Check (AUX Channel Tests)	AUXProbeCheck	Enable, Disable	Select to enable or disable probe check for AUX Channel Tests.
Configure	Probe Check (Dual Mode Tests)	DualModeProbeCheck	true, false	Select to enable or disable probe check for Dual Mode Tests.
Configure	Probe Check (Physical Layer Tests)	PhysicalLayerTestsProbeCheck	Enable, Disable	Select to enable or disable probe check for Physical Layer Tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Random Noise End Location (EZJIT Complete)	RandomNoise_EndLocation	(Accepts user-defined text), 0.5, 0.6, 0.7, 0.8, 0.9	Set the end location for the random noise measurement in Eye Diagram Test (TP3_EQ). This configuration only applicable when the [Random Noise Measurement Method (TP3_EQ)] configuration variable is set to [EZJIT Complete]. Unit: UI.
Configure	Random Noise Measurement Method (TP3_EQ)	RandomNoiseMeasMethod	Histogram, EZJITComplete, SpecifyRN	Select the random noise measurement method in Eye Diagram Test (TP3_EQ). This configuration only applicable if the random jitter and noise derate included in the eye mask generation. For [Histogram] method, histogram is used to perform random noise measurement. For [EZJIT Complete], EZJIT Complete is used to perform random noise measurement. For [Specify RN], specified [Random Noise High] and [Random Noise Low] are used for random noise.
Configure	Random Noise Measurement Number (EZJIT Complete)	RandomNoise_MeasNumber	(Accepts user-defined text), 1, 5, 10, 15, 20	Set the measurement number for the random noise measurement in Eye Diagram Test (TP3_EQ). If measurement number set to one, the random noise measurement will be performed at [Random Noise Start Location]. This configuration only applicable when the [Random Noise Measurement Method (TP3_EQ)] configuration variable is set to [EZJIT Complete].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Random Noise NBit Start (VHigh) - Arbitrary Pattern	NBitStartRNoiseVHighArbitraryPattern	(Accepts user-defined text), 7, 10	Set the bit location of the serial pattern search where the Arbitrary Pattern's High Level (VHigh) random noise measurement start performed in Eye Diagram Test (TP3_EQ). The start location must be within the serial pattern search specified in [Random Noise Serial Pattern (VHigh) - Arbitrary Pattern] configuration variable.
Configure	Random Noise NBit Start (VHigh) - HBR2CPAT	TP3_EQ_NBit_Start_Top	(Accepts user-defined text), 7, 10	Set the bit location of the serial pattern search where the HBR2CPAT's High Level (VHigh) random noise measurement start performed in Eye Diagram Test (TP3_EQ). The start location must be within the serial pattern search specified in [Random Noise Serial Pattern (VHigh) - HBR2CPAT] configuration variable.
Configure	Random Noise NBit Start (VLow) - Arbitrary Pattern	NBitStartRNoiseVLowArbitraryPattern	(Accepts user-defined text), 4, 6, 7	Set the bit location of the serial pattern search where the Arbitrary Pattern's Low Level (VLow) random noise measurement start performed in Eye Diagram Test (TP3_EQ). The start location must be within the serial pattern search specified in [Random Noise Serial Pattern (VLow) - Arbitrary Pattern] configuration variable.
Configure	Random Noise NBit Start (VLow) - HBR2CPAT	TP3_EQ_NBit_Start_Bottom	(Accepts user-defined text), 4, 6	Set the bit location of the serial pattern search where the HBR2CPAT's Low Level (VLow) random noise measurement start performed in Eye Diagram Test (TP3_EQ). The start location must be within the serial pattern search specified in [Random Noise Serial Pattern (VLow) - HBR2CPAT] configuration variable.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Random Noise Serial Pattern (VHigh) - Arbitrary Pattern	SerialPatternRNoiseVHighArbitraryPattern	(Accepts user-defined text), 010001111, 010001111001, 1010110001110	Set the serial pattern search for Arbitrary Pattern's High Level (VHigh) random noise measurement in Eye Diagram Test (TP3_EQ). This configuration support only 8 bits maximum when the [Random Noise Serial Pattern Eye Method] configuration variable is set to method [SDA Pattern Qualify]. If more than 8 bits is set by user, the first 8 bits will be used for serial pattern search.
Configure	Random Noise Serial Pattern (VHigh) - HBR2CPAT	TP3_EQ_SerialPatternTop	(Accepts user-defined text), 010001111001, 1010110001110	Set the serial pattern search for HBR2CPAT's High Level (VHigh) random noise measurement in Eye Diagram Test (TP3_EQ). This configuration support only 8 bits maximum when the [Random Noise Serial Pattern Eye Method] configuration variable is set to method [SDA Pattern Qualify]. If more than 8 bits is set by user, the first 8 bits will be used for serial pattern search.
Configure	Random Noise Serial Pattern (VLow) - Arbitrary Pattern	SerialPatternRNoiseVLowArbitraryPattern	(Accepts user-defined text), 101110000, 0100001110101, 10001000101	Set the serial pattern search for Arbitrary Pattern's Low Level (VLow) random noise measurement in Eye Diagram Test (TP3_EQ). This configuration support only 8 bits maximum when the [Random Noise Serial Pattern Eye Method] configuration variable is set to method [SDA Pattern Qualify]. If more than 8 bits is set by user, the first 8 bits will be used for serial pattern search.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Random Noise Serial Pattern (VLow) - HBR2CPAT	TP3_EQ_SerialPatternBottom	(Accepts user-defined text), 0100001110101, 10001000101	Set the serial pattern search for HBR2CPAT's Low Level (VLow) random noise measurement in Eye Diagram Test (TP3_EQ). This configuration support only 8 bits maximum when the [Random Noise Serial Pattern Eye Method] configuration variable is set to method [SDA Pattern Qualify]. If more than 8 bits is set by user, the first 8 bits will be used for serial pattern search.
Configure	Random Noise Serial Pattern Eye Method	SerialPatternMethodRandomNoise	UDF Serial Eye, InfiniiScan Generic Serial, SDA Pattern Qualify	Select the serial pattern search method for High Level (VHigh) and Low Level (VLow) random noise measurement in Eye Diagram Test (TP3_EQ).
Configure	Random Noise Start Location (EZJIT Complete)	RandomNoise_StartLocation	(Accepts user-defined text), 0.1, 0.2, 0.3, 0.4, 0.5	Set the start location for the random noise measurement in Eye Diagram Test (TP3_EQ). This configuration only applicable when the [Random Noise Measurement Method (TP3_EQ)] configuration variable is set to [EZJIT Complete]. Unit: UI.
Configure	Random Noise VHigh (mV) (Specify RN)	RandomNoise_High	(Accepts user-defined text), 0.2	Set the High Level (VHigh) random noise (RN) rms in Eye Diagram Test (TP3_EQ). This configuration only applicable when the [Random Noise Measurement Method (TP3_EQ)] configuration variable is set to [Specify RN]. Unit: mV.
Configure	Random Noise VLow (mV) (Specify RN)	RandomNoise_Low	(Accepts user-defined text), 0.2	Set the High Level (VLow) random noise (RN) rms in Eye Diagram Test (TP3_EQ). This configuration only applicable when the [Random Noise Measurement Method (TP3_EQ)] configuration variable is set to [Specify RN]. Unit: mV.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Reference Device AUX Channel Voltage Swing (mV)	AUXSensitivityTestLevel	(Accepts user-defined text), 240, 250, 260, 270, 280	Set the AUX Channel voltage swing set to the reference device for AUX Channel Calibration Test. Unit: mV.
Configure	Reference Sink Embedding	ReferenceSinkEmbedding	True, False	Select whether to include reference sink model embedding when running tests at TP_RX_DFE test point.
Configure	Reference Sink Model Type	ReferenceSinkModelType	Reference_Sink_Model	Select the type of reference sink model to be embedded when running tests at TP_RX_DFE test point.
Configure	Rise-Fall MisMatch Edges	RiseFallMisMatchEdge	(Accepts user-defined text), 100, 1000	Set the number of edges measured for the Rise-Fall Time Mismatch Test.
Configure	Rise-Fall Time Mismatch Threshold	MisMatchThreshold	90/10, 85/15, 80/20, 75/25, 70/30	Set the threshold used for the Rise-Fall Time Mismatch Test.
Configure	Rm Resistance (ohm)	InrushTestRmResistance	(Accepts user-defined text), 0.05, 0.1, 1.0	Set the resistance value of the Rm resistor used for Inrush Tests. Unit: ohm.
Configure	Rx Test Lane DC Block Delay Time (ps)	RxTestLaneDCBlockDelayTime	(Accepts user-defined text), 113, 118	Set the Rx test lane DC block delay time to be removed. Select [118]ps for typical delay time of N9398C or N9399C. Select [113]ps for typical delay time of 11742A. This configuration only applicable when the [Rx Test Lane DC Block Delay Time Removal] configuration variable is set to [Enable] for [DPoC] and [DPoC 1.4a] Test Specification. Unit: ps.
Configure	Rx Test Lane DC Block Delay Time Removal	RxTestLaneDCBlockDelayTimeRemoval	Disable, Enable	Select to enable or disable Rx test lane DC block delay time removal. This configuration only applicable for [DPoC] and [DPoC 1.4a] Test Specification.
Configure	SCPI Command Timeout	SCPITimeout	(Accepts user-defined text), 80000, 160000	Define the timeout period for scpi command sent to scope in miliseconds.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	SSC Acquisitions	SSCCount	(Accepts user-defined text), 10, 20	Number of SSC cycle captured for SSC related tests. Max number is 25.
Configure	SSC Filter Frequency (MHz)	SSCFilterFrequency	(Accepts user-defined text), Auto, 5.00, 1.98, 1.70	Set the cutoff fequency of the low pass filter used for SSC related tests. Unit: MHz. This configuration only applicable when the [SSC Filter Type] config variable is set to [Second Order Butterwoth Filter]. For [Auto], the DisplayPort application will set the cutoff frequency of the low pass filter based on Test Specification selected, which is: 1.98MHz for DP 1.4, 1.2b, DPoC, MyDP 1.0 and MyDP HBR25 5.00MHz for DP 1.4a, DPoC 1.4a and above Test Specification
Configure	SSC Filter Type	SSCFilterType	Butterworth2, SmoothingFilter	Select the type of the low pass filter used for SSC related tests.
Configure	SSC Smoothing Points - HBR	SSCSmoothPointsHigh	(Accepts user-defined text), 61, 603, 701	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - HBR2	SSCSmoothPointsHBR2	(Accepts user-defined text), 120, 1206, 1402	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR2. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - HBR25	SSCSmoothPointsHBR25	(Accepts user-defined text), 120, 1206, 1402	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR25. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	SSC Smoothing Points - HBR3	SSCSmoothPointsHBR3	(Accepts user-defined text), 120, 1206, 1402, 1810	Set the number of smoothing points of the low pass filter used for SSC related tests for HBR3. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	SSC Smoothing Points - RBR	SSCSmoothPointsLow	(Accepts user-defined text), 37, 361, 401	Set the number of smoothing points of the low pass filter used for SSC related tests for RBR. This configuration only applicable when the [SSC Filter Type] config variable is set to [Smoothing Filter].
Configure	Sampling Rate (GSa/s) (AUX Channel Tests)	AUXSamplingRate	5, 10, 20, 40, 80, 8, 16, 32, 64	Set the acquisition sampling rate of the oscilloscope for AUX Channel Tests. Unit: GSa/s.
Configure	Sampling Rate (GSa/s) (Dual Mode Tests)	DualModeTestSamplingRate	20, 40, 80, 32, 64, 128	Set the acquisition sampling rate of the oscilloscope for Dual Mode Tests. Unit: GSa/s.
Configure	Sampling Rate (GSa/s) (Inrush Tests)	InrushTestSamplingRate	1, 2, 5, 10, 20, 40, 80, 8, 16, 32, 64	Set the acquisition sampling rate of the oscilloscope for Inrush Tests. Unit: GSa/s.
Configure	Sampling Rate (GSa/s) (Low Frequency Uncorrelated Deterministic Jitter)	UDJ_LF_SamplingRate	20, 40, 80, 32, 64, 128	Set the acquisition sampling rate of the oscilloscope for Low Frequency Uncorrelated Deterministic Jitter Tests. Note: If the selected sampling rate is not available in the oscilloscope, the DisplayPort application will use the highest sampling rate available in the oscilloscope. Unit: GSa/s.
Configure	Sampling Rate (MSa/s) (AUX Channel Sensitivity Test)	AUXSensitivitySamplingRate	5, 10, 20, 40, 80, 8, 16, 32, 64	Set the acquisition sampling rate of the oscilloscope for AUX Channel Sensitivity Test. Unit: MSa/s.
Configure	Screenshot	ScreenshotEnable	Enable, Disable	Select to enable or disable screenshot for all tests except Eye Diagram Tests and Eye Diagram Tests (TP3_EQ).

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Screenshot File Format	ScreenshotFileFormat	8bpp Format, 24bpp Format	Select the screenshot file format for all tests. For [8bpp Format], the DisplayPort application will convert the image file format from 24bpp to 8bpp to reduce the project file size. However, this setting will increase the wait time after the test completed or stopped as the image file convertion only happens at the run ended.
Configure	Search Pattern	DMInterPairSkewSearchPattern	(Accepts user-defined text)	Define the search pattern for the Dual Mode Inter Pair Skew Test. For [Auto], the application will search for "00101010110010101011", "0010101010010101010", "1101010100110101010100" or "1101010101110101010101" pattern.
Configure	Serial Pattern Eye Method (Voltage Level)	SerialPatternEyeMethod	1, 2	Set the search method for serial pattern in High Level (VHigh) and Low Level (VLow) measurements.
Configure	Single-Ended Vertical Offset (mV)	FixedSingleEndedVerticalOffset	(Accepts user-defined text), 0	Set the fixed value used for the vertical offset of single-ended signal for RBR, HBR, HBR2 and HBR3. This configuration only applicable when the [Identical Vertical Scale Mode] configuration variable is set to [Fixed]. Unit: mV.
Configure	Sink AUX Channel Traffic Timeout (us)	SinkAUXTimeout	(Accepts user-defined text), 300, 400	Set the timeout period where sink need to reply for source AUX command. This configuration only applicable when the [Test Method] configuration variable is set to oscilloscope decode method [Scope Method]. Unit: us.
Configure	Sink Data Rate Measurement	SinkDataRateMeasurement	(Accepts user-defined text), Data, Clock	Specify the method to measure data rate on waveform. User can specifically enter the Data rate by themselves.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Sink Equalizer	SinkEqualizer	2, 5, 10, Manual, Off	Select the equalization to be use for the Sink Tests. For [User Defined File], user need to provide custom user defined Equalization Coefficient file.
Configure	Sink Mask	SinkMask	TP2, TP3	Selects the type of mask to use for the eye test. (TP2 for Source; TP3 for Sink)
Configure	Sink Mask Movement	SinkMaskMovement	Fixed, FindPass, FindMargin	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Configure	Source AUX Channel Traffic Timeout (us)	SourceAUXTimeout	(Accepts user-defined text), 300, 400	Set the timeout period where source need to wait for sink reply before transmitting the next AUX command. This configuration only applicable when the [Test Method] configuration variable is set to oscilloscope decode method [Scope Method]. Unit: us.
Configure	Tap 1 Value - HBR2	DFE_Tap1Value_HBR2	(Accepts user-defined text), 0.005	Set the tap 1 value to be used in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual].
Configure	Tap 1 Value - HBR3	DFE_Tap1Value_HBR3	(Accepts user-defined text), 0.005	Set the tap 1 value to be used in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual].

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Test Method	AUXSensitivityTestMethod	Reference Device Method, Scope Method	Select the test method used for AUX Channel Sensitivity Test to either through built in test from reference device (Reference Device Method) or oscilloscope decode (Scope Method). If the selected reference device does not support built in test, the oscilloscope decode method will be used.
Configure	Test Plan Check Mode	TestPlanCheckerMode	Off, On	Select to turn on or off test plan check mode to simulate actual test plan run flow without actual tests being run.
Configure	Test Plan Check Mode Option	TestPlanCheckModeOption	TurnOnAutomation, ManualInspection, GenerateReport	Select the option for the test plan check mode. This configuration only applicable when the [Test Plan Check Mode] configuration variable is turned on. [Turn on Automation] allows you to verify signal changed through automation by visual inspection for each test plan permutation (if automation is enabled). [Manual Inspection] allows you to run through test plans with DUT settings message being shown. [Generate Report] allows you to run through test plans without message being shown and generate report that shows all test states at the end.
Configure	Threshold Mode	ThresholdMode	Auto, Min Max, Top Base, Absolute Zero	Select the threshold mode to either by VMax/VMin, VTop/VBase or threshold at absolute 0. For [Auto], [Min Max] threshold mode is used for RBR and HBR while [Absolute Zero] threshold mode is used for HBR2 and HBR3.
Configure	Transition Edges	TransitionEdge	(Accepts user-defined text), 100, 500, 1000	Set the number of edges measured for the transition tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Transition VH Pattern	TransitionVHPattern	01111, 0111, 011, 0011	Set the pattern for rise time measurement to either 01111, 0111 or 011. The default setting is 0111.
Configure	Transition VL Pattern	TransitionVLPattern	10000, 1000, 100, 1100	Set the pattern for fall time measurement to either 10000, 1000 or 100. The default setting is 1000.
Configure	Trigger Level (V) (Inrush Tests)	InrushTestTriggerLevel	(Accepts user-defined text), 0.10, 0.25, 0.50, 1.00, 2.00	Set the initial trigger level used to trigger Vd signal for Inrush Tests. Unit: V.
Configure	Trigger Pattern	DMIntraPairSkewTriggerPattern	0000001, 000111, 0011, 01, 0101010, 10101, 010	Define the trigger pattern for the Dual Mode Intra Pair Skew Test.
Configure	Turn Off CTLE	TurnOffCTLE	True, False	Select whether to turn off the CTLE when running tests at TP3_EQ test point.
Configure	Upper Target - HBR2	DFE_UpperTarget_HBR2	(Accepts user-defined text), 1.00	Set the upper value to be used in the DFE equalizer for HBR2 when running tests at TP3_EQ test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual]. Unit: V.
Configure	Upper Target - HBR3	DFE_UpperTarget_HBR3	(Accepts user-defined text), 1.00	Set the upper target value to be used in the DFE equalizer for HBR3 when running tests at TP3_DFE test point. This configuration only applicable when the [DFE Setup] configuration variable is set to [Manual]. Unit: V.
Configure	VH Non Transition Bit Location - Arbitrary Pattern	VHNonTransBitLocation_ArbitraryPattern	(Accepts user-defined text), 2.5, 5.5	Set the pattern bit location used for High Level (VHigh) non transition measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	VH Pattern - Arbitrary Pattern	VHPattern_ArbitraryPattern	(Accepts user-defined text), 011111	Set the serial pattern search for High Level (VHigh) measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test.
Configure	VH Pattern - PRBS 7	VHPattern	10111111, 1011111, 101111	Set the pattern for VH measurement to either 1111110, 11110, 1110 or 110. The default setting is 1111110. Maximum 8 bits only.
Configure	VH Transition Bit Location - Arbitrary Pattern	VHTransBitLocation_ArbitraryPattern	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for High Level (VHigh) transition measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	VL Non Transition Bit Location - Arbitrary Pattern	VLNonTransBitLocation_ArbitraryPattern	(Accepts user-defined text), 2.5, 5.5	Set the pattern bit location used for Low Level (VLow) non transition measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.
Configure	VL Pattern - Arbitrary Pattern	VLPattern_ArbitraryPattern	(Accepts user-defined text), 100000	Set the serial pattern search for Low Level (VLow) measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test.
Configure	VL Pattern - PRBS 7	VLPattern	1010000, 101000	Set the pattern for VL measurement to either 0000001, 00001, 0001 or 001. The default setting is 0000001. Maximum 8 bits only.
Configure	VL Transition Bit Location - Arbitrary Pattern	VLTransBitLocation_Arbitrary Pattern	(Accepts user-defined text), 1.4, 1.7	Set the pattern bit location used for Low Level (VLow) transition measurement in Non-PreEmphasis Level Test and Pre-Emphasis Level Test. Use comma separated location value, such as [x,y]. Where x is the start location, y is the end location.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	VSwing Edges	VSwingCount	(Accepts user-defined text), 20, 50, 100	Set the number of edges required when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
Configure	VTop & VBase Edges	VTopVBaseEdge	(Accepts user-defined text), 10, 50, 100, 500, 1000	Set the number of edges required when performing the VTop and VBase measurements.
Configure	Vc Vertical Scale/Div (V)	InrushTestVcScale	(Accepts user-defined text), 0.1, 0.2, 0.5, 1, 2, 5	Set the initial vertical scale per division of Vc signal for Inrush Tests. (Available for DisplayPort CTS 1.1a and below) Unit: V.
Configure	Vd Vertical Scale/Div (V)	InrushTestVdScale	(Accepts user-defined text), 0.1, 0.2, 0.5, 1, 2, 5	Set the initial vertical scale per division of Vd signal for Inrush Tests. Unit: V.
Configure	Vs Vertical Scale/Div (V)	InrushTestVsScale	(Accepts user-defined text), 0.1, 0.2, 0.5, 1, 2, 5	Set the initial vertical scale per division of Vs signal for Inrush Tests. (Available for DisplayPort CTS 1.2 and above) Unit: V.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR (MHz)	ZeroFrequencyHBR	(Accepts user-defined text), 450, 540, 650, 700, 725	Set the zero frequency of the 2/3 Poles CTLE used for HBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR No Cable Model (MHz)	ZeroFrequencyHBRNoCable	(Accepts user-defined text), 450, 540, 650, 700, 725	Set the zero frequency of the 2/3 Poles CTLE used for HBR tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Zero Frequency (CTLE Without AC Gain) - HBR2 (MHz)	ZeroFrequencyHBR2	(Accepts user-defined text), 450, 540, 640	Set the zero frequency of the 2/3 Poles CTLE used for HBR2 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR2 No Cable Model (MHz)	ZeroFrequencyHBR2NoCable	(Accepts user-defined text), 450, 540, 640	Set the zero frequency of the 2/3 Poles CTLE used for HBR2 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR25 (MHz)	ZeroFrequencyHBR25	(Accepts user-defined text), 450, 540, 640, 1000	Set the zero frequency of the 2/3 Poles CTLE used for HBR25 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR25 No Cable Model (MHz)	ZeroFrequencyHBR25NoCable	(Accepts user-defined text), 450, 540, 640, 1000, 2000	Set the zero frequency of the 2/3 Poles CTLE used for HBR25 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR3 (MHz)	ZeroFrequencyHBR3	(Accepts user-defined text), 450, 505, 540, 640, 1000	Set the zero frequency of the 2/3 Poles CTLE used for HBR3 tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	Zero Frequency (CTLE Without AC Gain) - HBR3 No Cable Model (MHz)	ZeroFrequencyHBR3NoCable	(Accepts user-defined text), 450, 505, 540, 640, 1000	Set the zero frequency of the 2/3 Poles CTLE used for HBR3 tests without cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Configure	Zero Frequency (CTLE Without AC Gain) - RBR (MHz)	ZeroFrequencyRBR	(Accepts user-defined text), 450, 540, 650, 700, 725	Set the zero frequency of the 2/3 Poles CTLE used for RBR tests with cable model at TP3_EQ test point. This configuration only applicable when the [CTLE Model] configuration variable is set to [Normal]. Unit: MHz.
Configure	eDP TP3_EQ Test Pattern Override	eDPTP3_EQ_TestPattern	(Accepts user-defined text), PRBS 7, D10.2, HBR2CPAT	Set the test pattern used for TP3_EQ tests for eDP tests.
Run Tests	Event	RunEvent	(None), Fail, Margin < N, Pass	Names of events that can be used with the StoreMode=Event or RunUntil RunEventAction options
Run Tests	RunEvent=Margin < N: Minimum required margin %	RunEvent_Margin < N_MinPercent	Any integer in range: 0 <= value <= 99	Specify N using the 'Minimum required margin %' control.
Set Up	1.62 Gbps	1.62 Gbps	0.0, 1.0	Enable or disable Bit Rate 1.62 Gbps support. Enable or disable Bit Rate 1.62 Gbps support.
Set Up	2.7 Gbps	2.7 Gbps	0.0, 1.0	Enable or disable Bit Rate 2.7 Gbps support. Enable or disable Bit Rate 2.7 Gbps support.
Set Up	3.24 Gbps	3.24 Gbps	0.0, 1.0	Enable or disable Bit Rate 3.24 Gbps support. Enable or disable Bit Rate 3.24 Gbps support.
Set Up	5.4 Gbps	5.4 Gbps	0.0, 1.0	Enable or disable Bit Rate 5.4 Gbps support. Enable or disable Bit Rate 5.4 Gbps support.
Set Up	6.75 Gbps	6.75 Gbps	0.0, 1.0	Enable or disable Bit Rate 6.75 Gbps support. Enable or disable Bit Rate 6.75 Gbps support.
Set Up	8.1 Gbps	8.1 Gbps	0.0, 1.0	Enable or disable Bit Rate 8.1 Gbps support. Enable or disable Bit Rate 8.1 Gbps support.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	AUX Channel Controller Mode	DPTCMode	Standard DP Test Mode, Link Training Mode	Select the AUX Channel Controller mode for DisplayPort Test Controller (DPTC) automation. Select the AUX Channel Controller mode for DisplayPort Test Controller (DPTC) automation.
Set Up	AUX Channel Differential Vertical Offset	perTextOffset	(Accepts user-defined text)	Set the vertical offset of AUX Channel differential signal in mV. Set the vertical offset of AUX Channel differential signal in mV.
Set Up	AUX Channel Differential Vertical Scale	perTxtVerticalScale	(Accepts user-defined text)	Set the vertical scale of AUX Channel differential signal in mV. Set the vertical scale of AUX Channel differential signal in mV.
Set Up	AUX Channel Holdoff Time	perTxtHoldOffTime	(Accepts user-defined text)	Set the trigger holdoff time used for signal acquisition of AUX Channel Tests in us. Set the trigger holdoff time used for signal acquisition of AUX Channel Tests in us.
Set Up	AUX Channel Lane	AuxLane	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for AUX Channel Lane when using Differential Probe Connection or AUX Plus Lane when using Single-Ended Connection. Select the channel used for AUX Channel Lane when using Differential Probe Connection or AUX Plus Lane when using Single-Ended Connection.
Set Up	AUX Channel Lower Threshold	perTxtAuxLowerThreshold	(Accepts user-defined text)	Set the measurement lower threshold used for AUX Channel Tests in mV. Set the measurement lower threshold used for AUX Channel Tests in mV.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	AUX Channel Single-Ended Vertical Scale	AUXSEChannelScale	(Accepts user-defined text)	Set the vertical scale of AUX Channel single-ended signal in mV when using Single-Ended Connection. Note: AUX+ and AUX- signal share the same vertical scale. Set the vertical scale of AUX Channel single-ended signal in mV when using Single-Ended Connection. Note: AUX+ and AUX- signal share the same vertical scale.
Set Up	AUX Channel Trigger Level	perTxtTriggerLevel	(Accepts user-defined text)	Set the trigger level used for signal acquisition of AUX Channel Tests in mV. Set the trigger level used for signal acquisition of AUX Channel Tests in mV.
Set Up	AUX Channel Upper Threshold	perTxtAuxUpperThreshold	(Accepts user-defined text)	Set the measurement upper threshold used for AUX Channel Tests in mV. Set the measurement upper threshold used for AUX Channel Tests in mV.
Set Up	AUX Minus Channel Lane	AuxMinusLane	Channel 3, Channel 4	Select the channel used for AUX Minus Channel Lane when using Single-Ended Connection. Select the channel used for AUX Minus Channel Lane when using Single-Ended Connection.
Set Up	AUX Minus Channel Probe Offset	ProbeMinusOffset	(Accepts user-defined text)	Set the probe offset in mV of AUX Minus Channel when using Single-Ended Connection. Set the probe offset in mV of AUX Minus Channel when using Single-Ended Connection.
Set Up	AUX Plus Channel Probe Offset	ProbePlusOffset	(Accepts user-defined text)	Set the probe offset in mV of AUX Channel when using Differential Probe Connection or AUX Plus Channel when using Single-Ended Connection. Set the probe offset in mV of AUX Channel when using Differential Probe Connection or AUX Plus Channel when using Single-Ended Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Acquisition Mode (AUX Channel Tests)	AuxChannelAcquisitionMode	Live, Offline	Select the mode used for signal acquisition of AUX Channel Tests. Select the mode used for signal acquisition of AUX Channel Tests.
Set Up	Analyze Device	AnalyzeDevice	GTX1060, NVIDIA_GTX1060, Simulated Waveform, Source	Select the device to analyze if 'Analyze Mode' is selected for 'Capture and Analysis Mode'. Select the device to analyze if 'Analyze Mode' is selected for 'Capture and Analysis Mode'.
Set Up	Arbitrary Pattern Differential Simulated Waveform File	SimulatedArbitraryDifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential Arbitrary Pattern. Set the simulated waveform file for differential Arbitrary Pattern.
Set Up	Arbitrary Pattern Single-Ended Minus Simulated Waveform File	SimulatedArbitrarySingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus Arbitrary Pattern. Set the simulated waveform file for single-ended minus Arbitrary Pattern.
Set Up	Arbitrary Pattern Single-Ended Plus Simulated Waveform File	SimulatedArbitrarySingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus Arbitrary Pattern. Set the simulated waveform file for single-ended plus Arbitrary Pattern.
Set Up	Capture And Analysis Mode	CaptureAnalysisMode	Standard Mode: Capture and analyze live waveform, Capture Mode: Acquire and store waveforms only, Analyze Mode: Analyze captured waveforms	Select the capture and analysis mode if 'Physical Layer Tests' is selected for 'Test Selection'. Select the capture and analysis mode if 'Physical Layer Tests' is selected for 'Test Selection'.
Set Up	Clock (Differential Probe)	DMClk	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Dual Mode Clock when using Differential Probe Connection. Select the channel used for Dual Mode Clock when using Differential Probe Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Clock Minus (Single Ended)	DMClkMinus	Channel 3, Channel 4	Select the channel used for Dual Mode Clock- when using Single-Ended Connection. Select the channel used for Dual Mode Clock- when using Single-Ended Connection.
Set Up	Clock Plus (Single Ended)	DMClkPlus	Channel 1, Channel 2	Select the channel used for Dual Mode Clock+ when using Single-Ended Connection. Select the channel used for Dual Mode Clock+ when using Single-Ended Connection.
Set Up	Comments	Comments	(Accepts user-defined text)	Additional comments. Additional comments.
Set Up	Connection Setup Complete Status	ConnectionSetupComplete	0.0, 1.0	Determine whether the connection setup is completed. Determine whether the connection setup is completed.
Set Up	Connection Type (AUX Channel Tests)	AUXConnectionType	Differential Probe, Single-Ended (A-B)	Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for AUX Channel Tests. Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for AUX Channel Tests.
Set Up	Connection Type (Dual Mode Tests)	DMConnectionType	Differential Probe, Single-Ended (A-B)	Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Dual Mode Tests. Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Dual Mode Tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Connection Type (Physical Layer Tests)	ConnectionType	Differential Probe, Single-Ended (A-B)	Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Physical Layer Tests. If 'Single-Ended Tests' or 'Both' is selected for 'Test Type', only 'Single-Ended (A-B)' connection will be available. Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Physical Layer Tests. If 'Single-Ended Tests' or 'Both' is selected for 'Test Type', only 'Single-Ended (A-B)' connection will be available.
Set Up	Connection Type (Physical Layer Tests)	WaveformConnectionType	Differential Probe, Single-Ended (A-B)	Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Physical Layer Tests. If 'Single-Ended Tests' or 'Both' is selected for 'Test Type', only 'Single-Ended (A-B)' connection will be available. Select the connection type, either 'Differential Probe' connection or 'Single-Ended (A-B)' connection for Physical Layer Tests. If 'Single-Ended Tests' or 'Both' is selected for 'Test Type', only 'Single-Ended (A-B)' connection will be available.
Set Up	Connector Type	ConnectorType	Standard DP/mDP, USB Type-C	Select the connector type, either 'Standard DP/mDP' or 'USB Type-C'. Note: The connector type will affects the cable model used for TP3_EQ tests. Select the connector type, either 'Standard DP/mDP' or 'USB Type-C'. Note: The connector type will affects the cable model used for TP3_EQ tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Consumer Power Profile 1	ConsumerPowerProfile1	0.0, 1.0	Enable or disable Consumer Power Profile 1 support. Enable or disable Consumer Power Profile 1 support.
Set Up	Consumer Power Profile 2	ConsumerPowerProfile2	0.0, 1.0	Enable or disable Consumer Power Profile 2 support. Enable or disable Consumer Power Profile 2 support.
Set Up	Consumer Power Profile 3	ConsumerPowerProfile3	0.0, 1.0	Enable or disable Consumer Power Profile 3 support. Enable or disable Consumer Power Profile 3 support.
Set Up	D10.2 Differential Simulated Waveform File	SimulatedD102DifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential D10.2. Set the simulated waveform file for differential D10.2.
Set Up	D10.2 Single-Ended Minus Simulated Waveform File	SimulatedD102SingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus D10.2. Set the simulated waveform file for single-ended minus D10.2.
Set Up	D10.2 Single-Ended Plus Simulated Waveform File	SimulatedD102SingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus D10.2. Set the simulated waveform file for single-ended plus D10.2.
Set Up	DPTC Automation Script File	perTxtScript	(Accepts user-defined text)	Select the script file for DisplayPort Test Controller (DPTC) automation. This script file only applicable if script mode is enabled. Select the script file for DisplayPort Test Controller (DPTC) automation. This script file only applicable if script mode is enabled.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	DPTC Configuration	AutomationConfig	(Accepts user-defined text)	Configure the DisplayPort Test Controller (DPTC) remotely. Note: The DisplayPort Test Controller must be enabled before configure the DisplayPort Test Controller remotely. Configure the DisplayPort Test Controller (DPTC) remotely. Note: The DisplayPort Test Controller must be enabled before configure the DisplayPort Test Controller remotely.
Set Up	DUT Orientation (USB Type-C)	TypeCDUTOrientation	Normal, Inverted	Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT. Select the orientation type, either 'Normal' or 'Inverted' for USB Type-C DUT.
Set Up	Data 0 (Differential Probe)	DMD0	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Dual Mode Data 0 when using Differential Probe Connection. Select the channel used for Dual Mode Data 0 when using Differential Probe Connection.
Set Up	Data 0 Minus (Single Ended)	DMD0Minus	Channel 3, Channel 4	Select the channel used for Dual Mode Data 0- when using Single-Ended Connection. Select the channel used for Dual Mode Data 0- when using Single-Ended Connection.
Set Up	Data 0 Plus (Single Ended)	DMD0Plus	Channel 1, Channel 2	Select the channel used for Dual Mode Data 0+ when using Single-Ended Connection. Select the channel used for Dual Mode Data 0+ when using Single-Ended Connection.
Set Up	Data 1 (Differential Probe)	DMD1	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Dual Mode Data 1 when using Differential Probe Connection. Select the channel used for Dual Mode Data 1 when using Differential Probe Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Data 1 Minus (Single Ended)	DMD1Minus	Channel 3, Channel 4	Select the channel used for Dual Mode Data 1- when using Single-Ended Connection. Select the channel used for Dual Mode Data 1- when using Single-Ended Connection.
Set Up	Data 1 Plus (Single Ended)	DMD1Plus	Channel 1, Channel 2	Select the channel used for Dual Mode Data 1+ when using Single-Ended Connection. Select the channel used for Dual Mode Data 1+ when using Single-Ended Connection.
Set Up	Data 2 (Differential Probe)	DMD2	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Dual Mode Data 2 when using Differential Probe Connection. Select the channel used for Dual Mode Data 2 when using Differential Probe Connection.
Set Up	Data 2 Minus (Single Ended)	DMD2Minus	Channel 3, Channel 4	Select the channel used for Dual Mode Data 2- when using Single-Ended Connection. Select the channel used for Dual Mode Data 2- when using Single-Ended Connection.
Set Up	Data 2 Plus (Single Ended)	DMD2Plus	Channel 1, Channel 2	Select the channel used for Dual Mode Data 2+ when using Single-Ended Connection. Select the channel used for Dual Mode Data 2+ when using Single-Ended Connection.
Set Up	Data Pattern	DataPattern	Standard DP Pattern, Arbitrary Pattern	Select the data pattern, either 'Standard DP Pattern' or 'Arbitrary Pattern'. Select the data pattern, either 'Standard DP Pattern' or 'Arbitrary Pattern'.
Set Up	De-Embed Fixture	DeEmbedFixture	0.0, 1.0	Enable or disable fixture de-embedding based on the 'Fixture Type' selected. Enable or disable fixture de-embedding based on the 'Fixture Type' selected.
Set Up	Device ID	DeviceID	(Accepts user-defined text)	Device identifier. Device identifier.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Device Type (AUX Channel Tests)	AUXDUTType	Source, Sink	Select the device type, either 'Source' or 'Sink' for AUX Channel Tests. Select the device type, either 'Source' or 'Sink' for AUX Channel Tests.
Set Up	Device Type (Dual Mode Tests)	DualModeDUTType	Source	Select the device type, only 'Source' for Dual Mode Tests. Select the device type, only 'Source' for Dual Mode Tests.
Set Up	Device Type (Physical Layer Tests)	DUTType	Source, Sink, Cable	Select the device type, either 'Source', 'Sink' or 'Cable' for Physical Layer Tests. Select the device type, either 'Source', 'Sink' or 'Cable' for Physical Layer Tests.
Set Up	DisplayPort Alt Mode	DPAltMode	Alt Mode: DP 4 Lanes, Alt Mode: DP 2 + 2	Select the DisplayPort Alt Mode supported by the DUT, either 'DP 4 Lanes' or 'DP 2 + 2'. Select the DisplayPort Alt Mode supported by the DUT, either 'DP 4 Lanes' or 'DP 2 + 2'.
Set Up	DisplayPort Test Controller	AutomatedType	TCPIP, UnigrafDPTC	Select the DisplayPort Test Controller (DPTC) used for automation. Select the DisplayPort Test Controller (DPTC) used for automation.
Set Up	Enable DPTC Automation	pcbEnableAutomation	0.0, 1.0	Enable or disable DisplayPort Test Controller (DPTC) automation. Enable or disable DisplayPort Test Controller (DPTC) automation.
Set Up	Enable Type-C Controller Automation	EnableTypeCTestController	0.0, 1.0	Enable or disable USB Type-C Test Controller automation. Enable or disable USB Type-C Test Controller automation.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Fixture Type	FixtureType	Wilder Tech DP-TPA-P/ BIT-DP-PTF-0003, Wilder Tech mDP-TPA-P/ BIT-mDP-PTF-000 1, Keysight W2641B, Luxshare ICT mDP Plug, Other	Select the fixture type based on the actual fixture used for the test. If the actual fixture used is not listed, please select 'Other'. Select the fixture type based on the actual fixture used for the test. If the actual fixture used is not listed, please select 'Other'.
Set Up	HBR2 Preferred Level Setting with Cable Model	PreferredLevelPreEmphasis	Swing 0/ Pre-emphasis 0/ PC2 Level 0, Swing 0/ Pre-emphasis 1/ PC2 Level 0, Swing 0/ Pre-emphasis 2/ PC2 Level 0, Swing 1/ Pre-emphasis 0/ PC2 Level 0, Swing 1/ Pre-emphasis 1/ PC2 Level 0, Swing 1/ Pre-emphasis 2/ PC2 Level 0, Swing 2/ Pre-emphasis 0/ PC2 Level 0, Swing 2/ Pre-emphasis 1/ PC2 Level 0	Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR2 TP3_EQ tests with cable model. Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR2 TP3_EQ tests with cable model.
Set Up	HBR2 Preferred Level Setting with No Cable Model	PreferredNoCableLevelPreE mphasis	Swing 0/ Pre-emphasis 0/ PC2 Level 0, Swing 0/ Pre-emphasis 1/ PC2 Level 0, Swing 0/ Pre-emphasis 2/ PC2 Level 0, Swing 1/ Pre-emphasis 0/ PC2 Level 0, Swing 1/ Pre-emphasis 1/ PC2 Level 0, Swing 1/ Pre-emphasis 2/ PC2 Level 0, Swing 2/ Pre-emphasis 0/ PC2 Level 0, Swing 2/ Pre-emphasis 1/ PC2 Level 0	Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR2 TP3_EQ tests with no cable model. Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR2 TP3_EQ tests with no cable model.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	HBR2CPAT Differential Simulated Waveform File	SimulatedHBR2CPATDifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential HBR2CPAT. Set the simulated waveform file for differential HBR2CPAT.
Set Up	HBR2CPAT Single-Ended Minus Simulated Waveform File	SimulatedHBR2CPATSingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus HBR2CPAT. Set the simulated waveform file for single-ended minus HBR2CPAT.
Set Up	HBR2CPAT Single-Ended Plus Simulated Waveform File	SimulatedHBR2CPATSingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus HBR2CPAT. Set the simulated waveform file for single-ended plus HBR2CPAT.
Set Up	HBR3 Preferred Level Setting with Cable Model	HBR3PreferredLevelPreEmphasis	Swing 0/ Pre-emphasis 0/ PC2 Level 0, Swing 0/ Pre-emphasis 1/ PC2 Level 0, Swing 0/ Pre-emphasis 2/ PC2 Level 0, Swing 1/ Pre-emphasis 0/ PC2 Level 0, Swing 1/ Pre-emphasis 1/ PC2 Level 0, Swing 1/ Pre-emphasis 2/ PC2 Level 0, Swing 2/ Pre-emphasis 0/ PC2 Level 0, Swing 2/ Pre-emphasis 1/ PC2 Level 0	Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR3 TP3_EQ tests with cable model. Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR3 TP3_EQ tests with cable model.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	HBR3 Preferred Level Setting with No Cable Model	HBR3PreferredNoCableLevel PreEmphasis	Swing 0/ Pre-emphasis 0/ PC2 Level 0, Swing 0/ Pre-emphasis 1/ PC2 Level 0, Swing 0/ Pre-emphasis 2/ PC2 Level 0, Swing 1/ Pre-emphasis 0/ PC2 Level 0, Swing 1/ Pre-emphasis 1/ PC2 Level 0, Swing 1/ Pre-emphasis 2/ PC2 Level 0, Swing 2/ Pre-emphasis 0/ PC2 Level 0, Swing 2/ Pre-emphasis 1/ PC2 Level 0	Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR3 TP3_EQ tests with no cable model. Select the preferred voltage level, pre-emphasis level and post-cursor 2 level for HBR3 TP3_EQ tests with no cable model.
Set Up	Lane	Lane	1 Lane, 2 Lanes, 4 Lanes	Select the number of lane(s) supported by the DUT. Select the number of lane(s) supported by the DUT.
Set Up	Lane 0 (Differential Probe)	Lane0	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Lane 0 when using Differential Probe Connection. Select the channel used for Lane 0 when using Differential Probe Connection.
Set Up	Lane 0 Minus (Single Ended)	Lane0Minus	Channel 3, Channel 4	Select the channel used for Lane 0- when using Single-Ended Connection. Select the channel used for Lane 0- when using Single-Ended Connection.
Set Up	Lane 0 Plus (Single Ended)	Lane0Plus	Channel 1, Channel 2	Select the channel used for Lane 0+ when using Single-Ended Connection. Select the channel used for Lane 0+ when using Single-Ended Connection.
Set Up	Lane 1 (Differential Probe)	Lane1	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Lane 1 when using Differential Probe Connection. Select the channel used for Lane 1 when using Differential Probe Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Lane 1 Minus (Single Ended)	Lane1Minus	Channel 3, Channel 4	Select the channel used for Lane 1- when using Single-Ended Connection. Select the channel used for Lane 1- when using Single-Ended Connection.
Set Up	Lane 1 Plus (Single Ended)	Lane1Plus	Channel 1, Channel 2	Select the channel used for Lane 1+ when using Single-Ended Connection. Select the channel used for Lane 1+ when using Single-Ended Connection.
Set Up	Lane 2 (Differential Probe)	Lane2	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Lane 2 when using Differential Probe Connection. Select the channel used for Lane 2 when using Differential Probe Connection.
Set Up	Lane 2 Minus (Single Ended)	Lane2Minus	Channel 3, Channel 4	Select the channel used for Lane 2- when using Single-Ended Connection. Select the channel used for Lane 2- when using Single-Ended Connection.
Set Up	Lane 2 Plus (Single Ended)	Lane2Plus	Channel 1, Channel 2	Select the channel used for Lane 2+ when using Single-Ended Connection. Select the channel used for Lane 2+ when using Single-Ended Connection.
Set Up	Lane 3 (Differential Probe)	Lane3	Channel 1, Channel 2, Channel 3, Channel 4	Select the channel used for Lane 3 when using Differential Probe Connection. Select the channel used for Lane 3 when using Differential Probe Connection.
Set Up	Lane 3 Minus (Single Ended)	Lane3Minus	Channel 3, Channel 4	Select the channel used for Lane 3- when using Single-Ended Connection. Select the channel used for Lane 3- when using Single-Ended Connection.
Set Up	Lane 3 Plus (Single Ended)	Lane3Plus	Channel 1, Channel 2	Select the channel used for Lane 3+ when using Single-Ended Connection. Select the channel used for Lane 3+ when using Single-Ended Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Lane A (2 Lanes and 4 Lanes, Differential Probe, Physical Layer Tests)	LaneA	Lane 0	Select the first lane (Lane A) if number of channels is less than number of lanes when using Differential Probe Connection. Select the first lane (Lane A) if number of channels is less than number of lanes when using Differential Probe Connection.
Set Up	Lane A (2 Lanes and 4 Lanes, Single-Ended, Physical Layer Tests)	LaneASMA	Lane 0	Select the first lane (Lane A) if number of channels is less than number of lanes when using Single-Ended Connection. Select the first lane (Lane A) if number of channels is less than number of lanes when using Single-Ended Connection.
Set Up	Lane A (Differential Probe, Dual Mode Tests)	DMLaneADiff	Clock	Select the first lane (Lane A) if number of channels is less than number of lanes when using Differential Probe Connection. Select the first lane (Lane A) if number of channels is less than number of lanes when using Differential Probe Connection.
Set Up	Lane A (Single-Ended, Dual Mode Tests)	DMLaneASMA	Clock	Select the first lane (Lane A) if number of channels is less than number of lanes when using Single-Ended Connection. Select the first lane (Lane A) if number of channels is less than number of lanes when using Single-Ended Connection.
Set Up	Lane B (4 Lanes, Differential Probe, Physical Layer Tests)	LaneB	Lane 0	Select the second lane (Lane B) if number of channels is less than number of lanes when using Differential Probe Connection. Select the second lane (Lane B) if number of channels is less than number of lanes when using Differential Probe Connection.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Lane B (4 Lanes, Single-Ended, Physical Layer Tests)	LaneBSMA	Lane 0	Select the second lane (Lane B) if number of channels is less than number of lanes when using Single-Ended Connection. Select the second lane (Lane B) if number of channels is less than number of lanes when using Single-Ended Connection.
Set Up	Lane B (Differential Probe, Dual Mode Tests)	DMLaneBDiff	Data 0, Data 1, Data 2	Select the second lane (Lane B) if number of channels is less than number of lanes when using Differential Probe Connection. Select the second lane (Lane B) if number of channels is less than number of lanes when using Differential Probe Connection.
Set Up	Lane B (Single-Ended, Dual Mode Tests)	DMLaneBSMA	Data 0, Data 1, Data 2	Select the second lane (Lane B) if number of channels is less than number of lanes when using Single-Ended Connection. Select the second lane (Lane B) if number of channels is less than number of lanes when using Single-Ended Connection.
Set Up	N7015A Cable	N7015ACable	Without Cable, With Cable	Select whether the N7015A fixture include additional cable. Select whether the N7015A fixture include additional cable.
Set Up	No of Channels (Dual Mode Tests)	DMConnectionChannels	2 Channels, 4 Channels	Select the number of channel(s) based on the actual number of channel(s) used for Dual Mode Tests. Select the number of channel(s) based on the actual number of channel(s) used for Dual Mode Tests.
Set Up	No of Channels (Physical Layer Tests)	ConnectionSetting	1 Channel	Select the number of channel(s) based on the actual number of channel(s) used for Physical Layer Tests. Select the number of channel(s) based on the actual number of channel(s) used for Physical Layer Tests.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Number of Save Waveform (AUX Channel Tests)	perTxtAcquisitionNo	(Accepts user-defined text)	Set the number of waveform to be saved for offline processing of AUX Channel Tests. Set the number of waveform to be saved for offline processing of AUX Channel Tests.
Set Up	Operator ID	OperatorID	(Accepts user-defined text)	Operator identifier. Operator identifier.
Set Up	PCTPAT Differential Simulated Waveform File	SimulatedPCTPATDifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential PCTPAT. Set the simulated waveform file for differential PCTPAT.
Set Up	PCTPAT Single-Ended Minus Simulated Waveform File	SimulatedPCTPATSingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus PCTPAT. Set the simulated waveform file for single-ended minus PCTPAT.
Set Up	PCTPAT Single-Ended Plus Simulated Waveform File	SimulatedPCTPATSingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus PCTPAT. Set the simulated waveform file for single-ended plus PCTPAT.
Set Up	PLTPAT Differential Simulated Waveform File	SimulatedPLTPATDifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential PLTPAT. Set the simulated waveform file for differential PLTPAT.
Set Up	PLTPAT Single-Ended Minus Simulated Waveform File	SimulatedPLTPATSingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus PLTPAT. Set the simulated waveform file for single-ended minus PLTPAT.
Set Up	PLTPAT Single-Ended Plus Simulated Waveform File	SimulatedPLTPATSingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus PLTPAT. Set the simulated waveform file for single-ended plus PLTPAT.
Set Up	PRBS 7 Differential Simulated Waveform File	SimulatedPRBS7DifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential PRBS 7. Set the simulated waveform file for differential PRBS 7.
Set Up	PRBS 7 Single-Ended Minus Simulated Waveform File	SimulatedPRBS7SingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus PRBS 7. Set the simulated waveform file for single-ended minus PRBS 7.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	PRBS 7 Single-Ended Plus Simulated Waveform File	SimulatedPRBS7SingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus PRBS 7. Set the simulated waveform file for single-ended plus PRBS 7.
Set Up	Post-Cursor 2 Level 0	Level 0	0.0, 1.0	Enable or disable Post-Cursor 2 Level 0 support. Enable or disable Post-Cursor 2 Level 0 support.
Set Up	Post-Cursor 2 Level 1	Level 1	0.0, 1.0	Enable or disable Post-Cursor 2 Level 1 support. Enable or disable Post-Cursor 2 Level 1 support.
Set Up	Post-Cursor 2 Level 2	Level 2	0.0, 1.0	Enable or disable Post-Cursor 2 Level 2 support. Enable or disable Post-Cursor 2 Level 2 support.
Set Up	Post-Cursor 2 Level 3	Level 3	0.0, 1.0	Enable or disable Post-Cursor 2 Level 3 support. Enable or disable Post-Cursor 2 Level 3 support.
Set Up	Pre-emphasis 0	Pre-emphasis 0	0.0, 1.0	Enable or disable Pre-emphasis Level 0 support. Enable or disable Pre-emphasis Level 0 support.
Set Up	Pre-emphasis 1	Pre-emphasis 1	0.0, 1.0	Enable or disable Pre-emphasis Level 1 support. Enable or disable Pre-emphasis Level 1 support.
Set Up	Pre-emphasis 2	Pre-emphasis 2	0.0, 1.0	Enable or disable Pre-emphasis Level 2 support. Enable or disable Pre-emphasis Level 2 support.
Set Up	Pre-emphasis 3	Pre-emphasis 3	0.0, 1.0	Enable or disable Pre-emphasis Level 3 support. Enable or disable Pre-emphasis Level 3 support.
Set Up	Project ID	ProjectID	(Accepts user-defined text)	Project identifier. Project identifier.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Provider Power Profile 1	ProviderPowerProfile1	0.0, 1.0	Enable or disable Provider Power Profile 1 support. Enable or disable Provider Power Profile 1 support.
Set Up	Provider Power Profile 2	ProviderPowerProfile2	0.0, 1.0	Enable or disable Provider Power Profile 2 support. Enable or disable Provider Power Profile 2 support.
Set Up	Provider Power Profile 3	ProviderPowerProfile3	0.0, 1.0	Enable or disable Provider Power Profile 3 support. Enable or disable Provider Power Profile 3 support.
Set Up	Reference Device (AUX Channel Tests)	ReferenceDUTConnectivity	Yes, No	Select whether a reference source or sink is connected for AUX Channel Tests. Select whether a reference source or sink is connected for AUX Channel Tests.
Set Up	SSC	SSCOption	Disabled, Enabled, Both	Select the SSC capability supported by the DUT. Select the SSC capability supported by the DUT.
Set Up	SSC Disabled	SSC Disabled	0.0, 1.0	Enable or disable SSC Disabled support. Enable or disable SSC Disabled support.
Set Up	SSC Enabled	SSC Enabled	0.0, 1.0	Enable or disable SSC Enabled support. Enable or disable SSC Enabled support.
Set Up	Save Waveform Type (AUX Channel Tests)	AUXWaveformType	AUX Channel Tests, AUX Channel Calibration Tests, AUX Channel Sensitivity Tests	Select the type of waveform to be saved for AUX Channel Tests. Select the type of waveform to be saved for AUX Channel Tests.
Set Up	Show Normative Tests Only	HideInformative	0.0, 1.0	Enable or disable show normative tests only. Enable or disable show normative tests only.
Set Up	TMDS Clock Frequency (Dual Mode Tests)	DualModeTMDSClockFrequency	25MHz to 165MHz, 165MHz to 600MHz	Select the TMDS clock frequency range supported by the DUT. Select the TMDS clock frequency range supported by the DUT.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	TPS4 Differential Simulated Waveform File	SimulatedTPS4DifferentialWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for differential TPS4. Set the simulated waveform file for differential TPS4.
Set Up	TPS4 Single-Ended Minus Simulated Waveform File	SimulatedTPS4SingleEndedMinusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended minus TPS4. Set the simulated waveform file for single-ended minus TPS4.
Set Up	TPS4 Single-Ended Plus Simulated Waveform File	SimulatedTPS4SingleEndedPlusWaveformFilePath	(Accepts user-defined text)	Set the simulated waveform file for single-ended plus TPS4. Set the simulated waveform file for single-ended plus TPS4.
Set Up	Test Selection	TestLayer	Physical Layer Tests, AUX PHY and Inrush Tests, Dual Mode Tests, Test Tools	Select the test selection. Select the test selection.
Set Up	Test Setup Complete Status	TestSetupComplete	0.0, 1.0	Determine whether the test setup is completed. Determine whether the test setup is completed.
Set Up	Test Specification	DPCTSVersion	1.2b, 1.4a, 1.4, DPoC 1.4a, DPoC, MyDP 1.0, MyDP HBR25	Select the test specification. Select the test specification.
Set Up	Test Tools	TestTools	CTLE Optimization	Select the test tools if 'Test Tools' is selected for 'Test Selection'. Select the test tools if 'Test Tools' is selected for 'Test Selection'.

Table 2 Configuration Variables and Values (continued)

GUI Location	Label	Variable	Values	Description
Set Up	Test Type	TestType	Differential Tests, Single-Ended Tests, Both	Select the test type, either 'Differential Tests', 'Single-Ended Tests' or 'Both' if 'Source' is selected for 'Device Type'. Note: For 'Both', both differential tests and single-ended tests will be available with single-ended connection. Select the test type, either 'Differential Tests', 'Single-Ended Tests' or 'Both' if 'Source' is selected for 'Device Type'. Note: For 'Both', both differential tests and single-ended tests will be available with single-ended connection.
Set Up	Voltage Level Swing 0	Swing 0	0.0, 1.0	Enable or disable Voltage Level Swing 0 support. Enable or disable Voltage Level Swing 0 support.
Set Up	Voltage Level Swing 1	Swing 1	0.0, 1.0	Enable or disable Voltage Level Swing 1 support. Enable or disable Voltage Level Swing 1 support.
Set Up	Voltage Level Swing 2	Swing 2	0.0, 1.0	Enable or disable Voltage Level Swing 2 support. Enable or disable Voltage Level Swing 2 support.
Set Up	Voltage Level Swing 3	Swing 3	0.0, 1.0	Enable or disable Voltage Level Swing 3 support. Enable or disable Voltage Level Swing 3 support.
Set Up	Waveform Setup Complete Status	WaveformSetupComplete	0.0, 1.0	Determine whether the waveform setup is completed. Determine whether the waveform setup is completed.

3 Test Names and IDs

The following table shows the mapping between each test's numeric ID and name. The numeric ID is required by various remote interface methods.

- Name – The name of the test as it appears on the user interface **Select Tests** tab.
- Test ID – The number to use with the RunTests method.
- Description – The description of the test as it appears on the user interface **Select Tests** tab.

For example, if the graphical user interface displays this tree in the **Select Tests** tab:

- All Tests
  - Rise Time
  - Fall Time

then you would expect to see something like this in the table below:

Table 3 Example Test Names and IDs

Name	Test ID	Description
Fall Time	110	Measures clock fall time.
Rise Time	100	Measures clock rise time.

and you would run these tests remotely using:

```
ARSL syntax
-----------
arsl -a ipaddress -c "SelectedTests '100,110'"
arsl -a ipaddress -c "Run"

C# syntax
---------
remoteAte.SelectedTests = new int[]{100,110};
remoteAte.Run();
```

Here are the actual Test names and IDs used by this application. Listed at the end, you may also find:

- Deprecated IDs and their replacements.
- Macro IDs which may be used to select multiple related tests at the same time.

NOTE The file, "TestInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 4 Test IDs and Names

Name	TestID	Description
3.1 Lane 0 - Eye Diagram Test (TP2_CTLE) - Arbitrary Pattern	1316011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP2_CTLE) - TPS4	1216011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_CTLE) - Arbitrary Pattern	1316001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_CTLE) - TPS4	1216001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - TPS4	1218001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_DFE) - Arbitrary Pattern	1317001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_DFE) - TPS4	1217001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 0 - Eye Diagram Test (TP3_EQ) - Arbitrary Pattern	1315001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	1215001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP3_EQ) - PRBS 7	1211001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP_RX_DFE) - Arbitrary Pattern	1319001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test (TP_RX_DFE) - TPS4	1219001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test - Arbitrary Pattern	1310001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test - PRBS 7	1210001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - TPS4	1218011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1317011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_DFE) - TPS4	1217011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1315011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	1215011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS 7	1211011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - Arbitrary Pattern	1319011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 0 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - TPS4	1219011	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP2_CTLE) - Arbitrary Pattern	1316012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP2_CTLE) - TPS4	1216012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_CTLE) - Arbitrary Pattern	1316002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_CTLE) - TPS4	1216002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 1 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - TPS4	1218002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_DFE) - Arbitrary Pattern	1317002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_DFE) - TPS4	1217002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_EQ) - Arbitrary Pattern	1315002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	1215002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP3_EQ) - PRBS 7	1211002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP_RX_DFE) - Arbitrary Pattern	1319002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test (TP_RX_DFE) - TPS4	1219002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test - Arbitrary Pattern	1310002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 1 - Eye Diagram Test - PRBS 7	1210002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - TPS4	1218012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1317012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_DFE) - TPS4	1217012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1315012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	1215012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS 7	1211012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - Arbitrary Pattern	1319012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 1 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - TPS4	1219012	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 2 - Eye Diagram Test (TP2_CTLE) - Arbitrary Pattern	1316013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP2_CTLE) - TPS4	1216013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_CTLE) - Arbitrary Pattern	1316003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_CTLE) - TPS4	1216003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - TPS4	1218003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_DFE) - Arbitrary Pattern	1317003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_DFE) - TPS4	1217003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_EQ) - Arbitrary Pattern	1315003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	1215003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 2 - Eye Diagram Test (TP3_EQ) - PRBS 7	1211003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP_RX_DFE) - Arbitrary Pattern	1319003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test (TP_RX_DFE) - TPS4	1219003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test - Arbitrary Pattern	1310003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test - PRBS 7	1210003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - TPS4	1218013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1317013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_DFE) - TPS4	1217013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1315013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	1215013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS 7	1211013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - Arbitrary Pattern	1319013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 2 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - TPS4	1219013	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP2_CTLE) - Arbitrary Pattern	1316014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP2_CTLE) - TPS4	1216014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_CTLE) - Arbitrary Pattern	1316004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_CTLE) - TPS4	1216004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_DFE) (VESA DFE Tool) - TPS4	1218004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 3 - Eye Diagram Test (TP3_DFE) - Arbitrary Pattern	1317004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_DFE) - TPS4	1217004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_EQ) - Arbitrary Pattern	1315004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_EQ) - HBR2CPAT	1215004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP3_EQ) - PRBS 7	1211004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP_RX_DFE) - Arbitrary Pattern	1319004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test (TP_RX_DFE) - TPS4	1219004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test - Arbitrary Pattern	1310004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test - PRBS 7	1210004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - Arbitrary Pattern	1318014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_DFE) (VESA DFE Tool) - TPS4	1218014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1317014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_DFE) - TPS4	1217014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1315014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT	1215014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS 7	1211014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - Arbitrary Pattern	1319014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.1 Lane 3 - Eye Diagram Test with No Cable Model (TP_RX_DFE) - TPS4	1219014	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
3.10 Lane 0 - AC Common Mode Test (Informative) - Arbitrary Pattern	13110001	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 0 - AC Common Mode Test (Informative) - PRBS 7	12110001	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 0 - AC Common Mode Test (Informative) - TPS4	12110011	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.10 Lane 1 - AC Common Mode Test (Informative) - Arbitrary Pattern	13110002	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 1 - AC Common Mode Test (Informative) - PRBS 7	12110002	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 1 - AC Common Mode Test (Informative) - TPS4	12110012	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 2 - AC Common Mode Test (Informative) - Arbitrary Pattern	13110003	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 2 - AC Common Mode Test (Informative) - PRBS 7	12110003	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 2 - AC Common Mode Test (Informative) - TPS4	12110013	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 3 - AC Common Mode Test (Informative) - Arbitrary Pattern	13110004	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 3 - AC Common Mode Test (Informative) - PRBS 7	12110004	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.10 Lane 3 - AC Common Mode Test (Informative) - TPS4	12110014	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
3.11 Lane 0 - Non ISI Jitter Test (TP2_CTLE) - Arbitrary Pattern	1334011	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test (TP2_CTLE) - TPS4	1234011	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test (TP3_CTLE) - Arbitrary Pattern	1334001	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 0 - Non ISI Jitter Test (TP3_CTLE) - TPS4	1234001	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test (TP3_DFE) - Arbitrary Pattern	1331001	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test (TP3_DFE) - TPS4	1231001	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test - Arbitrary Pattern	1330001	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 0 - Non ISI Jitter Test - HBR2CPAT	1232001	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 0 - Non ISI Jitter Test - PRBS 7	1230001	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 0 - Non ISI Jitter Test - TPS4	1233001	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 0 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1331011	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - TPS4	1231011	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test (TP2_CTLE) - Arbitrary Pattern	1323011	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 0 - Total Jitter Test (TP2_CTLE) - TPS4	1223011	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test (TP3_CTLE) - Arbitrary Pattern	1323001	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test (TP3_CTLE) - TPS4	1223001	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test (TP3_DFE) - Arbitrary Pattern	1324001	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test (TP3_DFE) - TPS4	1224001	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1324011	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 0 - Total Jitter Test with No Cable Model (TP3_DFE) - TPS4	1224011	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test (TP2_CTLE) - Arbitrary Pattern	1334012	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 1 - Non ISI Jitter Test (TP2_CTLE) - TPS4	1234012	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test (TP3_CTLE) - Arbitrary Pattern	1334002	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test (TP3_CTLE) - TPS4	1234002	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test (TP3_DFE) - Arbitrary Pattern	1331002	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test (TP3_DFE) - TPS4	1231002	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Non ISI Jitter Test - Arbitrary Pattern	1330002	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 1 - Non ISI Jitter Test - HBR2CPAT	1232002	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 1 - Non ISI Jitter Test - PRBS 7	1230002	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 1 - Non ISI Jitter Test - TPS4	1233002	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 1 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1331012	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 1 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - TPS4	1231012	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP2_CTLE) - Arbitrary Pattern	1323012	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP2_CTLE) - TPS4	1223012	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP3_CTLE) - Arbitrary Pattern	1323002	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP3_CTLE) - TPS4	1223002	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP3_DFE) - Arbitrary Pattern	1324002	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test (TP3_DFE) - TPS4	1224002	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 1 - Total Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1324012	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 1 - Total Jitter Test with No Cable Model (TP3_DFE) - TPS4	1224012	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP2_CTLE) - Arbitrary Pattern	1334013	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP2_CTLE) - TPS4	1234013	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP3_CTLE) - Arbitrary Pattern	1334003	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP3_CTLE) - TPS4	1234003	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP3_DFE) - Arbitrary Pattern	1331003	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test (TP3_DFE) - TPS4	1231003	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test - Arbitrary Pattern	1330003	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 2 - Non ISI Jitter Test - HBR2CPAT	1232003	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 2 - Non ISI Jitter Test - PRBS 7	1230003	To evaluate the amount of Non ISI Jitter accompanying the data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 2 - Non ISI Jitter Test - TPS4	1233003	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 2 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1331013	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - TPS4	1231013	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP2_CTLE) - Arbitrary Pattern	1323013	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP2_CTLE) - TPS4	1223013	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP3_CTLE) - Arbitrary Pattern	1323003	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP3_CTLE) - TPS4	1223003	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP3_DFE) - Arbitrary Pattern	1324003	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test (TP3_DFE) - TPS4	1224003	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 2 - Total Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1324013	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 2 - Total Jitter Test with No Cable Model (TP3_DFE) - TPS4	1224013	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP2_CTLE) - Arbitrary Pattern	1334014	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP2_CTLE) - TPS4	1234014	To evaluate the Non ISI Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP3_CTLE) - Arbitrary Pattern	1334004	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP3_CTLE) - TPS4	1234004	To evaluate the Non ISI Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP3_DFE) - Arbitrary Pattern	1331004	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test (TP3_DFE) - TPS4	1231004	To evaluate the Non ISI Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test - Arbitrary Pattern	1330004	To evaluate the amount of Non ISI Jitter accompanying the data transmission.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 3 - Non ISI Jitter Test - HBR2CPAT	1232004	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 3 - Non ISI Jitter Test - PRBS 7	1230004	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 3 - Non ISI Jitter Test - TPS4	1233004	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
3.11 Lane 3 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1331014	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Non ISI Jitter Test with No Cable Model (TP3_DFE) - TPS4	1231014	To evaluate the Non ISI Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test (TP2_CTLE) - Arbitrary Pattern	1323014	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test (TP2_CTLE) - TPS4	1223014	To evaluate the Total Jitter (TP2_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test (TP3_CTLE) - Arbitrary Pattern	1323004	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test (TP3_CTLE) - TPS4	1223004	To evaluate the Total Jitter (TP3_CTLE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test (TP3_DFE) - Arbitrary Pattern	1324004	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.11 Lane 3 - Total Jitter Test (TP3_DFE) - TPS4	1224004	To evaluate the Total Jitter (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test with No Cable Model (TP3_DFE) - Arbitrary Pattern	1324014	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.11 Lane 3 - Total Jitter Test with No Cable Model (TP3_DFE) - TPS4	1224014	To evaluate the Total Jitter with No Cable Model (TP3_DFE) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Deterministic Jitter Test (TP3_EQ) - Arbitrary Pattern	1336001	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Deterministic Jitter Test (TP3_EQ) - D10.2	1235001	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	1236001	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1336011	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2	1235011	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 0 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1236011	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Random Jitter Test (TP3_EQ) - Arbitrary Pattern	1338001	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Random Jitter Test (TP3_EQ) - D10.2	1238001	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Random Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1338011	To evaluate the Random Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Random Jitter Test with No Cable Model (TP3_EQ) - D10.2	1238011	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test (TP3_EQ) - Arbitrary Pattern	1322001	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test (TP3_EQ) - D10.2	1221001	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test (TP3_EQ) - HBR2CPAT	1222001	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 0 - Total Jitter Test (TP3_EQ) - PRBS 7	1225001	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test - Arbitrary Pattern	1320001	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test - PRBS 7	1220001	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1322011	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ) - D10.2	1221011	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1222011	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 0 - Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7	1225011	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Deterministic Jitter Test (TP3_EQ) - Arbitrary Pattern	1336002	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 1 - Deterministic Jitter Test (TP3_EQ) - D10.2	1235002	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	1236002	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1336012	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2	1235012	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1236012	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Random Jitter Test (TP3_EQ) - Arbitrary Pattern	1338002	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Random Jitter Test (TP3_EQ) - D10.2	1238002	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Random Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1338012	To evaluate the Random Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 1 - Random Jitter Test with No Cable Model (TP3_EQ) - D10.2	1238012	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test (TP3_EQ) - Arbitrary Pattern	1322002	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test (TP3_EQ) - D10.2	1221002	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test (TP3_EQ) - HBR2CPAT	1222002	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test (TP3_EQ) - PRBS 7	1225002	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test - Arbitrary Pattern	1320002	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test - PRBS 7	1220002	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1322012	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ) - D10.2	1221012	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1222012	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 1 - Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7	1225012	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Deterministic Jitter Test (TP3_EQ) - Arbitrary Pattern	1336003	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Deterministic Jitter Test (TP3_EQ) - D10.2	1235003	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	1236003	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1336013	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2	1235013	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 2 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1236013	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Random Jitter Test (TP3_EQ) - Arbitrary Pattern	1338003	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Random Jitter Test (TP3_EQ) - D10.2	1238003	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Random Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1338013	To evaluate the Random Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Random Jitter Test with No Cable Model (TP3_EQ) - D10.2	1238013	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test (TP3_EQ) - Arbitrary Pattern	1322003	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test (TP3_EQ) - D10.2	1221003	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test (TP3_EQ) - HBR2CPAT	1222003	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 2 - Total Jitter Test (TP3_EQ) - PRBS 7	1225003	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test - Arbitrary Pattern	1320003	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test - PRBS 7	1220003	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1322013	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ) - D10.2	1221013	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1222013	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 2 - Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7	1225013	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Deterministic Jitter Test (TP3_EQ) - Arbitrary Pattern	1336004	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 3 - Deterministic Jitter Test (TP3_EQ) - D10.2	1235004	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Deterministic Jitter Test (TP3_EQ) - HBR2CPAT	1236004	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1336014	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2	1235014	To evaluate the Deterministic Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1236014	To evaluate the Deterministic Jitter No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Random Jitter Test (TP3_EQ) - Arbitrary Pattern	1338004	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Random Jitter Test (TP3_EQ) - D10.2	1238004	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Random Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1338014	To evaluate the Random Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 3 - Random Jitter Test with No Cable Model (TP3_EQ) - D10.2	1238014	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test (TP3_EQ) - Arbitrary Pattern	1322004	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test (TP3_EQ) - D10.2	1221004	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test (TP3_EQ) - HBR2CPAT	1222004	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test (TP3_EQ) - PRBS 7	1225004	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test - Arbitrary Pattern	1320004	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test - PRBS 7	1220004	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) - Arbitrary Pattern	1322014	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) - D10.2	1221014	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT	1222014	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.12 Lane 3 - Total Jitter Test with No Cable Model (TP3_EQ) - PRBS 7	1225014	To evaluate the Total Jitter with No Cable Model (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
3.13 Lane 0 - Unit Interval Test (Informative) - PRBS 7	12160001	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
3.13 Lane 1 - Unit Interval Test (Informative) - PRBS 7	12160002	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
3.13 Lane 2 - Unit Interval Test (Informative) - PRBS 7	12160003	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
3.13 Lane 3 - Unit Interval Test (Informative) - PRBS 7	12160004	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
3.14 Lane 0 - Main Link Frequency Compliance (Maximum) - D10.2	12190001	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
3.14 Lane 0 - Main Link Frequency Compliance (Minimum) - D10.2	12191001	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
3.14 Lane 0 - Main Link Frequency Compliance - Arbitrary Pattern	13193001	
3.14 Lane 0 - Main Link Frequency Compliance - D10.2	12193001	
3.14 Lane 1 - Main Link Frequency Compliance (Maximum) - D10.2	12190002	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
3.14 Lane 1 - Main Link Frequency Compliance (Minimum) - D10.2	12191002	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.14 Lane 1 - Main Link Frequency Compliance - Arbitrary Pattern	13193002	
3.14 Lane 1 - Main Link Frequency Compliance - D10.2	12193002	
3.14 Lane 2 - Main Link Frequency Compliance (Maximum) - D10.2	12190003	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
3.14 Lane 2 - Main Link Frequency Compliance (Minimum) - D10.2	12191003	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
3.14 Lane 2 - Main Link Frequency Compliance - Arbitrary Pattern	13193003	
3.14 Lane 2 - Main Link Frequency Compliance - D10.2	12193003	
3.14 Lane 3 - Main Link Frequency Compliance (Maximum) - D10.2	12190004	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
3.14 Lane 3 - Main Link Frequency Compliance (Minimum) - D10.2	12191004	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
3.14 Lane 3 - Main Link Frequency Compliance - Arbitrary Pattern	13193004	
3.14 Lane 3 - Main Link Frequency Compliance - D10.2	12193004	
3.15 Lane 0 - SSC Modulation Frequency Test - Arbitrary Pattern	13170001	
3.15 Lane 0 - SSC Modulation Frequency Test - D10.2	12170001	
3.15 Lane 1 - SSC Modulation Frequency Test - Arbitrary Pattern	13170002	
3.15 Lane 1 - SSC Modulation Frequency Test - D10.2	12170002	
3.15 Lane 2 - SSC Modulation Frequency Test - Arbitrary Pattern	13170003	
3.15 Lane 2 - SSC Modulation Frequency Test - D10.2	12170003	
3.15 Lane 3 - SSC Modulation Frequency Test - Arbitrary Pattern	13170004	
3.15 Lane 3 - SSC Modulation Frequency Test - D10.2	12170004	
3.16 Lane 0 - SSC Modulation Deviation Test - Arbitrary Pattern	13180001	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.16 Lane 0 - SSC Modulation Deviation Test - D10.2	12180001	
3.16 Lane 1 - SSC Modulation Deviation Test - Arbitrary Pattern	13180002	
3.16 Lane 1 - SSC Modulation Deviation Test - D10.2	12180002	
3.16 Lane 2 - SSC Modulation Deviation Test - Arbitrary Pattern	13180003	
3.16 Lane 2 - SSC Modulation Deviation Test - D10.2	12180003	
3.16 Lane 3 - SSC Modulation Deviation Test - Arbitrary Pattern	13180004	
3.16 Lane 3 - SSC Modulation Deviation Test - D10.2	12180004	
3.17 Lane 0 - SSC Deviation HF Variation Test (Informative) - Arbitrary Pattern	13200001	
3.17 Lane 0 - SSC Deviation HF Variation Test (Informative) - D10.2	12200001	
3.17 Lane 1 - SSC Deviation HF Variation Test (Informative) - Arbitrary Pattern	13200002	
3.17 Lane 1 - SSC Deviation HF Variation Test (Informative) - D10.2	12200002	
3.17 Lane 2 - SSC Deviation HF Variation Test (Informative) - Arbitrary Pattern	13200003	
3.17 Lane 2 - SSC Deviation HF Variation Test (Informative) - D10.2	12200003	
3.17 Lane 3 - SSC Deviation HF Variation Test (Informative) - Arbitrary Pattern	13200004	
3.17 Lane 3 - SSC Deviation HF Variation Test (Informative) - D10.2	12200004	
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 1/Swing 0) - PRBS 7	1261001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - Arbitrary Pattern	1364101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	1264101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PRBS 7	1264001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - Arbitrary Pattern	1362101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	1262101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PRBS 7	1262001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - Arbitrary Pattern	1363101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PLTPAT	1263101	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PRBS 7	1263001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 0 - Non Pre-Emphasis Level Test - PRBS 7	1260001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 1/Swing 0) - PRBS 7	1261002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - Arbitrary Pattern	1364102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	1264102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PRBS 7	1264002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - Arbitrary Pattern	1362102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	1262102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PRBS 7	1262002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - Arbitrary Pattern	1363102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PLTPAT	1263102	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PRBS 7	1263002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 1 - Non Pre-Emphasis Level Test - PRBS 7	1260002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 1/Swing 0) - PRBS 7	1261003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - Arbitrary Pattern	1364103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	1264103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PRBS 7	1264003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - Arbitrary Pattern	1362103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	1262103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PRBS 7	1262003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - Arbitrary Pattern	1363103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PLTPAT	1263103	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PRBS 7	1263003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 2 - Non Pre-Emphasis Level Test - PRBS 7	1260003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 1/Swing 0) - PRBS 7	1261004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - Arbitrary Pattern	1364104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PLTPAT	1264104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 0) - PRBS 7	1264004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - Arbitrary Pattern	1362104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PLTPAT	1262104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 2/Swing 1) - PRBS 7	1262004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - Arbitrary Pattern	1363104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PLTPAT	1263104	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test (Swing 3/Swing 2) - PRBS 7	1263004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.2 Lane 3 - Non Pre-Emphasis Level Test - PRBS 7	1260004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 0) - Arbitrary Pattern	1372101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 0) - PLTPAT	1272101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 0) - PRBS 7	1272001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 1) - Arbitrary Pattern	1373101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1273101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 1) - PRBS 7	1273001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 2) - Arbitrary Pattern	1374101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1274101	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Non-Transition Voltage Range Measurement (Swing 2) - PRBS 7	1274001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Peak to Peak Voltage Test - Arbitrary Pattern	1366101	To evaluate the peak to peak voltage of the differential output signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 0 - Peak to Peak Voltage Test - PLTPAT	1266101	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 0 - Peak to Peak Voltage Test - PRBS 7	1266001	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT	1279001	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 2/Level 1) - PCTPAT	1279101	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 0 - Post-Cursor2 Verification Test (Level 3/Level 2) - PCTPAT	1279201	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 0 - Pre-Emphasis Level Test - Arbitrary Pattern	1370501	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Pre-Emphasis Level Test - D10.2	1271001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Pre-Emphasis Level Test - PLTPAT	1270501	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - Pre-Emphasis Level Test - PRBS 7	1270001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 0 - VTX_MEQ_DELTA - PLTPAT	1295101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_MEQ_LEVEL0_DELTA - PLTPAT	1291101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT	1281101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT	1282101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 0 - VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT	1283101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT	1285101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT	1286101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT	1287101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_PE_RATIO - PLTPAT	1298101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 0 - VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT	1299101	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 0) - Arbitrary Pattern	1372102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 0) - PLTPAT	1272102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 0) - PRBS 7	1272002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 1) - Arbitrary Pattern	1373102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1273102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 1) - PRBS 7	1273002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 2) - Arbitrary Pattern	1374102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1274102	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Non-Transition Voltage Range Measurement (Swing 2) - PRBS 7	1274002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Peak to Peak Voltage Test - Arbitrary Pattern	1366102	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 1 - Peak to Peak Voltage Test - PLTPAT	1266102	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 1 - Peak to Peak Voltage Test - PRBS 7	1266002	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 1 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT	1279002	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 1 - Post-Cursor2 Verification Test (Level 2/Level 1) - PCTPAT	1279102	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 1 - Post-Cursor2 Verification Test (Level 3/Level 2) - PCTPAT	1279202	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 1 - Pre-Emphasis Level Test - Arbitrary Pattern	1370502	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Pre-Emphasis Level Test - D10.2	1271002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Pre-Emphasis Level Test - PLTPAT	1270502	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - Pre-Emphasis Level Test - PRBS 7	1270002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 1 - VTX_MEQ_DELTA - PLTPAT	1295102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 1 - VTX_MEQ_LEVEL0_DELTA - PLTPAT	1291102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT	1281102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT	1282102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT	1283102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT	1285102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT	1286102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT	1287102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_PE_RATIO - PLTPAT	1298102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 1 - VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT	1299102	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 0) - Arbitrary Pattern	1372103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 0) - PLTPAT	1272103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 0) - PRBS 7	1272003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 1) - Arbitrary Pattern	1373103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1273103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 1) - PRBS 7	1273003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 2) - Arbitrary Pattern	1374103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1274103	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Non-Transition Voltage Range Measurement (Swing 2) - PRBS 7	1274003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Peak to Peak Voltage Test - Arbitrary Pattern	1366103	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 2 - Peak to Peak Voltage Test - PLTPAT	1266103	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 2 - Peak to Peak Voltage Test - PRBS 7	1266003	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 2 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT	1279003	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 2 - Post-Cursor2 Verification Test (Level 2/Level 1) - PCTPAT	1279103	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 2 - Post-Cursor2 Verification Test (Level 3/Level 2) - PCTPAT	1279203	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 2 - Pre-Emphasis Level Test - Arbitrary Pattern	1370503	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 2 - Pre-Emphasis Level Test - D10.2	1271003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Pre-Emphasis Level Test - PLTPAT	1270503	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - Pre-Emphasis Level Test - PRBS 7	1270003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 2 - VTX_MEQ_DELTA - PLTPAT	1295103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_MEQ_LEVEL0_DELTA - PLTPAT	1291103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT	1281103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT	1282103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT	1283103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT	1285103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT	1286103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT	1287103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 2 - VTX_PE_RATIO - PLTPAT	1298103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 2 - VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT	1299103	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 0) - Arbitrary Pattern	1372104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 0) - PLTPAT	1272104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 0) - PRBS 7	1272004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) - Arbitrary Pattern	1373104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) - PLTPAT	1273104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 1) - PRBS 7	1273004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) - Arbitrary Pattern	1374104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) - PLTPAT	1274104	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Non-Transition Voltage Range Measurement (Swing 2) - PRBS 7	1274004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Peak to Peak Voltage Test - Arbitrary Pattern	1366104	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 3 - Peak to Peak Voltage Test - PLTPAT	1266104	To evaluate the peak to peak voltage of the differential output signal.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 3 - Peak to Peak Voltage Test - PRBS 7	1266004	To evaluate the peak to peak voltage of the differential output signal.
3.3 Lane 3 - Post-Cursor2 Verification Test (Level 1/Level 0) - PCTPAT	1279004	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 3 - Post-Cursor2 Verification Test (Level 2/Level 1) - PCTPAT	1279104	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 3 - Post-Cursor2 Verification Test (Level 3/Level 2) - PCTPAT	1279204	This test evaluates the effect of adding Post-Cursor2 in a Source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor2 setting.
3.3 Lane 3 - Pre-Emphasis Level Test - Arbitrary Pattern	1370504	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Pre-Emphasis Level Test - D10.2	1271004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Pre-Emphasis Level Test - PLTPAT	1270504	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - Pre-Emphasis Level Test - PRBS 7	1270004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
3.3 Lane 3 - VTX_MEQ_DELTA - PLTPAT	1295104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_MEQ_LEVEL0_DELTA - PLTPAT	1291104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_OUTPUT_LEVEL0_RATIO (VSL 1/VSL 0) - PLTPAT	1281104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_OUTPUT_LEVEL0_RATIO (VSL 2/VSL 0) - PLTPAT	1282104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.3 Lane 3 - VTX_OUTPUT_LEVEL0_RATIO (VSL 3/VSL 0) - PLTPAT	1283104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_OUTPUT_RATIO (VSL 1/VSL 0) - PLTPAT	1285104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_OUTPUT_RATIO (VSL 2/VSL 1) - PLTPAT	1286104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_OUTPUT_RATIO (VSL 3/VSL 2) - PLTPAT	1287104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_PE_RATIO - PLTPAT	1298104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.3 Lane 3 - VTX_TRANSITION_BIT_OUTPUT_RATIO - PLTPAT	1299104	To ensures that the system budget is obeyed and ensures that level and pre-emphasis settings are monotonic so that a Sink can rely on the Source to incrementally increase upon request by sink.
3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - Arbitrary Pattern	1390001	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 0/ Lane 1 - Inter Pair Skew Test - PRBS 7	1290001	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 0/ Lane 2 - Inter Pair Skew Test - Arbitrary Pattern	1390002	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 0/ Lane 2 - Inter Pair Skew Test - PRBS 7	1290002	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 0/ Lane 3 - Inter Pair Skew Test - Arbitrary Pattern	1390003	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 0/ Lane 3 - Inter Pair Skew Test - PRBS 7	1290003	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 1/ Lane 2 - Inter Pair Skew Test - Arbitrary Pattern	1390004	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 1/ Lane 2 - Inter Pair Skew Test - PRBS 7	1290004	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.4 Lane 1/ Lane 3 - Inter Pair Skew Test - Arbitrary Pattern	1390005	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 1/ Lane 3 - Inter Pair Skew Test - PRBS 7	1290005	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 2/ Lane 3 - Inter Pair Skew Test - Arbitrary Pattern	1390006	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.4 Lane 2/ Lane 3 - Inter Pair Skew Test - PRBS 7	1290006	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
3.5 Lane 0 - Intra Pair Skew Test (Informative) - Arbitrary Pattern	13100001	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 0 - Intra Pair Skew Test (Informative) - D10.2	12100001	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 1 - Intra Pair Skew Test (Informative) - Arbitrary Pattern	13100002	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 1 - Intra Pair Skew Test (Informative) - D10.2	12100002	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 2 - Intra Pair Skew Test (Informative) - Arbitrary Pattern	13100003	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 2 - Intra Pair Skew Test (Informative) - D10.2	12100003	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 3 - Intra Pair Skew Test (Informative) - Arbitrary Pattern	13100004	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.5 Lane 3 - Intra Pair Skew Test (Informative) - D10.2	12100004	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
3.6 Lane 0 - Fall Time Test (Informative) - PRBS 7	1250001	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
3.6 Lane 0 - Rise Time Test (Informative) - PRBS 7	1240001	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
3.6 Lane 1 - Fall Time Test (Informative) - PRBS 7	1250002	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
3.6 Lane 1 - Rise Time Test (Informative) - PRBS 7	1240002	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
3.6 Lane 2 - Fall Time Test (Informative) - PRBS 7	1250003	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
3.6 Lane 2 - Rise Time Test (Informative) - PRBS 7	1240003	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
3.6 Lane 3 - Fall Time Test (Informative) - PRBS 7	1250004	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.6 Lane 3 - Rise Time Test (Informative) - PRBS 7	1240004	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
3.7 Lane 0 - Falling Mismatch Test (Informative) - PRBS 7	12130001	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 0 - Rising Mismatch Test (Informative) - PRBS 7	12120001	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 1 - Falling Mismatch Test (Informative) - PRBS 7	12130002	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 1 - Rising Mismatch Test (Informative) - PRBS 7	12120002	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 2 - Falling Mismatch Test (Informative) - PRBS 7	12130003	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 2 - Rising Mismatch Test (Informative) - PRBS 7	12120003	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 3 - Falling Mismatch Test (Informative) - PRBS 7	12130004	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.7 Lane 3 - Rising Mismatch Test (Informative) - PRBS 7	12120004	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
3.8 Lane 0 - Overshoot Test (Informative) - PRBS 7	1265001	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
3.8 Lane 1 - Overshoot Test (Informative) - PRBS 7	1265002	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
3.8 Lane 2 - Overshoot Test (Informative) - PRBS 7	1265003	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
3.8 Lane 3 - Overshoot Test (Informative) - PRBS 7	1265004	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
3.9 Lane 0 - Frequency Accuracy Test - D10.2	1280001	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
3.9 Lane 1 - Frequency Accuracy Test - D10.2	1280002	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
3.9 Lane 2 - Frequency Accuracy Test - D10.2	1280003	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
3.9 Lane 3 - Frequency Accuracy Test - D10.2	1280004	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
8.1 Aux Channel Eye Test (Sink)	125011	To evaluate the AUX Channel waveform for sink device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 Aux Channel Eye Test (Sink)	5011	To evaluate the AUX Channel waveform for sink device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 Aux Channel Eye Test (Source)	125001	To evaluate the AUX Channel waveform for source device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 Aux Channel Eye Test (Source)	5001	To evaluate the AUX Channel waveform for source device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 Aux Channel Peak to Peak Voltage Test (Sink)	125012	To evaluate the peak to peak voltage AUX Channel waveform for sink.
8.1 Aux Channel Peak to Peak Voltage Test (Sink)	5012	To evaluate the peak to peak voltage AUX Channel waveform for sink.
8.1 Aux Channel Peak to Peak Voltage Test (Source)	125002	To evaluate the peak to peak voltage AUX Channel waveform for source.
8.1 Aux Channel Peak to Peak Voltage Test (Source)	5002	To evaluate the peak to peak voltage AUX Channel waveform for source.
8.1 eDP Aux Channel Eye Test (Sink)	5111	To evaluate the AUX Channel waveform for sink device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 eDP Aux Channel Eye Test (Source)	5101	To evaluate the AUX Channel waveform for source device ensuring that timing variables and amplitude trajectories support DisplayPort system objectives of Bit Error Rate in data transmission.
8.1 eDP Aux Channel Peak to Peak Voltage Test (Sink)	5112	To evaluate the peak to peak voltage AUX Channel waveform for sink.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
8.1 eDP Aux Channel Peak to Peak Voltage Test (Source)	5102	To evaluate the peak to peak voltage AUX Channel waveform for source.
8.2 Aux Channel Eye Sensitivity Test (Sink)	125051	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.2 Aux Channel Eye Sensitivity Test (Sink)	5051	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.2 Aux Channel Eye Sensitivity Test (Source)	125041	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.2 Aux Channel Eye Sensitivity Test (Source)	5041	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.2 eDP Aux Channel Eye Sensitivity Test (Sink)	5151	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.2 eDP Aux Channel Eye Sensitivity Test (Source)	5141	To evaluate the sensitivity to the AUX Channel eye opening of a Device Under Test.
8.3a Inrush Energy Power Test	7000	To evaluate the Inrush Energy at the power supply input of a Power consuming Device Under Test or to evaluate the inrush tolerance at the power supply output of a power providing Device Under Test.
8.3b Inrush Peak Current Test	7001	To evaluate the Inrush Energy at the power supply input of a Power consuming Device Under Test or to evaluate the inrush tolerance at the power supply output of a power providing Device Under Test.
8.5a Inrush Energy Power Test	127000	To evaluate the Inrush Energy at the power supply input of a Power consuming Device Under Test or to evaluate the inrush tolerance at the power supply output of a power providing Device Under Test.
8.5b Inrush Peak Current Test	127001	To evaluate the Inrush Energy at the power supply input of a Power consuming Device Under Test or to evaluate the inrush tolerance at the power supply output of a power providing Device Under Test.
9.2 Aux Channel Slew Rate Test (Sink)	125013	To evaluate the peak to peak voltage AUX Channel waveform for sink.
9.2 Aux Channel Slew Rate Test (Source)	125003	To evaluate the AUX signaling edge rates for source to minimize crosstalk to Main-Link signals.
Aux Channel Eye Sensitivity Calibration (Reference Sink)	125021	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Sink AUX eye opening has meet the minimum level for futher AUX sensitivity testing.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Aux Channel Eye Sensitivity Calibration (Reference Sink)	5021	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Sink AUX eye opening has meet the minimum level for futher AUX sensitivity testing.
Aux Channel Eye Sensitivity Calibration (Reference Source)	125031	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Source AUX eye opening has meet the minimum level for futher AUX sensitivity testing.
Aux Channel Eye Sensitivity Calibration (Reference Source)	5031	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Source AUX eye opening has meet the minimum level for futher AUX sensitivity testing.
Aux Channel Unit Interval Test (Sink)	125010	To evaluate the unit interval of AUX channel.
Aux Channel Unit Interval Test (Sink)	5010	To evaluate the unit interval of AUX channel.
Aux Channel Unit Interval Test (Source)	125000	To evaluate the unit interval of AUX channel.
Aux Channel Unit Interval Test (Source)	5000	To evaluate the unit interval of AUX channel.
Clock Recovery Settings	1200	
Clock Recovery Settings - DisplayPort 1.1, DisplayPort 1.1a	1	
Configurable Parameter Settings	1201	
Configurable Parameter Settings - DisplayPort 1.1, DisplayPort 1.1a	0	
D0 - Dual Mode Data Jitter	611	To evaluate data jitter of a source operating in dual-mode.
D0 - Dual Mode Data Jitter	911	To evaluate data jitter of a source operating in dual-mode.
D0 - Dual Mode Data Peak-Peak Differential Voltage (Max)	821	To evaluate data maximum peak to peak voltage of a source operating in dual-mode.
D0 - Dual Mode Data Peak-Peak Differential Voltage (Min)	811	To evaluate data minimum peak to peak voltage of a source operating in dual-mode.
D0 - Dual Mode Eye Diagram Testing	601	To evaluate the waveform ensuring that timing variables and amplitude trajectories meet the requirements for a dual-mode source device.
D0 - Dual Mode Intra Pair Skew Test	701	To evaluate the skew, or time delay, between respective sides of a differential data of a source operating in dual-mode.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
D0/D1 - Dual Mode Inter Pair Skew Test	711	To evaluate the skew, or time delay, between respective differential data of a source operating in dual-mode.
D0/D2 - Dual Mode Inter Pair Skew Test	712	To evaluate the skew, or time delay, between respective differential data of a source operating in dual-mode.
D1 - Dual Mode Data Jitter	612	To evaluate data jitter of a source operating in dual-mode.
D1 - Dual Mode Data Jitter	912	To evaluate data jitter of a source operating in dual-mode.
D1 - Dual Mode Data Peak-Peak Differential Voltage (Max)	822	To evaluate data maximum peak to peak voltage of a source operating in dual-mode.
D1 - Dual Mode Data Peak-Peak Differential Voltage (Min)	812	To evaluate data minimum peak to peak voltage of a source operating in dual-mode.
D1 - Dual Mode Eye Diagram Testing	602	To evaluate the waveform ensuring that timing variables and amplitude trajectories meet the requirements for a dual-mode source device.
D1 - Dual Mode Intra Pair Skew Test	702	To evaluate the skew, or time delay, between respective sides of a differential data of a source operating in dual-mode.
D1/D2 - Dual Mode Inter Pair Skew Test	713	To evaluate the skew, or time delay, between respective differential data of a source operating in dual-mode.
D2 - Dual Mode Data Jitter	613	To evaluate data jitter of a source operating in dual-mode.
D2 - Dual Mode Data Jitter	913	To evaluate data jitter of a source operating in dual-mode.
D2 - Dual Mode Data Peak-Peak Differential Voltage (Max)	823	To evaluate data maximum peak to peak voltage of a source operating in dual-mode.
D2 - Dual Mode Data Peak-Peak Differential Voltage (Min)	813	To evaluate data minimum peak to peak voltage of a source operating in dual-mode.
D2 - Dual Mode Eye Diagram Testing	603	To evaluate the waveform ensuring that timing variables and amplitude trajectories meet the requirements for a dual-mode source device.
D2 - Dual Mode Intra Pair Skew Test	703	To evaluate the skew, or time delay, between respective sides of a differential data of a source operating in dual-mode.
Dual Mode TMDS Clock Duty Cycle (Max)	502	To evaluate the maximum duty cycle of the TMDS clock signal of a source operating in dual-mode.
Dual Mode TMDS Clock Duty Cycle (Min)	501	To evaluate the minimum duty cycle of the TMDS clock signal of a source operating in dual-mode.
Dual Mode TMDS Clock Jitter	503	To evaluate the jitter of the TMDS clock signal of a source operating in dual-mode.
Dual Mode TMDS Clock Jitter	803	To evaluate the jitter of the TMDS clock signal of a source operating in dual-mode.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Equalizer Settings	1208	
Equalizer Settings - CTLE Optimization	11208	
Equalizer Settings - DisplayPort 1.4	1408	
Equalizer Settings - eDP	108	
Eye Diagram Settings	1205	
Eye Diagram Settings - CTLE Optimization	11205	
Eye Diagram Settings - eDP	105	
Jitter Separation Settings	1202	
Jitter Separation Settings - DisplayPort 1.1, DisplayPort 1.1a	2	
Lane 0 - AC Common Mode Test	110001	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13910021	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - TPS4	12910021	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13910031	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - TPS4	12910031	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13910041	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - TPS4	12910041	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13910051	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - TPS4	12910051	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13910061	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - TPS4	12910061	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13910071	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - TPS4	12910071	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13910081	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - TPS4	12910081	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13910091	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - TPS4	12910091	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13910101	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - TPS4	12910101	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13910011	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - TPS4	12910011	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13920021	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - TPS4	12920021	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13920031	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - TPS4	12920031	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13920041	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - TPS4	12920041	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13920051	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - TPS4	12920051	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13920061	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - TPS4	12920061	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13920071	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - TPS4	12920071	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13920081	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - TPS4	12920081	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13920091	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - TPS4	12920091	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13920101	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - TPS4	12920101	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13920011	To find the optimized DC gain value for the CTLE.
Lane 0 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - TPS4	12920011	To find the optimized DC gain value for the CTLE.
Lane 0 - Cable Eye Diagram Test	12150001	
Lane 0 - Cable Eye Diagram Test	150001	
Lane 0 - Cable Non ISI Jitter Test	12240001	
Lane 0 - Cable Non ISI Jitter Test	240001	
Lane 0 - Cable Total Jitter Test	12230001	
Lane 0 - Cable Total Jitter Test	230001	
Lane 0 - D10.2 eDP Deterministic Jitter (TP3_EQ)	35101	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - D10.2 eDP Random Jitter (TP3_EQ)	38101	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - D10.2 eDP Total Jitter Test (TP3_EQ)	21101	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Eye Diagram Test	10001	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - Fall Time Test (Informative)	50001	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
Lane 0 - Falling MisMatch Test (Informative)	130001	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 0 - Frequency Accuracy Test	80001	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
Lane 0 - HBR2CPAT eDP Deterministic Jitter Test (TP3_EQ)	36101	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - HBR2CPAT eDP Total Jitter Test (TP3_EQ)	20101	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Intra Pair Skew Test	100001	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 0 - Link Layer Phy Change Test - Bit Rate	12320001	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Lane 0 - Link Layer Phy Change Test - Level	12310001	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Lane 0 - Link Layer Phy Change Test - Pre-Emphasis	12300001	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - Arbitrary Pattern	1339001	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - D10.2	1239001	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - Main Link Frequency Compliance	193001	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 0 - Main Link Frequency Compliance (SSC Frequency Max)	190001	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
Lane 0 - Main Link Frequency Compliance (SSC Frequency Min)	191001	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
Lane 0 - Non ISI Jitter Test	30001	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
Lane 0 - Non Pre-Emphasis Level Test	60001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 0 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	61001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 0 - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	64001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 0 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	62001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 0 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	63001	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 0 - Non-Transition Voltage Range Measurement (Swing 0)	72001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 0 - Non-Transition Voltage Range Measurement (Swing 1)	73001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 0 - Non-Transition Voltage Range Measurement (Swing 2)	74001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 0 - Overshoot Test	65001	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
Lane 0 - Pre-Emphasis Level Test	70001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - Pre-Emphasis Level Test [D10.2]	71001	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 0 - Rise Time Test (Informative)	40001	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
Lane 0 - Rising MisMatch Test (Informative)	120001	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 0 - SSC Deviation HF Variation Test (Informative)	200001	Verify SSC profile does not include any frequency excursions which would exceed 1250ppm/uSec
Lane 0 - SSC Modulation Deviation Test	180001	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 0 - SSC Modulation Frequency Test	170001	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - SSC Unit Interval Test	160001	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
Lane 0 - Sink Eye Diagram Test	12140001	
Lane 0 - Sink Eye Diagram Test	140001	
Lane 0 - Sink Non ISI Jitter Test	12220001	
Lane 0 - Sink Non ISI Jitter Test	220001	
Lane 0 - Sink Total Jitter Test	12210001	
Lane 0 - Sink Total Jitter Test	210001	
Lane 0 - Total Jitter Test	20001	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0 - eDP Eye Diagram Test	15101	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - eDP Eye Diagram Test (TP3_EQ)	10101	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 0 - eDP Intra Pair Skew Test	100101	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 0 - eDP Main Link Frequency Compliance	193101	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 0 - eDP Non ISI Jitter Test	30101	To evaluate the amount of eDP Non ISI Jitter accompanying the data transmission.
Lane 0 - eDP SSC Modulation Deviation Test	180101	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 0 - eDP SSC Modulation Frequency Test	170101	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 0 - eDP Total Jitter Test	20111	To evaluate the eDP Total Jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 0/ Lane 1 - Inter Pair Skew Test	90001	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 0/ Lane 1 - eDP Inter Pair Skew Test	90101	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 0/ Lane 2 - Inter Pair Skew Test	90002	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 0/ Lane 2 - eDP Inter Pair Skew Test	90102	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 0/ Lane 3 - Inter Pair Skew Test	90003	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 0/ Lane 3 - eDP Inter Pair Skew Test	90103	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 1 - AC Common Mode Test	110002	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13910022	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - TPS4	12910022	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13910032	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - TPS4	12910032	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13910042	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - TPS4	12910042	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13910052	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - TPS4	12910052	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13910062	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - TPS4	12910062	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13910072	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - TPS4	12910072	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13910082	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - TPS4	12910082	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13910092	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - TPS4	12910092	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13910102	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - TPS4	12910102	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13910012	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - TPS4	12910012	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13920022	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - TPS4	12920022	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13920032	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - TPS4	12920032	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13920042	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - TPS4	12920042	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13920052	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - TPS4	12920052	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13920062	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - TPS4	12920062	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13920072	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - TPS4	12920072	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13920082	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - TPS4	12920082	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13920092	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - TPS4	12920092	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13920102	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - TPS4	12920102	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13920012	To find the optimized DC gain value for the CTLE.
Lane 1 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - TPS4	12920012	To find the optimized DC gain value for the CTLE.
Lane 1 - Cable Eye Diagram Test	12150002	
Lane 1 - Cable Eye Diagram Test	150002	
Lane 1 - Cable Non ISI Jitter Test	12240002	
Lane 1 - Cable Non ISI Jitter Test	240002	
Lane 1 - Cable Total Jitter Test	12230002	
Lane 1 - Cable Total Jitter Test	230002	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - D10.2 eDP Deterministic Jitter (TP3_EQ)	35102	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - D10.2 eDP Random Jitter (TP3_EQ)	38102	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - D10.2 eDP Total Jitter Test (TP3_EQ)	21102	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Eye Diagram Test	10002	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - Fall Time Test (Informative)	50002	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
Lane 1 - Falling MisMatch Test (Informative)	130002	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 1 - Frequency Accuracy Test	80002	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
Lane 1 - HBR2CPAT eDP Deterministic Jitter Test (TP3_EQ)	36102	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - HBR2CPAT eDP Total Jitter Test (TP3_EQ)	20102	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Intra Pair Skew Test	100002	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 1 - Link Layer Phy Change Test - Bit Rate	12320002	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Link Layer Phy Change Test - Level	12310002	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Lane 1 - Link Layer Phy Change Test - Pre-Emphasis	12300002	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Lane 1 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - Arbitrary Pattern	1339002	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - D10.2	1239002	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1 - Main Link Frequency Compliance	193002	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 1 - Main Link Frequency Compliance (SSC Frequency Max)	190002	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
Lane 1 - Main Link Frequency Compliance (SSC Frequency Min)	191002	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
Lane 1 - Non ISI Jitter Test	30002	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
Lane 1 - Non Pre-Emphasis Level Test	60002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 1 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	61002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 1 - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	64002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 1 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	62002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 1 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	63002	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 1 - Non-Transition Voltage Range Measurement (Swing 0)	72002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 1 - Non-Transition Voltage Range Measurement (Swing 1)	73002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - Non-Transition Voltage Range Measurement (Swing 2)	74002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 1 - Overshoot Test	65002	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
Lane 1 - Pre-Emphasis Level Test	70002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 1 - Pre-Emphasis Level Test [D10.2]	71002	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 1 - Rise Time Test (Informative)	40002	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
Lane 1 - Rising MisMatch Test (Informative)	120002	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 1 - SSC Deviation HF Variation Test (Informative)	200002	Verify SSC profile does not include any frequency excursions which would exceed 1250ppm/uSec
Lane 1 - SSC Modulation Deviation Test	180002	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 1 - SSC Modulation Frequency Test	170002	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - SSC Unit Interval Test	160002	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
Lane 1 - Sink Eye Diagram Test	12140002	
Lane 1 - Sink Eye Diagram Test	140002	
Lane 1 - Sink Non ISI Jitter Test	12220002	
Lane 1 - Sink Non ISI Jitter Test	220002	
Lane 1 - Sink Total Jitter Test	12210002	
Lane 1 - Sink Total Jitter Test	210002	
Lane 1 - Total Jitter Test	20002	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 1 - eDP Eye Diagram Test	15102	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - eDP Eye Diagram Test (TP3_EQ)	10102	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 1 - eDP Intra Pair Skew Test	100102	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 1 - eDP Main Link Frequency Compliance	193102	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 1 - eDP Non ISI Jitter Test	30102	To evaluate the amount of eDP Non ISI Jitter accompanying the data transmission.
Lane 1 - eDP SSC Modulation Deviation Test	180102	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 1 - eDP SSC Modulation Frequency Test	170102	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 1 - eDP Total Jitter Test	20112	To evaluate the eDP Total Jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 1/ Lane 2 - Inter Pair Skew Test	90004	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 1/ Lane 2 - eDP Inter Pair Skew Test	90104	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 1/ Lane 3 - Inter Pair Skew Test	90005	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 1/ Lane 3 - eDP Inter Pair Skew Test	90105	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 2 - AC Common Mode Test	110003	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13910023	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - TPS4	12910023	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13910033	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - TPS4	12910033	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13910043	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - TPS4	12910043	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13910053	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - TPS4	12910053	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13910063	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - TPS4	12910063	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13910073	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - TPS4	12910073	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13910083	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - TPS4	12910083	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13910093	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - TPS4	12910093	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13910103	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - TPS4	12910103	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13910013	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - TPS4	12910013	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13920023	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - TPS4	12920023	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13920033	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - TPS4	12920033	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13920043	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - TPS4	12920043	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13920053	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - TPS4	12920053	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13920063	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - TPS4	12920063	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13920073	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - TPS4	12920073	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13920083	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - TPS4	12920083	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13920093	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - TPS4	12920093	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13920103	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - TPS4	12920103	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13920013	To find the optimized DC gain value for the CTLE.
Lane 2 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - TPS4	12920013	To find the optimized DC gain value for the CTLE.
Lane 2 - Cable Eye Diagram Test	12150003	
Lane 2 - Cable Eye Diagram Test	150003	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Cable Non ISI Jitter Test	12240003	
Lane 2 - Cable Non ISI Jitter Test	240003	
Lane 2 - Cable Total Jitter Test	12230003	
Lane 2 - Cable Total Jitter Test	230003	
Lane 2 - D10.2 eDP Deterministic Jitter (TP3_EQ)	35103	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - D10.2 eDP Random Jitter (TP3_EQ)	38103	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - D10.2 eDP Total Jitter Test (TP3_EQ)	21103	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Eye Diagram Test	10003	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - Fall Time Test (Informative)	50003	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
Lane 2 - Falling MisMatch Test (Informative)	130003	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 2 - Frequency Accuracy Test	80003	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
Lane 2 - HBR2CPAT eDP Deterministic Jitter Test (TP3_EQ)	36103	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - HBR2CPAT eDP Total Jitter Test (TP3_EQ)	20103	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Intra Pair Skew Test	100003	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 2 - Link Layer Phy Change Test - Bit Rate	12320003	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Lane 2 - Link Layer Phy Change Test - Level	12310003	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Lane 2 - Link Layer Phy Change Test - Pre-Emphasis	12300003	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Lane 2 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - Arbitrary Pattern	1339003	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - D10.2	1239003	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - Main Link Frequency Compliance	193003	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 2 - Main Link Frequency Compliance (SSC Frequency Max)	190003	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
Lane 2 - Main Link Frequency Compliance (SSC Frequency Min)	191003	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
Lane 2 - Non ISI Jitter Test	30003	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
Lane 2 - Non Pre-Emphasis Level Test	60003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 2 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	61003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 2 - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	64003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 2 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	62003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 2 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	63003	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Non-Transition Voltage Range Measurement (Swing 0)	72003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 2 - Non-Transition Voltage Range Measurement (Swing 1)	73003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 2 - Non-Transition Voltage Range Measurement (Swing 2)	74003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 2 - Overshoot Test	65003	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
Lane 2 - Pre-Emphasis Level Test	70003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 2 - Pre-Emphasis Level Test [D10.2]	71003	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 2 - Rise Time Test (Informative)	40003	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
Lane 2 - Rising MisMatch Test (Informative)	120003	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 2 - SSC Deviation HF Variation Test (Informative)	200003	Verify SSC profile does not include any frequency excursions which would exceed 1250ppm/uSec
Lane 2 - SSC Modulation Deviation Test	180003	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 2 - SSC Modulation Frequency Test	170003	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - SSC Unit Interval Test	160003	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
Lane 2 - Sink Eye Diagram Test	12140003	
Lane 2 - Sink Eye Diagram Test	140003	
Lane 2 - Sink Non ISI Jitter Test	12220003	
Lane 2 - Sink Non ISI Jitter Test	220003	
Lane 2 - Sink Total Jitter Test	12210003	
Lane 2 - Sink Total Jitter Test	210003	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 2 - Total Jitter Test	20003	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2 - eDP Eye Diagram Test	15103	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - eDP Eye Diagram Test (TP3_EQ)	10103	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 2 - eDP Intra Pair Skew Test	100103	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 2 - eDP Main Link Frequency Compliance	193103	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 2 - eDP Non ISI Jitter Test	30103	To evaluate the amount of eDP Non ISI Jitter accompanying the data transmission.
Lane 2 - eDP SSC Modulation Deviation Test	180103	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 2 - eDP SSC Modulation Frequency Test	170103	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 2 - eDP Total Jitter Test	20113	To evaluate the eDP Total Jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 2/ Lane 3 - Inter Pair Skew Test	90006	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 2/ Lane 3 - eDP Inter Pair Skew Test	90106	To evaluate the skew, or time delay, between respective differential data lanes in the DisplayPort interface.
Lane 3 - AC Common Mode Test	110004	To evaluate the AC common mode noise, or true and complement mismatch, of the differential data line of a DisplayPort interface.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13910024	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-1dB) - TPS4	12910024	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13910034	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-2dB) - TPS4	12910034	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13910044	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-3dB) - TPS4	12910044	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13910054	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-4dB) - TPS4	12910054	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13910064	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-5dB) - TPS4	12910064	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13910074	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-6dB) - TPS4	12910074	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13910084	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-7dB) - TPS4	12910084	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13910094	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-8dB) - TPS4	12910094	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13910104	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (-9dB) - TPS4	12910104	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13910014	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with Cable Model (TP3_EQ) (0dB) - TPS4	12910014	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - Arbitrary Pattern	13920024	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-1dB) - TPS4	12920024	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - Arbitrary Pattern	13920034	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-2dB) - TPS4	12920034	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - Arbitrary Pattern	13920044	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-3dB) - TPS4	12920044	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - Arbitrary Pattern	13920054	To find the optimized DC gain value for the CTLE.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-4dB) - TPS4	12920054	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - Arbitrary Pattern	13920064	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-5dB) - TPS4	12920064	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - Arbitrary Pattern	13920074	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-6dB) - TPS4	12920074	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - Arbitrary Pattern	13920084	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-7dB) - TPS4	12920084	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - Arbitrary Pattern	13920094	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-8dB) - TPS4	12920094	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - Arbitrary Pattern	13920104	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (-9dB) - TPS4	12920104	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - Arbitrary Pattern	13920014	To find the optimized DC gain value for the CTLE.
Lane 3 - CTLE Optimization with No Cable Model (TP3_EQ) (0dB) - TPS4	12920014	To find the optimized DC gain value for the CTLE.
Lane 3 - Cable Eye Diagram Test	12150004	
Lane 3 - Cable Eye Diagram Test	150004	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Cable Non ISI Jitter Test	12240004	
Lane 3 - Cable Non ISI Jitter Test	240004	
Lane 3 - Cable Total Jitter Test	12230004	
Lane 3 - Cable Total Jitter Test	230004	
Lane 3 - D10.2 eDP Deterministic Jitter (TP3_EQ)	35104	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - D10.2 eDP Random Jitter (TP3_EQ)	38104	To evaluate the Random Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - D10.2 eDP Total Jitter Test (TP3_EQ)	21104	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Eye Diagram Test	10004	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - Fall Time Test (Informative)	50004	To evaluate the lane transition (fall) of a differential data lane in a DisplayPort interface.
Lane 3 - Falling MisMatch Test (Informative)	130004	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 3 - Frequency Accuracy Test	80004	To evaluate that the clock distribution network of the source device conform to within an acceptable tolerance of the nominal operating frequency.
Lane 3 - HBR2CPAT eDP Deterministic Jitter Test (TP3_EQ)	36104	To evaluate the Deterministic Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - HBR2CPAT eDP Total Jitter Test (TP3_EQ)	20104	To evaluate the Total Jitter (TP3_EQ) accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Intra Pair Skew Test	100004	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 3 - Link Layer Phy Change Test - Bit Rate	12320004	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Lane 3 - Link Layer Phy Change Test - Level	12310004	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Lane 3 - Link Layer Phy Change Test - Pre-Emphasis	12300004	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Lane 3 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - Arbitrary Pattern	1339004	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Low Frequency Uncorrelated Deterministic Jitter Test (Informative) - D10.2	1239004	To evaluate the Low Frequency Uncorrelated Deterministic Jitter (UDJ_LF) accompanying the data transmission at either an explicit bit error rate of 1E-6 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - Main Link Frequency Compliance	193004	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 3 - Main Link Frequency Compliance (SSC Frequency Max)	190004	To evaluate the rate variation under all conditions does not exceed +300PPM as set by the DisplayPort standard.
Lane 3 - Main Link Frequency Compliance (SSC Frequency Min)	191004	To evaluate the rate variation under all conditions does not exceed -5300PPM as set by the DisplayPort standard.
Lane 3 - Non ISI Jitter Test	30004	To evaluate the amount of Non ISI Jitter accompanying the data transmission.
Lane 3 - Non Pre-Emphasis Level Test	60004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 3 - Non-PreEmphasis Level Test (Swing 1/ Swing 0)	61004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 3 - Non-PreEmphasis Level Test (Swing 2/ Swing 0)	64004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 3 - Non-PreEmphasis Level Test (Swing 2/ Swing 1)	62004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.
Lane 3 - Non-PreEmphasis Level Test (Swing 3/ Swing 2)	63004	To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Non-Transition Voltage Range Measurement (Swing 0)	72004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 3 - Non-Transition Voltage Range Measurement (Swing 1)	73004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 3 - Non-Transition Voltage Range Measurement (Swing 2)	74004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 3 - Overshoot Test	65004	To evaluate the overshoot and undershoot of a differential data lane in a DisplayPort interface.
Lane 3 - Pre-Emphasis Level Test	70004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 3 - Pre-Emphasis Level Test [D10.2]	71004	This test evaluates the effect of pre-emphasis of the source waveform measuring peak differential amplitude assuring accuracy of pre-emphasis setting.
Lane 3 - Rise Time Test (Informative)	40004	To evaluate the lane transition (rise) of a differential data lane in a DisplayPort interface.
Lane 3 - Rising MisMatch Test (Informative)	120004	To evaluate the difference in rise and fall times of the two single-ended signals in a given differential data lane in a DisplayPort interface.
Lane 3 - SSC Deviation HF Variation Test (Informative)	200004	Verify SSC profile does not include any frequency excursions which would exceed 1250ppm/uSec
Lane 3 - SSC Modulation Deviation Test	180004	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 3 - SSC Modulation Frequency Test	170004	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - SSC Unit Interval Test	160004	To evaluate the overall variation in the Unit Interval width over at least one full SSC cycle to ensure it stays within the spec limit of 300PPM
Lane 3 - Sink Eye Diagram Test	12140004	
Lane 3 - Sink Eye Diagram Test	140004	
Lane 3 - Sink Non ISI Jitter Test	12220004	
Lane 3 - Sink Non ISI Jitter Test	220004	
Lane 3 - Sink Total Jitter Test	12210004	
Lane 3 - Sink Total Jitter Test	210004	

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Lane 3 - Total Jitter Test	20004	To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Lane 3 - eDP Eye Diagram Test	15104	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - eDP Eye Diagram Test (TP3_EQ)	10104	To evaluate the waveform to ensure that timing variabilities and amplitude trajectories are such to support the overall DisplayPort system objectives of Bit Error Rate in data transmission.
Lane 3 - eDP Intra Pair Skew Test	100104	To evaluate the skew, or time delay, between respective sides of a differential data lane in a DisplayPort interface.
Lane 3 - eDP Main Link Frequency Compliance	193104	To evaluate the rate variation under all conditions falls within -5300PPM and +300PPM as set by the DisplayPort standard.
Lane 3 - eDP Non ISI Jitter Test	30104	To evaluate the amount of eDP Non ISI Jitter accompanying the data transmission.
Lane 3 - eDP SSC Modulation Deviation Test	180104	To evaluate the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [The device must] operate in the region of 0 to -5000PPM.
Lane 3 - eDP SSC Modulation Frequency Test	170104	To evaluate the frequency of the SSC modulation and to validate it falls with specification limits.
Lane 3 - eDP Total Jitter Test	20114	To evaluate the eDP Total Jitter accompanying the data transmission at either an explicit bit error rate of 1E-9 or through an approved estimation technique . This measurement is a data time interval error (Data-TIE) jitter measurement.
Link Layer Phy Change Test (Lane 0) - Bit Rate	320001	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 0) - Level	310001	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 0) - PreEmphasis	300001	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Link Layer Phy Change Test (Lane 1) - Bit Rate	320002	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
Link Layer Phy Change Test (Lane 1) - Level	310002	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 1) - PreEmphasis	300002	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Link Layer Phy Change Test (Lane 2) - Bit Rate	320003	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 2) - Level	310003	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 2) - PreEmphasis	300003	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Link Layer Phy Change Test (Lane 3) - Bit Rate	320004	Link layer bit rate test verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 3) - Level	310004	Link layer level test verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.
Link Layer Phy Change Test (Lane 3) - PreEmphasis	300004	Link layer preEmphasis test verifies if the preEmphasis of the DUT can change accordingly from the lowest preEmphasis to the highest preEmphasis setting.
Non-PreEmphasis Level Settings	1206	
Offline Capture Waveform	101	To capture all waveforms required for testing.
PRBS Validation Algorithm Settings	1204	
PRBS Validation Algorithm Settings - DisplayPort 1.1, DisplayPort 1.1a	4	
Pre-Emphasis Level Settings	1207	
eDP Aux Channel Eye Sensitivity Calibration (Reference Sink)	5121	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Sink AUX eye opening has meet the minimum level for futher AUX sensitivity testing.
eDP Aux Channel Eye Sensitivity Calibration (Reference Source)	5131	The test is for calibration purpose to help adjusting AUX eye opening to suitable level. The test validates if voltage swing of a reference Source AUX eye opening has meet the minimum level for futher AUX sensitivity testing.

Table 4 Test IDs and Names (continued)

Name	TestID	Description
eDP Aux Channel Unit Interval Test (Sink)	5110	To evaluate the unit interval of AUX channel.
eDP Aux Channel Unit Interval Test (Source)	5100	To evaluate the unit interval of AUX channel.

4 Instruments

The following table shows the instruments used by this application. The name is required by various remote interface methods.

- Instrument Name — The name to use as a parameter in remote interface commands.
- Description — The description of the instrument.

For example, if an application uses an oscilloscope and a pulse generator, then you would expect to see something like this in the table below:

Table 5 Example Instrument Information

Name	Description
scope	The primary oscilloscope.
Pulse	The pulse generator used for Gen 2 tests.

and you would be able to remotely control an instrument using:

```
ARSL syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
arsl -a ipaddress -c "SendScpiCommandCustom 'Command=[scpi
command];Timeout=100;Instrument=pulsegen'"

arsl -a ipaddress -c "SendScpiQueryCustom 'Command=[scpi
query];Timeout=100;Instrument=pulsegen'"


C# syntax (replace [description] with actual parameter)
------------------------------------------------------------------------
SendScpiCommandOptions commandOptions = new SendScpiCommandOptions();
commandOptions.Command = "[scpi command]";
commandOptions.Instrument = "[instrument name]";
commandOptions.Timeout = [timeout];
remoteAte.SendScpiCommand(commandOptions);

SendScpiQueryOptions queryOptions = new SendScpiQueryOptions();
queryOptions.Query = "[scpi query]";
queryOptions.Instrument = "[instrument name]";
```

```
queryOptions.Timeout = [timeout];
remoteAte.SendScpiQuery(queryOptions);
```

Here are the actual instrument names used by this application:

NOTE The file, "InstrumentInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

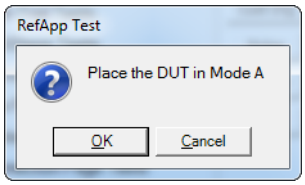
Table 6 Instrument Names

Instrument Name	Description
Infiniium	The primary oscilloscope

5 Message IDs

During the normal course of operation, an application displays multiple message prompts. The application's remote interface exposes a callback capability which enables remote clients to receive the text found in the prompt and to programmatically select the desired response (OK, Cancel, etc.). In order to determine which message is being received, the remote program could parse the message and look for key words. However, because message text is subject to change, a more reliable approach is to use the "message ID" that is attached to the more frequently-seen messages. The following table shows the IDs of the messages that this application may prompt during nominal operation.

For example, if the application may display the following prompt:



then you would expect to see something like this in the table below:

Message	ID	Responses	Usage
DUT mode message	313AEE2F-9EF0-476f-A2EB-29A5C7DE686F	OK=action completed and proceed, Cancel = abort test	App

- Message – A summary of the message in the prompt.
- ID – A unique code that will never change for this prompt, even if the message text changes (assuming the underlying purpose is maintained).
- Responses – The buttons on the prompt and their actions.
- Usage – The scope of the message:
  - "Common" – This message/ID may be used by other apps.

- "App" — This message/ID is unique to this app.
- "<testID>" — This message/ID is unique to this test ID.

A remote client would then structure the code in its message callback handler as shown below to manage message identification:

```
private static void OnSimpleMessage(object sender, MessageEventArgs e)
{
  if (e.ID == "313AEE2F-9EF0-476f-A2EB-29A5C7DE686F")
  {
    // Add code here to set the DUT in Mode A

    e.Response = DialogResult.OK;
  }
}
```

Here are actual message IDs used by this application:

NOTE The file, "MessageInfo.txt", which may be found in the same directory as this help file, contains all of the information found in the table below in a format suitable for parsing.

Table 7 Message IDs

Message	ID	Responses	Usage
Acq Limit: Can't determine minimum bandwidth	25A86458-151E-413D-B890-FC30CFD5ECAA	OK	Instrument
Activating limit will conflict with existing resutls	31A39751-6019-41de-89DF-59DB239DF978	OK=delete conflicting results, Cancel=cancel activation	Instrument
Already running tests	022467B0-6E08-40eb-B4D4-BBB018FBFBC7	OK	Instrument
App startup aborted	C2B67F67-E5D5-4845-8B63-443781223010	OK	Instrument
Can't set memory depth	FFFF1129-BD83-4318-993E-64C94033CEC4	OK=skip step and continue, Cancel=abort test	Instrument
Channel Setup: Unknown scope channel	CDE944EB-F440-4CB1-AFDC-7596461BCD86	OK	Instrument
Compliance/Debug mode change	9C72A970-8D7D-4b37-9787-48AEEA5DC3F1	OK=change mode, Cancel=abort action	Instrument
Confirmation Required	37437505-160C-4cc8-BA06-093C12994C1E	OK=continue, Cancel=abort test	Instrument
Connection change	879629E6-78FA-4a87-B247-A9DB4F0D7330	Abort=abort run, Retry=connection changed - continue run, Ignore=connection not chagned - continue run	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
Debug pause (messages vary)	50B66A97-A6A9-413f-8329-76DFAC492FD6	OK=resume, Cancel=abort run	Instrument
End of run summary	602F9866-F975-42b7-842C-D8447E5E3FCB	OK	Instrument
End of run summary (test aborted)	124580E4-4486-42d4-B908-C6D0FB2AEE93	OK	Instrument
Error during CSV file generation	C88B1C64-8334-4b15-8727-81F5E2BA2ED4	OK	Instrument
Error during app exit	81112706-F720-4787-81D3-B22A9B692B41	OK	Instrument
Expected signal not found	86C74779-322E-4585-A07A-26A2C8FAAC84	Abort=abort test, Retry=retry failed action, Ignore=skip failed step	Instrument
Expected signal not found	7957D5B8-E62D-4224-A7DD-70361E816A43	Retry=retry failed action, Cancel=abort test	Instrument
InfiniiSim: Not available because scope default prevented	B8461A2C-9F5F-4AF3-94C1-DF77080D517A	OK	Instrument
InfiniiSim: Scope doesn't support settings found in project	C9BC2205-8041-448b-AF31-CF602183E989	OK	Instrument
InfiniiSim: Unknown scope channel	4E5ECAF6-867C-47B3-982D-5F07E2090703	OK	Instrument
No test selected	B5D233AD-9EB4-4ac2-A443-A30A13643978	OK	Instrument
PrecisionProbe and InfiniiSim controllers turned off after config change	B4477006-D6D1-4375-9FF7-D8177FFC1BF9	OK	Instrument
PrecisionProbe/PrecisionCable: Not available because scope default prevented	6E60C9F8-8FBF-419C-B70A-B666FBDE3677	OK	Instrument
PrecisionProbe/PrecisionCable: Scope doesn't support settings found in project	2FC3B6FA-E28C-4700-9F46-4ABBA86A0D90	OK	Instrument
PrecisionProbe/PrecisionCable: Switch Controller is enabled	22F46DA8-89AE-4370-A57C-571DCF5BB87E	OK	Instrument
PrecisionProbe/PrecisionCable: Unknown scope channel	6788685B-9E88-47E6-BAE6-862F5BF3C9BA	OK	Instrument
Project loaded as read-only (reason)	98C785F8-D24F-4758-A18D-1CCE61F25371	OK	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
Project loaded with errors	58AD7A02-1E63-4d77-BC6C-6EF3E37AAD5B	OK	Instrument
Project not loaded	B2615E9C-5ED7-4db7-AEAF-2BC25C62B656	OK	Instrument
Project save failed (unauthorized access)	89DCC194-6254-4902-AE63-B7CCD12C8B2A	OK	Instrument
Run paused	FE2CF871-6D4A-4080-8FF9-770075590D9F	OK=resume, Cancel=abort run	Instrument
Setting change requires result deletion	8732A3AB-142C-47e5-86EA-DB737F415DDE	OK=delete results; Cancel=abort change	Instrument
Store mode change requires result deletion	884CDFDE-605E-4d04-B8FD-9B181E7FA468	OK=delete results, Cancel=abort change	Instrument
Switch Matrix controller turned off after config change	FC95EBAA-F33F-4eae-90BB-6A6A8F16E2DF	OK	Instrument
Switch Matrix: Auto mode unavailable after config change	6E5589DC-E073-4818-9E8A-782A75898475	OK	Instrument
Switch Matrix: Auto mode unavailable for model, all settings will be reset	F78BD2E2-BF29-42e0-98F8-23B6CE565B08	OK=go auto do reset, Cancel=abort action	Instrument
Switch Matrix: Confirm Auto mode	D5E1A12E-6218-4416-8451-5F9415D924BF	OK=go auto, Cancel=stay manual	Instrument
Switch Matrix: Obsolete items in settings discarded	0C45BD20-E0C2-481e-A3B6-9C1A26C2103A	OK	Instrument
Switch Matrix: Reconnect drivers	047FE44F-B251-49fa-B3C7-5590317230CD	Yes=use saved addresses, No=prompt for new addresses, Cancel=reset all settings	Instrument
Switch Matrix: Remove all InfiniiSim settings	C5560182-73BE-4901-941E-3DAEC9F07B33	OK=remove, Cancel=abort action	Instrument
Switch Matrix: User cancelled settings load	50F3FB70-AA6B-488e-8CFA-62CDA756F746	OK	Instrument
SwitchMatrix: Correction reset due to application route change	95FEA629-3BE1-4288-BA34-426516018B07	OK=Accept new routing, Cancel=Reset switch matrix settings	Instrument
SwitchMatrix: Instrument already connected to another driver	08556148-4D63-4edd-B894-22916F39849A	OK	Instrument
SwitchMatrix: Max num drivers exceeded	7D8994AB-FCC2-4294-87B3-19B972BB6510	OK	Instrument

Table 7 Message IDs (continued)

Message	ID	Responses	Usage
SwitchMatrix: Reset after drive reconnect fail	CF3E93B6-77FA-4FD7-B656-D286BE1C7C75	OK	Instrument
SwitchMatrix: Reset after drive reconnect fail	D298A4B8-F077-49BE-9CB2-AE6C14FB4705	OK	Instrument
SwitchMatrix: Unexpected multi-SPDT module	2723591D-55A9-44F3-9318-B732995D9427	OK	Instrument
SwitchMatrix: Unknown current switch state	ECE6535B-5C1A-4688-9E45-FB255435CC92	OK	Instrument
Unknown EEyeLocation parameter	FCA1C61B-D2EA-4671-AD48-9C080A6C6039	OK	Instrument
Upgrade app to open project	794C6148-ADF4-4b24-895D-74D94B76F8AE	OK	Instrument

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