IC Trends
Very-large-scale integration has led to a decrease in gate costs with improvements in performance, but along with these benefits grows the challenge of determining the most cost-effective way of making sure a chip is correctly manufactured. Physical defects on wafers have a probability of occurrence proportional to the defect density of the process technology. Current fault models are used to represent likely faults (stuck-at, delay, etc.) in a global context, but do not account for all possible defects. For example, advances in multilevel metallization processes have introduced new classes of defects for which new fault models must be developed for detecting “soft defects” such as noise, cross-talk, and signal integrity.

Defect escape rate – a measure of defects that escape the test – is a function of the probability of defects (defect density) and the test coverage. Defect escape rate will translate into a probability of faults at the next level of integration of the part, thus the earlier the detection, the lower the cost of correction. A defect caught at the chip level costs pennies on the dollar, while a defect caught in the field will cost thousands of dollars to correct. While test equipment evolves rapidly along with the development of integrated circuits, a lingering concern to lower the cost of test and improve time to volume propels the semiconductor industry to work in tandem with test vendors to continually develop design for test (DFT) methods that will facilitate more expedient and cost-effective test procedures.

Introduction to DFT
Design for Testability, commonly known as DFT, is a collection of existing and future techniques, used during design, that facilitate higher defect coverage, faster time to volume, and lower cost of test. Some of these techniques are general guidelines while others are hard and fast design rules, each with their own cost of operation and ROI. DFT methodologies have been in general (ad hoc) use by semiconductor companies for many years, but a more structured approach is being driven by a paradigm shift in how semiconductors are tested. Escalating test costs as a percentage of overall semiconductor manufacturing cost and increasing test development and diagnostics time has led manufacturers to incorporate DFT methodologies into the design phase via electronic design automation (EDA) tools. Their effectiveness is found at the test development and diagnostics stages, where TTV (time-to-volume) is critical, and the test execution or production stage, where defects are detected.
Considering possible defects in the design phase, semiconductor manufacturers can employ appropriate fault models for a given technology. This will ensure lower defect rates after test, while optimizing the test flow. Structural test techniques – such as Scan (DC/AC), BIST and IDDQ – are being widely used today. Slowly, new improvements are being developed in the industry, but Agilent will drive for breakthroughs and invent solutions that will revolutionize test.

**Customer Driven Design**

Test customers want faster time to volume. They need test to happen as automatically and as early in the cycle as possible. Companies who utilize design for testability eliminate the variables that drive up test development time, test execution time, defect diagnostics time, and complexity. Because some customers lack knowledge and expertise on DFT, they need to partner with chip designers to remove organizational barriers between design and test. EDA vendors are valuable partners for Agilent in this effort.

In this relationship between Agilent and EDA developers, customers win by receiving seamless transition from design into silicon and test, faster time to volume, lower cost of test and direct access to DFT experts.

In order for DFT and DFT-based testing to proceed, five key efforts need to happen simultaneously in intelligent test development:

1. DFT technologies must expand beyond stuck-at and delay fault models to include design specifications that allow additional and sufficient control and observation.
2. EDA vendors must automate and drive down the design effort of DFT to liberate design resources for the customer.
3. Early customers must contribute to DFT blueprints; their experience in the process will give the market momentum to change the test paradigm.
4. Semiconductor ATE test equipment needs to make the use of DFT as simple, intuitive, effective and economical as possible.
5. ATE vendors must provide semiconductor manufacturers with improved time to volume through the use of automated test program generation and diagnostic tools and linkages back into the EDA world.

**Agilent’s DFT Expertise**

Functional semiconductor test techniques attempt to emulate the final operating environment of the part by using a combination of at-speed test techniques; however, the component has to ultimately function in the system. With formidable competency at system-level functional test, Agilent leverages the knowledge story with core competencies in IC testers, DFT, and test techniques used at the board and system levels back to the semiconductor level in the form of broad DFT.
Cost of Test
A thorough cost of test analysis needs to address:

- Opportunity cost,
- DFT insertion time,
- IC real estate for DFT,
- Test program generation time,
- Tester capital cost,
- Tester cost of ownership (test time),
- Defect rate level (warranty) and
- Cost of root cause analysis for yield improvement (failure diagnostics).
- Time to Volume

Agilent’s DFT Strategy
Agilent’s vision for DFT is to create test that scales with Moore’s law at the customer’s market pace and removes barriers between design and test.

To that end Agilent is committed to:

- Driving breakthroughs in DFT development that will make it comprehensive, effective and robust;
- Partner with early customers to drive the market with customer-oriented solutions;
- Establish enabling alliances between manufacturers and leading EDA vendors in IC design; and
- Make the use of DFT methodologies as simple and economical as possible through the use of automated test program generation and diagnostic tools.
In fact, Agilent has already begun linking EDA tools to specific Agilent testers; alliances are already forged with Test Insight, Ltd., Synopsys and SynTest. One of the first tools to come out is the Agilent SmarTest Digital Program Generator product (N1150A) that provides the semiconductor manufacturer with an interactive tool for automated test program development and offers a seamless link from the EDA/DFT environment to the IC Test environment (see Figure 1). Additional EDA alliances will be announced in the future.

![Diagram](image)

**CLOSING THE EDA TO TESTER GAP AROUND DFT**

**Figure 1**

Agilent is poised to raise the bar of intelligent test, providing pivotal DFT solutions to customers at the pace of technology.