

# Booth Demonstration Details

DesignCon 2020, January 28-30, 2020

## Keysight Technologies Booth 725

Keysight's technical experts and application engineers will demonstrate the most advanced design and test solutions, developed for solving today's most difficult high-speed digital measurement challenges. Keysight is proud to be the host sponsor of DesignCon 2020.

### DDR5 Tx Design and Test

Keysight will demo a **total solution approach to DDR5** transmitter test. We provide new measurement science for efficient and accurate measurement results that include: automated compliance test for faster test time, BGA interposer for easy access to signal for testing, and seamless connection to data repository for quick test result analysis and fast decision-making process.

### DDR5 Rx Design and Test

Keysight will demo DDR5 receiver test using the M8020A BERT, UXR-Series oscilloscope, and M80885RCA DDR5 Rx compliance test software. Each new generation of the standard introduces new DDR physical layer test requirements. This is particularly true with DDR 5.0, which introduces **new receiver compliance tests** that were not required with previous generations of the standard. In collaboration with the Joint Electronic Devices Engineering Council (JEDEC) organization that defines DDR specifications, we develop measurement methods that test to precise industry specifications.

### PCIe 5.0 Tx Test

Keysight is the only T&M company on the PCI-SIG board. Keysight will demo a new PCI Express (PCIe) 5.0 transmitter test solution with the UXR-Series oscilloscope and D9050PCIC PCIe 5.0 Tx compliance test software. Technologies such as 400G Ethernet are driving I/O interconnect technologies, including PCI Express (PCIe), to 32 GT/s in the 5th generation of that standard. This increase in digital transmission speed and throughput introduces **significant signal integrity challenges**, issues such as connector crosstalk, receiver jitter sensitivity, and overall channel insertion loss, related to transmitter signal quality around the Nyquist frequency at which the PCIe 5.0 standard operates.



## PCIe 5.0 Rx Test

Keysight will demo a PCIe 5.0 receiver test solution with the M8040A BERT, UXR-Series oscilloscope, and N5991 Rx compliance test software to validate a robust receiver that can tolerate **significantly attenuated signals at 32 GT/s**. PCIe 5.0 utilizes aggressive equalization techniques that help the receiver restore the quality of the transmitted signal allowing for error-free recovery of the digital information from the PCIe signal. Due to these high data transfer rates, PCIe receivers often receive a heavily degraded signal resulting from the channel's high-frequency loss characteristics, resulting in unacceptable bit error ratios (BERs).

## 400GE PAM4 Tx Test

Keysight will demo a total solution approach to 400GE transmitter characterization. 400G signaling technology presents **extremely tight design margins**, and engineers demand higher instrumentation precision to extract margin for Tx characterization and validation. This demo station will examine SNDR and related 400G validation measurements on Keysight's N1000A DCA-X sampling and UXR-Series oscilloscopes.

## 100 GBaud Error Analysis

Keysight will demo a solution to design next-generation digital interfaces running at **speeds beyond 60 GBaud**. It offers great flexibility in terms of speed, modulation formats, as well as digital signal processing at the transmitter and receiver side. This solution includes Keysight's M8196A AWG and UXR-Series oscilloscope. In this demo we will show in-depth analysis of error mechanisms to improve designs and estimate link margins under different forward error correction scenarios.

## Layer 1 Test With FEC

Keysight will demo a compliance test solution for 400GBASE devices and components. Current and next-generation data communication networks will use 4-level pulse amplitude modulation (PAM4), forward error correction (FEC), and equalizing receivers to **achieve increased bandwidth** in data center networks. The solution consists of the M8040A BERT, combined with the A400GE-QDD, and a multiport 400G Ethernet module tester. It is designed to integrate FEC constraints into the physical design validation.

## Validate PAM4 400G BER

Keysight will demo its A400GE-QDD 400G Layer 1 BERT and FEC measurement system that provides BERs simultaneously on all electrical lanes in real-time. The A400GE-QDD **evaluates the performance of FEC for PAM4 encoded signaling** in a fast (minutes not days) and efficient manner. Testing of optical transceivers, silicon devices, and copper DACs can now be done cost-effectively with a test solution specifically targeted for these measurements. The A400GE-QDD meets customers' requirements for reduced setup and measurement times.

## USB 4.0 & Type-C

USB4 is based on the Thunderbolt 3 technology. Keysight has been involved with Thunderbolt 3 in the silicon phase and has enabled Thunderbolt 3 customers for the past 5 years. We now bring our expertise and solutions to enable USB4 customers. USB4 will transmit 20 Gb/s on all 4 lanes of the Type-C connector in parallel over passive cables. The demo will showcase Keysight's solutions for USB4 over a lossy, low-cost, passive cable using the UXR-Series oscilloscope.

## Signal Integrity Analysis

Keysight will demo how a digital designer can develop intuitive insight into the transmission of digital data from the transmitter through the channel interconnects to the receiver. Hyperscale data centers are being developed all over the world, providing both the scale and the resource density needed to handle the massive workloads of big data and IoT. While much of the attention surrounding hyperscale is on its advanced server, storage, and internal networking architectures, it will also require extreme bandwidth over everything copper. Backplanes, line cards, ethernet cables, and even connectors become microwave transmission lines at 400G data rates.

## Power Integrity Analysis

Keysight will demo software and hardware for designing, measuring, and analyzing power distribution networks. **PathWave ADS PIPro Software** provides power integrity analysis of power distribution networks (PDN), including DC IR drop analysis, AC impedance analysis, and DeCap optimization. Model building and PI channel measurement will be shown with the P5028A Keysight Streamline USB Vector Network Analyzer. We will also show the N7020A Power Rail Probe and the D9010POWA Power Integrity Analysis Software, which together complement each other and provide a powerful means of measuring and analyzing power integrity.

## DDR5 IBIS-AMI Simulation

Keysight will demo system simulation of DDR5 using IBIS-AMI models, with an enhanced bit-by-bit channel simulator adapted specifically to the needs of DDR. PathWave ADS 2020 U1, provides a fast system setup with Memory Designer, an easy and accurate EM extraction process with SIPro, and the capability to **close the loop with measurement on hardware** by performing the same compliance tests on simulated waveforms.

## PathWave Design & Test Software

**PathWave** Desktop Edition is a design and test software platform for agile and connected engineering workflows. It accelerates your product development workflow by connecting every step in your path — from design and simulation, to prototype and test, to manufacturing — connected and integrated.

## KeysightCare

KeysightCare offers the industry's first cloud-based customer experience with dedicated, proactive support through a single point of contact for instruments, software, and solutions. We help you improve your time to market and reduce costly unplanned downtime and project delays through proactive engagement, faster response times, faster access to specialized experts, and faster time to resolution.

## Next Step

See you at DesignCon 2020!

Keysight will deliver eight complimentary, 40-minute education workshop sessions led by industry experts. [Click here for Keysight Education Forum](#) abstracts and additional details on all eight sessions.

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