Performance at the DUT: Techniques for Evaluating the Performance of an ATE System at the Device Under Test Socket

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Abstract

“Performance at the DUT” is a key phrase in the test and measurement industry and is used to indicate the true electrical signals that exist at the reference plane where the Device Under Test (DUT) connects to the Automated Test Equipment (ATE). The limited specifications provided by test equipment manufacturers and the fact that the test fixture can be a major source of signal degradation create significant challenges in measuring these signals. This paper presents the results of an industry collaboration to address some of these challenges for ATE applications running at 5 Gbps or greater. Topics include probing techniques for measurements at the DUT interface, calibration methods for measuring test fixture effects, source characterization at the DUT, and test fixture de-embedding from the measured device data.

Authors’ Biographies

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**Mike Resso**, the Signal Integrity Measurement Specialist in the Component Test Division of Agilent Technologies, has over twenty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high-speed digital interconnects utilizing Time Domain Reflectometry (TDR) and Vector Network Analysis (VNA). Mike has twice received the Agilent Spark of Insight award for his contributions to the company. He has authored or coauthored over 25 professional publications and received one US patent. Mike received a Bachelor of Science degree in Electrical and Computer Engineering from the University of California.

**Antonio Ciccomancini Scogna** is an application engineer at CST of America. He received the Ph.D. degree in electrical engineering from the University of L’Aquila, Italy in 2005, with a dissertation focusing on full-wave simulations and de-embedding techniques for the characterization of PCB discontinuities. In 2004 he received the CST University Publication Award for the use of the FIT technique in signal integrity applications and in August 2005 he joined CST. He is a member of IEEE.

**Orlando Bell** is VP of Engineering at GigaTest Labs. He joined GigaTest Labs after completing his MSEE at the University of Florida. For the past decade, he has specialized in the characterization of high-frequency interconnects based on measurements and the design of measurement fixtures for the DC to 20 GHz range. In addition, he heads the device characterization effort at GigaTest Labs, a measurement and model extraction service for BJT, GaAs FET, pHEMT devices.

**Ming Tsai** is a principal engineer at RF Design Group in Amalfi Semiconductor Inc. Prior to joining Amalfi, he was a staff hardware development engineer at Xilinx responsible for signal integrity analysis for high-speed signal transitions, and for high-speed loadboard design and characterization. He joined Xilinx in October 2004 and earned his Ph.D. degree from the electrical engineering department of the University of California, Los Angeles in 1996.
Introduction

“Performance at the DUT” is the ideal specification for an Automated Test Equipment (ATE) test fixture but one quickly finds that this simple definition is rather complicated to implement for I/Os running at multi-gigabit data rates. At data rates below 1 Gbps the propagating edges are on the order of inches in length, long enough that the signal at the test fixture PCB socket interface is roughly equal to the signal at the package bump and even further in at the IC. However, for multi-gigabit ATE systems running with 30 pS rise times, one can no longer make this assumption. The rise time edge occupies less than 200 mils and requires transmission line theory to understand the performance at each of these interfaces and how they interact with each other as they propagate through the test fixture to the DUT [1]. Depending on what previous data or simulations are available for correlation the ATE test fixture designer will often struggle on understanding whether to put the measurement plane at the IC, at the package bump, or at the transmission line on the test fixture board. It is desirable to have the DUT performance broken down such that the data can be used to evaluate the packaged device performance in the targeted application environment and not skewed by ATE test fixture induced characteristics.

Figure 1: “Performance at the DUT” specifications are not limited to ATE applications. Backplane applications also need to know how the backplane interconnect components distort the signal going into the device.

This signal integrity challenge is not limited to the ATE test community. Signal integrity issues plague many high-speed digital interconnects including backplanes, connectors, cables, PCBs and IC packages. The performance of the device at the device, excluding the electrical effects of the fixturing, is the ideal benchmark. Users of test and measurement equipment always face the challenge that instrumentation is typically specified to the “front-panel” or in the case of an ATE system the pogo pin interface at the test head. There can easily be significant discontinuities through connectors, cables, and PCB routings to or from the device that degrade the signal from its initial value. To
This paper looks carefully at the physical interface structures involved with a DUT on an ATE test fixture to understand the interactions that take place in the ATE environment. Probing and characterization methods will be shown for separating out the performance of the test fixture so that “Performance at the DUT” can be accurately obtained from a combination of measurements and 3D-EM simulations. The paper will start with a basic understanding of the benefits of simple test fixture calibration techniques that can provide accurate skew and simple loss models for the ATE test fixture. Interposer design and probing techniques will be demonstrated to provide a standard reference plane for test fixture measurements at the PCB and DUT interface. Advanced calibration techniques such as probe vendor supplied calibration substrates, custom PCB Through-Reflect-Lines (TRL) calibrations, and 3D-EM simulation de-embedding techniques will be discussed to show the benefits of improved calibration techniques to accurately de-embed the test fixture for multi-gigabit applications.

A design case study will show the results from a test fixture designed for a quad core microprocessor with I/Os running above 5 Gbps on an ATE system (Verigy V93000). The results from this demonstration will clearly highlight the challenges of measuring the “Performance at the DUT” and they will provide insight into the interactions of the test fixture PCB, and the DUT for these multi-gigabit data rate. The paper will conclude with a review of the results of obtaining the synthesized DUT performance based on the various calibration techniques and a discussion of the accuracy of the results. The results will show that the increasing data rates will force one to rely more heavily upon 3D-EM simulations to predict the interaction at an interface.

**Probing Technology, Interposer Design, and Mechanical Challenges**

This section discusses the three main technologies needed for fully characterizing a test fixture using probing techniques at the DUT interface. The characterization measurements can be done either isolated on a bench or docked to an ATE system.

**Probing Technology**

To measure the performance at the socket with enough fidelity for multi-gigabit signals and to obtain accurate S-parameters for de-embedding and model generation it is necessary to use high-performance micro coaxial probes. Figure 2 shows a picture of the micro coaxial probes used in this paper together with their individual performance measured by the manufacturer showing that the probes have sufficient characteristics to at least 40 GHz for the needed measurements.
Figure 2: The GGB Picoprobe Ground-Signal-Ground (GSG) with 400um pitch (left), probing an ATE test fixture (middle) and insertion loss performance of the probe measured by the manufacturer (right).

Micro-coaxial probes are designed for wafer probing and are fairly delicate as their electrical requirements can only be met by building mechanical compliance into the tips and ground wings. This delicate probe tip is unable to provide the mechanical force required to compress socket pins, and in addition the ground wings can be damaged if they get caught on the socket contacts. This is an important reason for using a probe interposer board for mating the probes to the DUT interface which is described in the next sub-section.

The probes come in a variety of configurations with signal only (S), ground-signal (G-S), and ground-signal-ground (G-S-G) contacts at the tip. High frequency performance is typically limited by the added inductance of the ground connection discontinuity and one finds that the G-S-G topology provides the best impedance matching by lowering this inductance. The G-S-G probes can be purchased with a variety of Ground to Signal spacings to accommodate the ATE applications ranging from DUT interface types (needles or socket) to tester interface (coax and/or pogo block). The former are usually in the 0.1 mm to 1 mm range, while the latter run in the 1 mm to 3 mm range. Electrically one finds that a tighter G-S spacing that is closer to the dimensions of the ~12 mil 50 ohm micro-coax used in the fabrication of the probe will improve the impedance matching. This small pitch of the G-S spacing on the probe then requires the use of a probe interposer board to provide this contact spacing and a transition to the DUT pin I/O topology.

**Interposer Design**

One of the main challenges in probing the test fixture where the DUT resides is the fact that the contact pitch between the signal pins and the reference pins can vary greatly not only due to the DUT I/O topology but also due to the pin out where the closest reference pin (e.g. GND in a single ended measurement) might be far away. Ideally one would like to use a fixed pitch probe to probe any signal pin without worrying about the pin-out of the device. The solution is to develop a PCB board known as the probe interposer that provides pads on the bottom for connecting to the ATE test fixture DUT interface and
pads on the top with a fixed ground to signal pad spacing of 5 mils for connecting to the probes. The ground to signal pad spacing is achieved by flooding the topside with a copper pour that direct connects to all ground pins and has a circular clearance around all signal and power pins (Figure 3). Filled vias with over plating provide a planar surface for the socket contacts and the probe landing. Ideally one would like the probe interposer to be as thin as possible to minimize the impact on the electrical performance of the measurement, however, mechanically the board must be thick enough to avoid significant bending when compressing the high density of socket pogo pins when measuring at the socket pin interface. A thickness of 100 mils was evaluated and determined to be sufficient for the compression of this 3.85 mm x 3.85 mm array of 1,200 pogo pins.

![Image of interposer and probe](image.jpg)

Figure 3: Example of an interposer designed for a specific BGA ball-out (left), interposer attached to the loadboard for probing connection (middle), and 400 um G-S-G probe tip connection to the probe interposer board (right).

**Mechanical Challenges**

Properly probing a test fixture presents several mechanical issues. For example, in an ATE test fixture the DUT socket pins and the ATE pogo vias are usually on opposite sides of the test fixture PCB requiring simultaneous measurement on two separate faces. Other complexities can arise in trying to accommodate the integral mechanical stiffener attached to the large ATE test fixture, mechanical attachments for temperature forcing environmental systems, and electrical connectors for added test capability. These items can cause mechanical interference with probes which have a limited vertical clearance typically ranging from 3 to 5 mm. Another problem of ATE test fixtures is that they are usually large and heavy which add to the complexity of maintaining a rigid probing connection. Figure 4 shows the mechanical solutions developed for the Verigy V93000 ATE system that can be used for probing the test fixture on the bench or with the test fixture docked to the ATE system.
Figure 4: Mechanical solution for probing an ATE test fixture. Left: Mechanical fixture with probe positioner attached to the loadboard that is in turn docked to the ATE system. Right: Mechanical fixture with probe attached to the ATE test fixture including legs for bench measurement and pogo pin to SMA block assembly for through path measurements.

Calibration Techniques

The first issue that arises in obtaining calibrated electrical performance of the ATE test fixture is that the ATE tester interface with the pogo pins or coaxial connections is not the same as the probing interface where the DUT socket resides. Therefore, a special calibration technique must be used to place the measurement reference plane at the coaxial connectors on one end and at the probes on the other. At DC this is a simple correction of subtracting out the losses of the cables and adapters used by the measurement system. At higher frequencies the calibration increases in complexity with reflection, radiation, and phase changes as well as the resistive losses being considered. Techniques have been developed with frequency domain network analyzers to provide NIST traceable calibration methods for moving the electrical reference plane to the end of the measurement cables for accurate characterization of the electrical performance of a DUT [6].

The simplest calibration technique, called an “insertable calibration” places reference standards on each port or cable end and then measures the through path by connecting the two measurement cable ends together. In the case of a DUT such as the ATE test fixture where one end is a probe interposer and the other is a coaxial connector, then an adapter is needed for connecting the two measurement cables together for the through path calibration. This requires a “non-insertable” calibration technique such as a “defined-thru”, “unknown-thru” or a two tier “adapter removal” calibration. Calibration standards come in the form of open, short, load, through and multiple through line lengths for connecting to the measurement cables and one must identify which combination of standards provides the best accuracy versus measurement simplicity for a given
application. A very common selection of coaxial standards is the SOLT calibration or Short, Open, Load, Through. Calibration standards can easily be purchased for a variety of coaxial connector types, and even the probe manufacturers sell characterized thin-film calibration substrates. However, the probe interposer board presents a challenge since it requires the design of custom standards. Experience has shown that the Through-Reflect-Multiple Lines (TRL) calibration standards can easily be fabricated on a PCB and provide the ability to move the electrical reference plane onto the PCB test fixture or to the bottom of the interposer board [5,7].

Figure 5: Qualitative comparison of fixture error reduction techniques and the PCB implementation of a TRL calibration for the probe and probe interposer. Note that the accuracy of the S-Parameter De-Embedding assumes a perfect data set in this graph and that actual accuracy will depend on which calibration method is used to obtain the de-embedding S-Parameters.

The theory of this calibration technique works quite well (Figure 5). However, implementing this technique for an ATE test fixture application poses a considerable challenge. The non-insertable calibration using customized standards requires a significant number of connections to be made as is the case for connecting the probes to as many as 7 standards in some TRL calibration kits. Increasing the number of network analyzer ports or cable connections from 2 to 4 compounds the problem and consideration of the case of 12 or 16 ports with a TRL calibration in this fashion becomes prohibitively time consuming [5]. The other issue is that as the number of required calibration standards increases so does the probability of an operator error and one can easily get an erroneous calibration.

A practical solution to this problem is to identify a way to use an automated Electronic Calibration module to the ends of the network analyzer cables to minimize operator connection errors and provide a NIST traceable reference plane. Then using post processing tools, one can de-embed the effects of the adapters required to connect from the NIST traceable reference plane at the end of the network analyzer cables to the desired reference plane on the ATE test fixture [8,9]. This method as shown in Figure 6 also provides the advantage of checking the data before and after the de-embedding of the adapter to make sure that the calibration method used to remove the adapter is providing
the desired accuracy. Now the issue becomes one of accurately measuring or simulating the electrical data for the adapters that are used to get to the desired reference plane such as the probe and probe interposer board in the case of the ATE test fixture.

Figure 6: NIST traceable coaxial calibration to the end of the Network Analyzer cables combined with Loadboard Probe Adapter de-embedding to get ATE Test Fixture S-Parameters.

As we mentioned before, the “non-insertable” calibration method of adapter removal with a TRL calibration will allow placement of a coaxial reference plane on one cable end and a PCB reference plane on the other. This is precisely what is needed for measuring the adapter going from the network analyzer coaxial cable connector to the ATE test fixture reference plane (Figure 7). This adapter removal with TRL calibration can be quite tedious for the case of the probe connection, but with this technique it only needs to be done for two ports, it does not have to be done at the same time or place as the ATE test fixture measurements, and the method can be repeated over time to evaluate the electrical repeatability of the adapter.

Figure 7: Utilization of TRL Calibration standards and adapter removal methods to move the measurement plane to either side of the G-S-G Probe so that the electrical performance can be measured for the desired application.
In theory the TRL calibration structures work quite well but here again the practical implementation does not always work as well as one would like. A large challenge comes in matching the ground reference topology for the ATE test fixture measurement with that used by the calibration structures. Probes are essentially point sources that can only launch signals at specific locations. By contrast, many DUT and tester interfaces use several grounds and have other signals in close proximity, therefore the flow of the ground currents at the reference plane may not match those measured with the calibration structures. In some cases this can lead to inconsistencies in the launch response. The use of an interposer adds to this grounding complexity since now the calibration structure needs to account for the probe and the interposer connection to the ATE test fixture. In an ideal world one would fabricate separate calibration structures for every signal pin to be measured so that the grounding topology can be replicated in the calibration. However, this would be time and cost prohibitive.

To understand the effect of the neighboring ground vias on the measurement path, one can run a simple experiment of probing a signal via pad with 1, 2, 3, or 4 neighboring ground vias in the DUT via field being probed.

![Figure 8: Experiment to see the effect of ground vias next to the signal via.](image)

The insertion loss and reflection data in Figure 8 show that for frequencies below about 10 GHz the use of 1 ground via versus 4 ground vias results in minimal differences for frequencies below 10 GHz. The TDR reflections from the probe end (Figure 9) also show that the best match is achieved with 4 surrounding ground vias at the DUT BGA pin out locations.
Figure 9: TDR at the probe end showing how the impedance discontinuity and resonant ringing decreases when the number of surrounding ground vias is increased.

Simulations of the interposer (Figure 10) show that the resonance is coming from the structure of the neighboring via field as the signal transitions through the interposer. In the case of the interposer calibration structures, these neighboring pins are coupling with the signal pins as frequency increases and the design of the interposer above 10 GHz becomes a challenge.

Figure 10: Simulations of the Probe Interposer design show that with only one neighboring ground via the unterminated adjacent vias can start to resonate. The grounding topology of the neighboring vias will vary when attached to the loadboard and this resonance will shift.

**Measuring the Probe and Probe Interposer Adapter**

Now that a method of calibration and an understanding of the challenges in making the adapter from the network analyzer coaxial cable to the desired reference plane on the ATE test fixture have been established, the TRL calibration structures can be fabricated.
TRL calibration and coaxial SOLT calibration with adapter removal will then allow the ability to measure the performance of this adapter for future de-embedding on test fixture measurements (Figure 11).

![Figure 11: Adapter Removal Calibration with PCB TRL standards and coaxial SOLT standards provides measured S-Parameters of the G-S-G Probe and the Probe with Interposer. This allows one to de-embed this data and move the reference plane to the end of the probe tip or to the bottom of the interposer board.](image)

Measuring just the probe connecting to the top of the interposer with the TRL adapter removal calibration shows data that is very similar to the calibration data provided by the vendor (Figure 2) and indicates that the interface of the interposer to the probe is working well. Measuring the probe and the interposer together (probe interposer adapter) with the reference plane at the bottom of the interposer shows that it matches well with the 3D-EM simulation. Figure 11 illustrates the resonant roll-off in the probe interposer adapter insertion loss similar to interposer simulations with only one adjacent ground via.

Looking at the bandwidth of the measured data for an ATE test fixture path of 17 inches of stripline prior to de-embedding the probe interposer adapter can provide some useful insights into how well the de-embedding process will work. The filter roll-off resonance location has moved further out in frequency then that measured for 1 neighboring ground via on the interposer indicating that the grounding topology and connections of the interposer to the real ATE test fixture is closer to a neighboring via topology of 3 grounds and should work well with the adapter de-embedding for frequencies of 10 GHz and below.
At frequencies above ~10 GHz one will need to look at improved calibration structures to better match the reference plane location on the ATE test structure. A simplistic way of looking at this reference plane issue is to consider two perfect 50 ohm coaxial cables of different dimensions (Figure 13).

Figure 13: Obtaining S-Parameter data on individual components does not guarantee that they will give the correct answer when cascaded together in a simulation. (3D-EM simulations using CST Microwave Studio time domain solver.)
Both of these 50 ohm cables would have S-parameters with very low loss and extremely small reflections and if one cascaded the S-parameters together in a simulator tool the result would be a low loss, low reflection cable. However, in the real world when one tries to connect these two different cable sizes together there is a physical discontinuity that can cause significant reflections or low pass filtering of the data. Placing a reference plane at such a location makes it difficult to build the standards in a way that the measurement technique does not significantly change the physical topology. For the case of a socket or a PCB via field, this would mean creating standards that expand in the vertical direction at the reference plane requiring sockets or PCBs with varying height. Varying the height of the socket or the PCB can add significant cost and time to a project and one may still question the ability to accurately fabricate the appropriate structures.

A better solution is to look at the use of 3D-EM simulation to provide a flexible tool for evaluating the interaction of two materials at a reference plane. The 3D-EM tool will also provide insight into the benefits of coupling for differential probing applications. The previous analysis assumes that the coupling is low and relies on single ended calibration techniques to avoid the more complex structures and calculations required for a multi-mode 4-Port TRL [5]. The other advantage to using a 3D-EM simulation tool is that it will also provide insight into how one can optimize or improve the probing adapter to ATE test fixture for higher data rate applications.

**Test Fixture Performance Measurement**

Now that a method has been established to de-embed the affects of the loadboard probe adapter and move the electrical reference plane to the DUT via field pads on the ATE test fixture we can compare the measured results with more traditional methods. A very common way to obtain the electrical data for a signal path on an ATE test fixture is to fabricate a test coupon with traces routing to coaxial connectors that simulate the best and worst case routing topologies (Figure 14).

![Figure 14: Example ATE Test Coupon fabricated on the same panel as the ATE Test Fixture. The test coupon will typically include min and max trace routings for each signal layer to quantify the losses and assist in the analysis of the DUT data measured with the Test Fixture.](image)

Plotting the data for the minimum and maximum trace lengths for 4 different signal layers shows how there can be as much as 4 dB of loss between the best and worst case...
traces on an ATE test fixture at 10 GHz. Transforming this data to loss per inch by subtracting the maximum and minimum trace length losses for a given layer shows that some of the differences are also coming from variations in the stripline dielectric losses. This data clearly shows the benefit of correcting the data to remove the effects of the ATE test fixture.

Figure 15: Variation in loss for different signal layers and different routing lengths. Total loss is shown on the left and then a loss per inch is shown on the right based on subtracting the minimum and maximum trace losses for a given layer.

Measuring the corresponding minimum 13 inch trace routing on the ATE test fixture by probing at the DUT via field with the probe interposer adapter shows a higher loss then the data from the test coupon (Figure 16). The difference is more than 1 dB at 10 GHz which is more than a 10% difference in voltage levels.

Figure 16: Trace loss for a 13.218 inch trace on the ATE test fixture versus the loss for the same length trace on a test coupon.

Other options exist such as consulting a probing house whom can perform full S-Parameter characterization. The probing house typically has neither the luxury of a coaxial pogo-pin to PCB adapter for the ATE interface nor a custom probe interposer for
the DUT interface end. Without the custom interfaces, one must select from a variety of probe spacings to find the best fit for the via field topologies connecting to the signal path. The pictures below (Figure 17) illustrate the type of setup required for making these measurements. The physical size of the test sample and the two-sided probing requirement dictate the need for a custom probing system with four positioners on a dual platen-system with remote optics. The positioners are able to swivel ±45 degrees on the platens, enabling the user to access the ground pins in multiple orientations. This capability is the key to probing directly on the pogo vias and on the device footprint.

Figure 17: Measurement of ATE Test Fixture by probing directly at the pogo vias on the ATE interface location and with the probe interposer adapter at the DUT location.

The measurements using the pogo-pin assembly compare well with the double-sided probe-based measurements, the difference being the signal-loss of the pogo-pin assembly which is on the order of 1 dB at 10 GHz.
Focus Calibration on an ATE system: Measuring “at-the-DUT”

The calibration examples in the previous section were all done by taking bench measurements of the test fixture and the resulting data provide an in-depth understanding of the losses of the test fixture and the accuracies involved in using a probe interposer adapter to measure “at-the-DUT performance. The frequency dependent losses measured on the ATE test fixture clearly show that at multi-gigabit data rates the long 30+ cm traces typical for a dense microprocessor application can significantly degrade the signals to and from the DUT. The increasing loss with frequency causes data-dependent level and timing jitter in addition to degrading the signal slew rate [2,3]. The standard ATE calibration to the pin electronics does not take into account any of the test fixture losses and this results in measured device data with less performance margin than what is expected. Applying the probe interposer technique to the in-situ focus calibration of the ATE system will allow the measurement of the “Performance at the DUT” for the ATE transmitted signals going to the DUT and for the DUT signals being received at the ATE pin electronics.

One typical approach for determining the “Performance-at-the-DUT” is to use a time domain transmisometry (TDT) or a vector network analyzer (VNA) to obtain trace loss data for each channel by employing either the simple test coupon approach or the higher accuracy measurement of each channel using the probe interposer. This data can then be used to de-embed the effects of the test fixture on the measured signal (e.g. by filtering the signal through an appropriate software filter that compensates for the test fixture effect) for a DUT transmitter eye height measurement or to define how much level compensation is needed for the ATE driver to get the needed data eye opening at the DUT for a receiver tolerance test. The accuracy of this method will depend on the ability to obtain accurate ATE pin electronic models over the desired frequency range.

A specific example of this is to “focus calibrate” the data eye height that is provided to a DUT receiver for a “receiver tolerance” test. Since the test fixture will add data-dependent level and timing jitter, it is expected that the programmed level on the ATE software will not correspond to the eye height seen by the DUT receiver. The proposed measurement-based modeling approach is to simulate the data eye at the DUT using a model of the pin electronics, pogo assembly and the measured test fixture S-Parameters. In this example of a Verigy V93000 PinScale HX card, the pin electronics already contains an integrated equalizer [3,4] that compensates for part of the loss and also needs to be included in the simulation. Figure 18 shows the simulation setup implemented using Agilent ADS.
Figure 18: ADS simulation setup for evaluating the needed focus calibration factor for the receiver sensitivity test.

Note that the simulation uses a very simplistic model of the pin electronics. Figure 19 (left) shows the simulated data eye at greater than 5 Gbps with a PRBS7 data pattern. The pin electronics driver levels were set to a 350 mV differential swing with the objective that the DUT receiver sees a 350 mV eye opening at approximately the middle of the data eye. From the simulated eye opening (Figure 19 left) a focus calibration scaling factor of 1.64 was derived for achieving the 350 mV eye opening at the DUT for this data pattern. Figure 19 (right) now shows the date eye at the DUT receiver with the programmed level swing at the ATE pin-electronics calibrated by the 1.64 factor and obtaining the 350 mV eye opening.

Figure 19: Simulated data eye without any focus calibration factor (left) and with the focus calibration factor inferred from the simulation (right).

If measured data is unavailable for the test fixture then one could use trace geometry, length, and dielectric material to simulate the loss of the test fixture for use in determining the focus calibration factor. However, as shown in Figure 15 the dielectric losses can vary from layer to layer and the losses of the via transitions are not insignificant and thus a simple transmission line model will have limited accuracy.
The measurement based modeling approach with VNA measured S-Parameters makes it easy to model a wide variety of data patterns and data rates. However, it is generally useful to verify the simulations with an in-situ focus calibration measurement to cross check the results. The in-situ probing measurement at the DUT has the advantage of using the active ATE pin electronics source signal with its inherent jitter characteristics. Figure 20 shows a picture of a manual focus calibration system (prototype) docked to a test fixture on the ATE system.

![Figure 20: Manual focus calibration system (prototype) docked to the test fixture and ATE system.](image)

The idea is to measure the stimulus signals from the ATE pin electronics at the DUT and in the other direction be able to inject a stimulus at the DUT that can be measured by the ATE pin electronics as shown in Figure 21.

![Figure 21: ATE "at-the-DUT" focus calibration approaches.](image)

The same process implemented in Figure 18 is used to determine the calibration factor needed to correct the eye height at the DUT but this time the focus calibration setup shown in Figure 20 will provide the data for derivation of the focus calibration factor. Figure 22 shows a comparison of the differential data eye using an optimal test fixture for the integrated pin-electronics equalization (as mentioned before the ATE pin electronics used in this example already includes an integrated equalizer) for a 350 mV single ended greater than 5 Gbps PRBS7 data signal and the same signal measured with the interposer probing setup for the 16.4 inch 10 mil signal trace.
Figure 22: Comparison of the single ended data eye at greater then 5 Gbps with a PRBS7 data pattern using an optimal test fixture for the pin electronics equalization (left) and using the longest trace (16 inch) in the ATE test fixture for a microprocessor characterization application (right). Note that vertical scales are not equal.

From the measured results it is clear that the inner eye height (defined by the markers) is significantly reduced compared to the optimal test fixture trace and more important both do not provide the exact 350 mV data eye height at the DUT. This is expected given that the trace is longer and thinner. It is then necessary to compensate for this reduction of the eye height by using a higher programmed voltage swing from the tester pin electronics. Figure 23 shows the results comparing the data eye with the ATE driver programmed to 350 mV and with the ATE driver programmed to 800 mV. This means that a calibration factor of approximately 2.28 is needed for this measurement point.

Figure 23: Comparison of the single ended data eye at greater then 5 Gbps with a PRBS7 data pattern without any calibration factor (left) and with the calibration factor (right). (Note that vertical scales are not equal).

The difference in the calibration factor when compared with the simulation based results is expected since the simulation model of the pin electronics does not model perfectly the ATE driver and more work needs to be invested in refining the simulation. It is expected that the time domain simulation would provide more optimistic results and that the in-situ calibration is pessimistic in that it also includes the probe interposer adapter and cabling to the measurement instruments.
The previous examples only dealt with focus calibrating the stimulus signal from the ATE system at the DUT, but as shown in Figure 21 it is also important to calibrate or de-embed the signals measured by the ATE receiver for the test-fixture loss. Figure 24 shows a real example of de-embedding the test fixture effects from the measured waveform and data eye using the test fixture characterization data to develop an inverse filter for convolving with the measured data pattern.

All of the approaches described in this section can be repeated for other ATE focused calibrations, for example the transmitter eye height measurement or the jitter tolerance test. It is important to notice that items like data-dependent jitter (DDJ) due to inter-symbol interference are not that easy to focus calibrate or de-embed. Therefore the simplest approach to reduce it is to compensate for it by equalization embedded on the pin electronics or on the test fixture [4].
Conclusion

Accurate measurement of DUT performance is needed for understanding how a device will perform in its target environment. This paper clearly shows that achieving “Performance-at-the-DUT” characterization on an ATE system is not a simple task as data rates enter the multi-gigabit domain. Long trace routings that are typical in high density microprocessor ATE test fixtures can easily degrade the signals and calibration techniques are required to remove these test fixture effects.

A probe interposer technique has been described that allows one to obtain accurate electrical performance of the test fixture up to 10 GHz and 3D-EM modeling techniques have been suggested for going higher in frequency. The probe interposer technique was compared with less accurate test coupon trace measurements and trace simulations to show that above 3 GHz the more sophisticated direct probing of the actual test fixture trace does make a difference. The probe interposer technique has the added benefit that it can enable VNA calibrations that use custom PCB TRL standards to move the reference plane for the S-parameter measurements to the interface of the DUT with the ATE test fixture.

“Focus Calibration” of the ATE system refers to a variety of techniques that are used for in-situ calibration of the ATE pin electronics to get “at-the-DUT” signal characterization. Simulating ATE pin electronic models with the measured S-parameters of the test fixture signal trace can provide a powerful tool for synthesizing the quality of the eye reaching the DUT and for de-embedding the test fixture effects from the measured data at the pin electronics. Accurate models for the ATE pin electronics that include jitter and frequency dependent source and receiver effects are not easy to obtain and so one must be careful to check the simulations with in-situ measurements at the DUT to ATE test fixture interface by using the probe interposer. Bench instrumentation can then be used to measure the signal coming from the ATE pin electronics, or to inject a known source signal into the tester.

The test fixture will clearly be the bottleneck as the pin-count and data rates continue to increase on ATE applications. Advancements in equalization techniques are coming that will allow much stronger integrated and programmable equalization on future ATE pin electronics [10] to compensate for test fixture losses. However, the challenge of how to correctly program this equalization remains and it will be necessary to measure and stimulate the signal at the DUT and feedback this information to the ATE system to correctly program the pin electronics equalization. This is the only way to assure the highest levels of measurement accuracy.

This paper cannot address every type of ATE “focus calibration” measurement, but the methodology used in evaluating the validity of the probe interposer technique demonstrates a systematic approach that can be applied in general for qualifying a multi-gigabit measurement at a complicated three-dimensional interface. The presented techniques of moving the measurement reference plane through de-embedding will
hopefully lead to the ability to separate out the performance of the Integrated Circuit (IC),
the IC and the package, and the full combination of IC, package and socket from a single
set of measured ATE data for improved correlation between the die performance and the
final packaged performance in the target environment of the end application.

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