Enable New Generation of Display Interface
啟動新一代高清晰顯示介面

Instructor: 余宥浚
Agenda

1. HDMI 2.0 introducing
2. MHL3.2 introducing
3. DisplayPort v1.3 updating
4. eDP v1.4 Electrical performance and validation solution
High Definition Multimedia Interface (HDMI)
HDMI Organizational Structure

- **HDMI LLC** is responsible **up to HDMI 1.4b**
  - Ruled by “7C” (7 founding companies)
  - No open industry participation in the definition of the Spec
  - CTS (Compliance Test Spec) includes vendor-specific test procedures

- **HDMI Forum** is responsible for **HDMI 2.0 and later**
  - Open industry consortium with 80+ members
  - Keysight is a member of the Technical Working Group and Test Subgroup
  - CTS describes generic test procedures – vendor independent
  - MOI’s (method of implementation) is created by each T&M vendor
  - Keysight was recently elected into Board of Directors
HDMI 2.0

Objectives of 2.0

- Increase the TMDS data rate to 6 Gbps
- Add protocol testing for 4:2:0 4k2k 50/60 Hz (2.97 Gbps)
- Add some protocol layer enhancements (3D, etc)
- Add a Direct Attach mode
- Add a Status Control and Data Channel (SCDC)
- Scrambling for EMI/RFI reduction
The HDMI 1.4 Interface

Transmitter

- Data TX
- xN PLL
- Ck

Sink (Display)

- Data RX
- xN PLL

Channel (cable)

TMDS (AV Link)

Ck Frequency = Data Rate/N

HDMI1.4:

Data Rates: 250M to 3.4 Gbs

N=10

EDID

HDCP

HEC/AR

Ethernet/Audio Return Channel

E-DDC (i2c)

CEC

+V

Controller
The HDMI2.0 Interface

HDMI 2.0 Interface Changes

**Transmitter**
- Data TX
- xN PLL
- Ck

**Sink (Display)**
- Data RX
- xN PLL

**Channel (cable)**
- TMDS (AV Link)
- Ck Frequency = Data Rate/N
- HDMI2.0:
  - **Data Rates**: 3.4 Gbs to 6Gbs
  - **N=40**

**New Feature**
- E-DDC (i2c)
- Ethernet/Audio Return Channel
- EDID
- HDCP
- SCDC
- HEC/ARC
- CEC Controller

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[Image of a diagram showing the HDMI 2.0 interface changes, including the transmitter and sink, channel (cable), and various signals and components such as Ck, Data TX, TMDS (AV Link), and control signals like EDID, HDCP, SCDC, HEC/ARC, and CEC.]

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**Keysight Technologies**

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Software Worst Case Cable Emulator for Tx Tests

Source Data Eye Diagram Test Setup

- Proposed Worst Cable Model shall be embedded into Oscilloscope.
- Effect of Crosstalk, Cable Attenuation and Cable Skew can be reflected.

**Source DUT**

- TPA-P
  - Diff. Probe
  - Single-ended Input
  - Termination

**Oscilloscope**

- CLK
- De-embed TPA-P/R (S4p)
- Worst Cable Model (S4p)
- EQ
- Eye Measurement

**Actual Crosstalk at Connector**

**Panasonic Proposed Worst Cable Model**

**TP2 Eye Diagram**
Source Skew 0.15Tbit
Source Jitter 0.3UI
Software Worst Case Cable Emulator for Tx Clock Jitter

DUT
5.94 Gbps Tx

TPA-P

+3.3V
Pull up Termination for non measured channel

Ch1: Clock + (single-ended)
Ch3: Clock - (single-ended)

N5380A/B 1169A probe

Keysight Scope
13 GHz or higher

Test both cases of 112 ps delay in positive and negative sides
Software Worst Case Cable Emulator for Tx Data Eye

DUT
5.94 Gbps Tx

+3.3V Pull up Termination for non measured channel

TPA-P

Ch1: Clock differential or Single-ended
Ch2: D1+ (single-ended)
Ch4: D1- (single ended)

Keysight Scope
13 GHz or higher

N5380A/B 1169A probe

Test both cases of 112 ps delay in positive and negative sides

CRU

112ps

EQ

Draw eye

Ch1: Clock differential or Single-ended
Ch2: D1+ (single-ended)
Ch4: D1- (single ended)
Equalization in HDMI

Equalization is stipulated to follow the relation below for freq response.
Phase of equalizer must be manifest to yield causal filter with this response.

\[
|H(j\omega)| = \begin{cases} 
  e^{N\omega^N} & (\omega < \omega_0) \\
  e^{-B(\omega-1.2\omega_0)^2} & (\omega_0 < \omega < 1.4\omega_0) \\
  e^{-D\omega+E} & (1.4\omega_0 < \omega) 
\end{cases}
\]

Where
\[
\begin{align*}
N &= 0.7 \\
\omega_0 &= 2\pi \times 2.5\text{GHz} \\
A &= 9.7E-8 \\
B &= \frac{7}{4} \times A \omega_0^{-1.3} \\
C &= 1.07 \times A \omega_0^{0.7} \\
D &= 0.7 \times A \omega_0^{-0.3} \\
E &= 1.98 \times A \omega_0^{0.7}
\end{align*}
\]

*Figure 6-2: Reference Cable Equalizer for 3.4 Gbps < R_{OK} ≤ 6 Gbps*
## Tests Identified in HDMI

<table>
<thead>
<tr>
<th>HDMI 1.4b Test</th>
<th>Test Point Coverage</th>
<th>Measurement Type Required</th>
<th>HDMI 2.0 Test</th>
<th>Test Point Coverage</th>
<th>Measurement Type Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2 TMDS $V_L$</td>
<td>TP1</td>
<td>Single Ended</td>
<td>HF1-1 $V_L$ and $V_{\text{swing}}$</td>
<td>TP1</td>
<td>Single Ended</td>
</tr>
<tr>
<td>7-3 Voff</td>
<td>TP1</td>
<td>Single Ended</td>
<td>HF1-2 Rise and Fall Times</td>
<td>TP1</td>
<td>Differential</td>
</tr>
<tr>
<td>7-4 TMDS Rise and Fall Times</td>
<td>TP1</td>
<td>Differential</td>
<td>HF1-3 Inter Pair Skew</td>
<td>TP1</td>
<td>Differential</td>
</tr>
<tr>
<td>7-6 TMDS Inter Pair Skew</td>
<td>TP1</td>
<td>Differential</td>
<td>HF1-4 Intra-Pair Skew</td>
<td>TP1</td>
<td>Single Ended</td>
</tr>
<tr>
<td>7-7 TMDS Intra-Pair Skew</td>
<td>TP1</td>
<td>Single Ended</td>
<td>HF1-5 Differential Voltage</td>
<td>TP1</td>
<td>Differential</td>
</tr>
<tr>
<td>7-8 TMDS Clock Duty Cycle</td>
<td>TP1</td>
<td>Differential</td>
<td>HF1-6 Clock Duty Cycle/Level</td>
<td>TP1</td>
<td>Differential</td>
</tr>
<tr>
<td>7-9 TMDS Clock Jitter</td>
<td>TP1</td>
<td>Differential</td>
<td>HF1-7 Clock Jitter</td>
<td>TP2EQ</td>
<td>Single Ended</td>
</tr>
<tr>
<td>7-10 TMDS Data Eye</td>
<td>TP1</td>
<td>Differential</td>
<td>HF1-8 Data Eye</td>
<td>TP2EQ</td>
<td>Single Ended</td>
</tr>
</tbody>
</table>
**Test Fixture**

*Wilder* fixtures have been re-designed for only a small difference in performance - they may go up to 11 GHz now. *Bitifeye* fixtures have been shown to exceed 13 GHz in performance. They are quotable and orderable.

**Wilder TPA HDMI Plug Fixture**

**Bitifeye 0101-0200-0 Plug Fixture**
New FlexEDID(VTF-501 FlexEDID)

- Enables arbitrary EDID images to be used.
  - SW can now download arbitrary EDID file to control test device. Single Format files will drive transmitter devices to correct bit rate for test.

- Fully Integrated to HDMI Compliance Test Software.
  - When active, single format files for specific resolution/format for test will be downloaded and the hot plug event will be activated.

- Enables Test Plan
  - Software keeps track of all that needs to be tested for the formats selected so you don’t have to!

- Comes with a $V_{cc}$ output that can be controlled independently.

Created by Vprime for Agilent.
HDMI 2.0 test solution overview from Keysight

Source Test
N5399C HDMI Electrical Compliance Test Software

Cable Assembly Test*, Source and Sink Impedance Tests
E5071C Option TDR ENA Network Analyzer

Sink Test (ParBERT)
N5990A Automatic SW for HDMI compliance
E4887A ParBERT TMDS Signal Generator
new Cable Emulator

Sink Test (AWG)
N5990A Automatic SW for HDMI compliance
M8190A/M8195A AWG

Protocol Test
U4998A SW for HDMI compliance
U4998A (N5998A) HDMI 1.4 protocol analyzer/generator

For HDMI 2.0 third party protocol testers are planned to be supported in the ValiFrame SW

DSO90000A Infinium real time scope 13 GHz

HDMI 2.0 TPA

HDMI 1.4*

or 2.0 TPA

13 GHz
The implementation in the HDMI compliance software allows virtually limitless possibilities in transfer function generation for our users to go far beyond mere compliance test.
Test Device: Control and Capability

For your device:
- HDMI1.4b & HDMI2.0?
- What are the Formats it can do?
- HDCP On/Off?
- How are you going to control it?
Physical Layer Cable Assembly Testing

Points to Know:

- HDMI2.0 doesn’t require new cable testing; still follows HDMI1.4b spec
- Standard Cable measurements for characterization and compliance testing: skew, impedance, attenuation, and crosstalk.
- “Stressed” Eye Diagram Analysis of Interconnects: allowing direct measurement of eye characteristics at the end of the link.
- Optional switch and test automation software available from Solutions Partner BitifEye

Time Domain
- Intra-Pair Skew (T31, T42)
- Inter-Pair Skew (Tdd21)
- Impedance (Tdd11)
- Impedance (Tdd22)

Frequency Domain
- Attenuation (Sdd21)
- Phase (Sdd21)
- FEXT (Sdd21)

Eye Diagram Analysis
- Jitter insertion
- Emphasis
- Equalization

Complete characterization of interconnects (Time domain, frequency domain, and Eye diagram)
Physical Layer Source/Sink Impedance Testing

Points to Know:
- Impedance measurements of Source and Sink required in HDMI2.0
- Source impedance measurements during transmission of actual data pattern (Hot TDR measurements) is required
- DC voltage bias can be applied through internal bias-tees
- Hot TDR with ENA-TDR, fast, accurate and no worry about ESD
HDMI 2.0 Sink Test Setup

ParBERT *and* AWG are supported

Same N5990A Test automation controls both setups

ParBERT E4887A

AWG M8190A/M8195A

Plus real-time oscilloscope for calibration (in both cases)

Much lower cost
Fewer accessories
Less re-configuration

ParBERT E4887A

Same N5990A Test automation controls both setups

ParBERT E4887A

AWG M8190A/M8195A

+ Bias-Ts

+ TTCs

+ Bias-Ts

+ Delay lines

Plus real-time oscilloscope for calibration (in both cases)
Mobile High Definition Link (MHL)
The clock is added in as a **common mode signal** to the differential signal that transmits the color data. The receiver then has both **differential and common mode detection circuits**.
MHL 1.0 and MHL 2.0: MHL 1.x Architecture

- Pixel Clock: **75MHz** (720p60, 1080p30)
- Serialized at: **225MHz**
- Data Transfer Clock: **75MHz**
- Data Transfer Rate: **2.25Gbps**
- **24 bits per color** transfer

Standard High Definition resolutions handled

From Synopsis website
MHL 1.0 and MHL 2.0: MHL 2.x Packed Pixel Mode

- Pixel Clock: **150MHz** (1080p60)
- Serialized at: **300MHz**
- Data Transfer Clock: **75MHz**
- Data Transfer Rate: **3.00 Gbps**
- 16 bits per color transfer

Now 1080p/60 handled
40 bits transmitted in a pixel clock cycle
uUSB connector is the de facto connector because of its presence in the mobile market.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Cable color</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Red</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>2</td>
<td>D-</td>
<td>White</td>
<td>Data -</td>
</tr>
<tr>
<td>3</td>
<td>D+</td>
<td>Green</td>
<td>Data +</td>
</tr>
<tr>
<td>4</td>
<td>ID</td>
<td></td>
<td>Mode Detect. May be N/C, GND or used as an attached device presence indicator (shorted to GND with resistor)</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Black</td>
<td>Ground</td>
</tr>
</tbody>
</table>

D- and D+ is the differential data lane.

ID: USB mode detect.
MHL 3.0 objectives

- Transmit at 6Gbs to handle 4kx2k 30Hz
- Implement Peripheral support (touch screen keyboard mouse) data traffic capability between portable and tv.
- Increase Charging capability to 10W (to handle higher power devices-i.e. tablet)
- HDCP 2.2 supported
- Enhanced 7.1 surround sound
- Support of multiple displays
- Backward Compatible with MHL1 and MHL2

6Gbs capability and added requirement of HID Data traffic requires the MHL AV link structure to be re-designed.
# MHL 3.0 Signal Changes

<table>
<thead>
<tr>
<th>Pin</th>
<th>MHL1&amp;2</th>
<th>MHL3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBus</td>
<td>VBus</td>
</tr>
<tr>
<td>2</td>
<td>MHL-</td>
<td>MHL-</td>
</tr>
<tr>
<td>3</td>
<td>MHL+</td>
<td>MHL+</td>
</tr>
<tr>
<td>4</td>
<td>CBus</td>
<td>eCBus-S</td>
</tr>
<tr>
<td>5</td>
<td>Ground</td>
<td>Ground</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>The MHL-/MHL+ is ONLY Differential in MHL3.</td>
</tr>
<tr>
<td>extended cbus has:</td>
</tr>
<tr>
<td>- original cbus functionality</td>
</tr>
<tr>
<td>- forwarded MHL clock</td>
</tr>
<tr>
<td>- handles forward and reverse data</td>
</tr>
</tbody>
</table>

There is NO common mode clock in MHL3.0
CBus line now requires more validation rigor.
MHL to Display: a simplified view

- MHL TMDS (differential pair)
- eCBus-S (single ended)
- Sync
- MHL Clock
- eCBus Data
- CBus/clock Logic
- CBus conversion
- AV Decode
- HID
- EDID
eCBus-S

Functions:

- MHL 1.x/2.x Discovery/Control (original Cbus).
- MHL3.0 recognition (Display capability).
- MHL clock forwarding for AV link decode.
- Forward and Reverse Data transmission.
MHL Clock on eCBus-S

- MHL Clock is fixed at 75MHz
- To support the **fixed rates** of MHL AV links this means the divide ratio changes...

<table>
<thead>
<tr>
<th>AV Link Rate</th>
<th>1.5Gbs</th>
<th>3.0Gbs</th>
<th>6.0 Gbs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Divide Ratio</td>
<td>20</td>
<td>40</td>
<td>80</td>
</tr>
</tbody>
</table>

- Clock Rising Edges are detected at the Sink
Data is transmitted on Falling Edges
Forward Data is easy to understand…

‘0’ transmitted  ‘1’ transmitted
eCBUS data on eCBus-S

- Data is transmitted on Falling Edges
- Reverse (Backward) Data

Conceptual diagram:

- MHL TX
- eCBus
- x1
- Diff amp
- BWD Data
- +Edge Detect
- Clock PLL
- MHL Clock
- Display
- HID
- FWD Data
- -Edge Detect

Transmitted data:
- '0'
- '1'

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eCBUS

Portable Device

AV Content

TMDS Clock/Discovery

Falling Edge Mod

FWD Data

BWD Data Rcvd

TMDS+

TMDS-

V_{BUS}

GND

eCBus

x1

Diff amp

Television

AV Data Detection

Panel

HID

BWD Data TX

+Edge Detect

FWD Data

-Edge Detect

Clock PLL

Discovery Logic

MHL Interface

MHL Clock

Panel

AV Data Detection

HID

BWD Data TX

+Edge Detect

FWD Data

-Edge Detect

Clock PLL

Discovery Logic

MHL Interface

MHL Clock
MHL3.0 Testing

Protocol and Physical Layer testing for Sink and Source

Since all MHL3.0 devices must support MHL 1.0 and MHL 2.0, they must pass the current MHL 1 & MHL 2 compliance test regimens.

Requires full **TMDS** (MHL Data) pair measurements.

Requires full **eCBus** validation (forward and reverse scenarios)
Electrical Layer testing

– MHL 3 electrical layer tests require that all Legacy MHL electrical layer tests are conducted first
  • Test setups for MHL 1 and 2 are required
  • Keysight / BitifEye offer a modular and scalable solution portfolio, the MHL 3 setups are add-ons to the MHL 1 and 2 setups

– Keysight / BitifEye support the following instrument configurations:
  • DSO for source Tx testing – already available
  • ParBERT E4887A-007 for sink/dongle Rx+Tx testing – available in Dec. ’14
  • AWG M8190A for source Rx testing – β-S/W available
  • AWG M8190A for sink/dongle Rx+Tx testing – available in 2015
  • Note that ParBERT cannot be used for MHL 3 source Rx testing (see next slide)
N6460B MHL Source Testing
Upgrade information: New Fixtures and Equipment

• MHL 3.0 Fixtures
  • new fixtures with high-speed eCBUS connectors
  • some of the old fixtures might be re-used for cal
  • availability and price TBD (Wilder)

• RELT Board (Relay-Echo-Cancellation-Level-Translation Board)
  • required for all sink/source/dongle tests
  • provided by Simplay Labs

• Test MCU
  • additional piece of hardware to control RELT
  • provided by Simplay Labs
Display port v1.3 updating
DisplayPort 1.3 Summary

- The VESA DisplayPort Standard, Version 1.3, was released on Sept 15, 2014
- Replaces DisplayPort Version 1.2b for new designs
- Backward compatible, offers new optional features
- Compliance tests expected 1st Half of 2015
Summary of Main New feature for DP 1.3

- 50% increase in video data transfer rate
  - supports higher resolutions
  - deeper colors
  - higher display refresh rates

- Further optimized for use on shared interfaces including DP Alt Mode on USB Type-C or Dockport

- “Living Room Friendly” features added to enhance applicability for consumer displays including digital televisions
DP 1.3 Link Rate Increase

<table>
<thead>
<tr>
<th>DP Version Introduction</th>
<th>Link Rate Name</th>
<th>Bit rate</th>
<th>Max Resolution Support (24 bpp, 60Hz Refresh, 4:4:4 format)</th>
<th>Max Resolution Support (24 bpp, 60Hz Refresh, 4:2:0 format)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP 1.0</td>
<td>RBR</td>
<td>1.62 Gbps</td>
<td>1920x1080</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.0</td>
<td>HBR</td>
<td>2.7 Gbps</td>
<td>2560x1600</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.2</td>
<td>HBR2</td>
<td>5.4 Gbps</td>
<td>4K x 2K</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.3</td>
<td>HBR3</td>
<td>8.1 Gbps</td>
<td>5K x 3K</td>
<td>8K x 4K</td>
</tr>
</tbody>
</table>

Total useable data transfer rate for DP 1.3 = 25.92 Gbps

8.1 Gbps link rate, per lane
x 0.8 to account for 8b/10b transport coding overhead
x 4 maximum number of available lanes

25.92 Gbps total usable data transfer rate
Optimization for Shared Interface Use

- Numerous specification enhancements to simplify the use of DisplayPort as an ingredient in the following interface examples:
  - The USB Type-C connector, using the Display Alt Moe
  - VESA DockPort Standard
  - VESA Mobility DisplayPort Standard (MyDP)
  - VESA Embedded DisplayPort Standard (eDP)
  - ThunderBolt
  - Future wireless interfaces

- Enhancement to DP1.3:
  - Improved link training to accommodate more varied and complex video transport topologies, along with the higher link rate of HBR3
  - The addition of link-trainable repeaters to increase performance and reliability across complex topologies (such as docking station + Hub + active cable)
  - Unified device register set to simplify implementation and allow devices to support various interface types
New “Living Room Friendly” Feature

Support of HDCP 2.2
- New content protection protocol that will be required for viewing premium video content at UHD resolution

Support of DisplayPort-to-HDMI 2.0 protocol conversion
- Enables the support of DisplayPort-to-HDMI 2.0 protocol adapters for use with DisplayPort video source devices, include devices that use the USB Type-C connector supporting DisplayPort Alt Mode

DisplayPort-to-HDMI 2.0 protocol converters will only require the HBR2 link rate and will support 4Kp60Hz in 4:4:4 pixel encoding format and CEC communication
New “Living Room Friendly” Feature (continued)

Support of native 4:2:0 pixel format

- This pixel format is often used for digital televisions to reduce video data rate requirements. The HBR3 link rate, combined with 4:2:0, can support a display resolution up to 8K x 4K (7680 x 4320), also known as QUHD
- Will also simplify DP-to-HDMI 2.0 protocol converter implementation when supporting HDMI digital TVs that require 4:2:0 format
eDP1.4 Electrical Performance and Validation Software (N6469A)
eDP and eDP1.4 Overview

eDP Provides a High-Speed, Bi-Directional Data Path Between the System Host and Display
eDP and eDP1.4 Overview

- Embedded interface targeted at portable devices.
- Prevalent now in laptops and tablets (v1.3).
- Previous instantiation eDP1.3 duplicated standard DisplayPort attributes (bit rate, level, pre-emphasis)
- eDP1.4 reduces power and increases flexibility: 7 bit rates identified, but can be arbitrary.
- 6 levels identified but can be arbitrary in groups of 1, 2, 3 or 4.
- 4 PreEmphasis settings identified, however, PE amount is arbitrary.
- Four connection types identified; all using IPEX connectors 20, 30, 40 and 50 pin interfaces.
- No compliance program is in effect, nor probably ever will be.
- Validators have huge hole in capability.
- Ecosystem has different types of vendors (flexible cable, panel, GPU)
eDP and eDP1.4 Testing Overview

Testing Problems in eDP implementations:

- eDP 1.4 supports Arbitrary settings/capabilities
- Connection models are varied (but at least IPEX connector is chosen)
- No Compliance mandate-internal interface NOT Box-to-Box interface
- Vendor/Supplier potential conflict in performance
This is a new type of application…
- not a compliance application: where
  - the conditions, methods and limits of test are established and documented by a standard, and
  - all implementers agree and obey these requirements.
- but, an ecosystem enabler that:
  - easily handles wide range of conditions to meet the many different integrators’ needs,
  - allows different test methods,
  - enables arbitrary test limits, and
  - facilitates the exchange of this test information between users’ sites, their vendors and their customers.
This is the **first application** to allow a user to define a test plan (device attributes, test methods, and test limits).

This is the **first application** that will enable entities in the supply chain to run identical test plans by merely exchanging a ‘test template’.

It will be the **official first eDP test application**, and the **first that addresses the particular needs of eDP1.4**.

The application extends the **natural, self-guiding GUI** structure started in DP, more thoroughly developed for HDMI, and now comes to **fullest manifestation in eDP1.4**.
Product Definition

✓ Product Model number is N6469A.

✓ Name of the product is ‘eDP1.4 Electrical Performance and Validation Software’.

✓ Targets eDP1.4, but addresses eDP1.3 and is potentially usable for other interfaces.

✓ Provides a GUI for user to input:
  Bit Rates to test, swing levels and pre-emphasis levels to test, and ssc. Test line limits for all tests including mask files for the different bit rates.

✓ Leverages well-accepted and successful DisplayPort tests and GUI structures.

✓ Creates a ‘template’ that can be exchanged with another party to test identically.
What the eDP sw application looks like
Fixture

Manufactured by Wilder Technologies

eDP-TPA40L-PC (kit # 640-0608-000)
40pin model
30 and 50 pin models available.
Questions
Critical Point of DP Certification

Allion Labs, Inc.

Eric Wen
Agenda

- Critical Point of DP Certification
- DisplayPort Standard v1.3 Update
- DP1.3 Link Rate Increase
- HBR3 Capability Example
- DP Alt Mode on USB Type-C
- Example of DP Alt mode configurations
- How to get DisplayPort Certified Logo?
- Allion Engineering Services
Critical Point of DP Certification

- Electrical Test for Sink and Source device takes at least 50% of entire test time.
- CDF (capability declaration form) accuracy will lower delays.
- Graphic and IC vendor are your best friends for device capabilities.
- Allion’s past experiences can also help you determine device capabilities.
- Ask questions before project starts can also help save valuable time.
DisplayPort 1.3 Update

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<td>DP 1.0</td>
<td>RBR</td>
<td>1.62 Gbps</td>
<td>1920x1080</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.0</td>
<td>HBR</td>
<td>2.7 Gbps</td>
<td>2560x1600</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.2</td>
<td>HBR2</td>
<td>5.4 Gbps</td>
<td>4K x 2K</td>
<td>Not supported</td>
</tr>
<tr>
<td>DP 1.3</td>
<td>HBR3</td>
<td>8.1 Gbps</td>
<td>5K x 3K</td>
<td>8K x 4K</td>
</tr>
</tbody>
</table>

8.1 Gbps/lane
x 0.8 for 8b/10b encoding overhead
x 4 maximum lanes
= **25.92 Gbps** total usable data rate
HBR3 Capability Example

- Multi-Stream Transport (MST) feature with HBR3, the following configurations can be achieved:
  - Two 4K UHD (3840 x 2160) displays
  - Up to Four 2560 x 1600 displays
  - Up to Seven 1080p or 1920 x 1200 displays
  - One 4K UHD display with up to Two 2560 x 1600 displays
DP Alt Mode on USB Type-C

- VESA DisplayPort Alt Mode Standard, Version 1, was released on Sept. 22, 2014
  - Enables the use of USB Type-C interface for DisplayPort
  - Thin profile suitable for both ultra portable device or larger device
  - Reversible plug for easy access
  - USB 3.1 Gen2 (10Gbps)
  - USB Power delivery, up to 100 watts
  - Supports DP Alternate Mode
  - High speed data, display, and system power all in one
Example of DP Alt mode configurations

- Source with USB Type-C to Sink with USB Type-C Connected by USB Type-C to USB Type-C cable
- Source with DisplayPort to Sink with USB Type-C Connected by DP to USB Type-C cable
- Source with USB Type-C to Sink with DisplayPort Connected by USB Type-C to DP cable
- USB Type-C Adaptor (HDMI/DVI/VGA)
How to get DisplayPort Certified Logo?

Certification Process:

1. Contact Allion to apply for testing

Material Preparation:
- Application Form (CDF)
- Send in devices
- Operation Instruction or driver if necessary

2. Testing

3. Report reviewed by VESA

Debug

Fail

Re-test

PASS

4. Use Logo on product

5. Adopter sends license to VESA

6. Adopter has VESA License?

Yes

Adopter send product info to VESA

No

Adopter send license to VESA

7. VESA update website

8. Adopter has VESA License?

Yes

Adopter to list product on web?

No

Adopter send license to VESA

No

Adopter to list product on web?
What Allion can offer Besides DP Certification?
Service Overview

With over 20 years of product testing experience, Allion offers technology suppliers complete professional engineering services for every stage of product development.

Preparation Stage
- Test Items Definition & Creation
- Check List Creation
- Test Schedule Arrangement & Management

Validation Stage
- Product Validation
- Digital Ecosystem Interoperability Testing
- RF Validation & Signal Integrity Testing
- Cable & Connector Testing
- Environmental Reliability Testing
- Standard Certification & Compliance
- Software Validation Solutions
- User Experience Optimization
- Superior Consulting Solutions

After-Service Stage
- Product Service Maintenance
- Customer Feedback Issue Tracking
Factsheet

As a leading authority in IT product validation and standards compliance, Allion provides world-class test services and consulting engineering solutions.

- Founded in 1991
- 700+ Qualified Engineers
- 30+ Logo Standard Certification Programs
- ISO/IEC 17025 Accredited
- 10,000+ Pieces of Test Equipment and Devices
- 20+ Years of Product Test Experience
- 300,000+ Test Projects Performed
Global Facilities

Our global facilities provide localized support to technology suppliers and distributors.
Allion is the premier resource for all of your 3rd party testing needs. Our services bring products to market more quickly, reliably, and cost effectively to protect your brand quality and that of your suppliers.

service@allion.com

Thank you!
Granite River Labs

USB Power Delivery, General Scope Protocol Decode and Waveform Bridge Solution

Alan Chuang 莊益林
0917586767
achuang@graniteriverlabs.com
GRL Convenient Locations

- GRL WW HQ & Lab
  Santa Clara, CA
- GRL US R&D
  Beaverton, OR
- Partner Lab
  Boeblingen, Germany
- GRL Taiwan Labs
  Hsinchu & Taipei
- GRL India Lab
  Bangalore
- GRL Malaysia Lab
  Penang
- GRL Japan Lab
  Yokohama
- GRL Asia Pacific HQ
  Singapore
### Connectivity Standards Covered

**Data Bus & Storage**

- **High Definition Video**
  - SlimPort®
  - DisplayPort
  - HDMI 1.4/2.0
  - V-By-One HS

- **High Speed Data**
  - PCIe Gen3/4
  - 10G Express
  - eDP/DP 1.3
  - MHL 3
  - HDMI 1.4/2.0
  - SAS Gen3/4
  - 10G

- **Fiber Channel**
  - 16GFC

- **Ethernet**
  - 1.25G
  - 3.125G
  - 10.31

- **SONET/STM**
  - STM-16
  - STM-64
  - ODU-2

- **ATC**
  - PCIe Gen3/4
  - 10G
  - 16GFC
  - 20G

**Enterprise Datacom & Telecom**

- **SDR**
  - DDR
  - QDR
  - FDR

- **IEEE 802**
  - External Ethernet
  - PHY I/F
  - SGMII, XAUI, SFP+, QSFP+
  - SONET
  - STM-16
  - STM-64
  - ODU-2
  - CEI 6G/11G

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  - QDR
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  - ODU-2
  - CEI 6G/11G

**Mobile**

- **USB Certified**
  - Type C/PD

- **UFS**
  - Future

- **UHS-2**
  - DDR3/eMMC

**Memory Bus & Card**

- **CFast, XQD**

**Future Standards**

- **Future**
  - Type C
  - UFS
  - UHS-2
  - CFast, XQD
Test Setup 1 - USB-PD eMark Cable Testing
Test Setup2 - CC Electrical & Protocol Decode Testing

DUT

10X Passive or Diff Probe Probes

BIST Carrier Mode 2 (alternating 0's and 1's)

Scope

USB/LAN .wfm, .bin, etc.

PC or Scope with GRL-USB-PD Automation SW

Note: Scope Ground needs to be established on only one side of link.
Test Setup 3 - Power Provider Stress

USB-PD Spec. Chapter 7

- Instrumentation Setup

Differential Probe
(Double Probed with DMM not shown)

Passive or Active Probe

Current Probe

Type-C Cable

Type-C Breakout Board

USB-PD Controller

USB/LAN

PC or Scope with GRL-USB-PD-SW Automation SW

USB/LAN .wfm, .bin, etc.

PD DUT

Vbus_US

Vbus_DS

I_U

eLoad - TBD
100W, (0-5A), 150mA/μS Variable Slew Rate
Proposed USB-PD Power Consumer Test Setup

USB-PD Spec. Chapter 7

Instrumentation Setup

- **Differential Probe**
- **Scope**
- **PD DUT**
- **Wilder Coupon**
- **Type-C Cable**
- **USB-PD Controller**
- **PC or Scope with GRL-USB-PD-SW Automation SW**
- **PS**

Vbus_US

Vbus_DS

CC1/CC2

GND

C1

C2

C3

C4

V_U

I_U

CC

PS
GRL Type-C/USB-PD Electrical & Protocol Test Software (GRL-USB-PD)

- SW Available Jan. 2015 (GRL-USB-PD)
  - Supports multiple Vendors Scopes and Performance Levels
  - BMC Eye Diagram & Timing Measurements
    - BitRate, Risetime, CRC Check
  - Bus Diagram and Signal View Window
  - CC Line Packet Decode
  - USB-PD Power Measurements
  - Report Generator
  - VDM Decode for Cables and Adaptors

- Controller Available Q2 2015 (GRL-USB-PDC)
  - Vbus (Voltage & Current) and Power Measurements
  - USB-PD Power Measurements
Electrical Compliance & Decode Using GRL-USB-PD
GRL-USB-PD Software Applications

- USB Power Delivery Rev 1.0
  - Chapter 5 Electrical Tests
  - Chapter 6 Protocol Tests
  - Chapter 7 Power Supply Tests

- USB Type-C Cable Specification
  - Chapter 4 – Type-C Functional Testing

- DisplayPort Alt Mode on USB Type-C
  - Chapter 5 – Discovery and USB-PD
Keysight Scope Protocol Decode
HDMI 2.0/1.4 Protocol Decode and Compliance Test

- Supports HDMI CTS 2.0 and CTS 1.4b
- One-box solution for both HDMI physical- and protocol-layer testing leveraging real-time oscilloscopes.
- Detailed HDMI protocol decodes. Multi-view decode capability:
  Bus viewer
  Frame viewer
  Event viewer
  Data packet viewer
  Protocol viewer
- First HDMI 2.0 Protocol Decode Solution, Supports scrambling
- Decodes RGB, YCbCr pixel encoding
- Supports 24, 30, 36 and 48 bits per pixels
Keysight Scope Protocol Decode
DP / eDP 1.2 Protocol Decode

• Conformance to DisplayPort 1.2 Specification
• Multi-Stream Transport (MST) support
• Supports DisplayPort 1, 2 and 4 lane designs
• Seamlessly links physical layer signals to DPmicro packets to DPstream to video frame
• Links the DP image to pixel details and corresponding micro packets and physical layer signals
• Displays the DisplayPort Stream/frame visually as it is in the specification
• Provides a link between the transmitted stream to the physical layer signal
• Displays the active video, secondary data and audio packets in a readable tabular format
• Embedded hooks to DisplayPort 1.2 Source PHY and Link Compliance Testing …Upcoming
• De-Scrambles DisplayPort physical layer signal
• Decodes RGB, YCbCr pixel encoding formats
• Supports 18, 24, 30, 36 and 48 bits per pixel
• Decodes live and stored waveforms
• Detailed micro packet description
• Automated PDF report generation
• GRL DisplayPort 1.2 Multi-lane
• Protocol Decode Software (GRL-DP-DEC)
• Embedded DisplayPort (eDP) support
Keysight Scope Protocol Decode
SD UHS-II Protocol Decode

- Supports UHS-II version 1.0 Specification
- Decodes all the UHS-II packets transactions for easy debug.
- Provides ability to correlate the UHS-II transactions to physical layer Signals
- Supports Full Duplex and Half Duplex Modes and pictorially represent the flow control
- Detailed packet Description provides every information of the packet
- Export the data to CSV, TXT or PDF file for further analysis
- Decodes the live and offline waveforms
- Supports Data Scrambling
- Oscilloscope auto setup
Test Software Solution

- Keysight VNA/TDR Test Automation Solutions
  1. SD UHS-II
  2. Thunderbolt
  3. SAS 12G
  4. HDMI 2.0
  5. MHL 3.0
  6. MIPI M-PHY

- Keysight Scope Protocol Decode Solutions
  1. HDMI 2.0/1.4 Protocol Decode and Compliance Test
  2. DisplayPort 1.2 Protocol Decode
  3. DisplayPort 1.2 AUX Decode
  4. SD UHS-II Protocol Decode
  5. EMMC5.0
Waveform Bridge

Display Port Compliance Test ADS Simulation Bench
Includes:
- Test Fixture Model
- Worst DP cable Model
- Worst DUT channel Model
- IO Models
Waveform Bridge

Real Waveform Data from PHY Test Chip DUT (not DP system)

Simulate Far-End Eye Pattern on ADS
Waveform Bridge

Feed ADS simulated waveform into Infinium on the scope

Run DP compliance test on the scope by using Simulated waveform

Set Up DP compliance test on the scope
Compliance Test Simulation Flow

IO Model in Compliance Channel
- PCB Channel
- Connector
- Cable
- Test Fixture
- PCB Layout
- PCI Express
- DisplayPort
- USB
- DDR
- MIPI

Simulation Tool
- VNA
- PLTS
- 3D Field Solver
- ADS

Simulated Waveform

Compliance Software
- Agilent
- GRL

GRL Compliance Simulation Automation & GUI Software

User
Total Approach to Testing

Variability

- Compliance Testing
  - Lower bar
  - May not match reality
  - Static snapshot

- Electrical Stress
  - PVT variation
  - Jitter impact
  - Electrical Margin

- Protocol Stress
  - Error handling
  - Random faults
  - Protocol margin

- Application Stress
  - Software interaction
  - O/S interaction
  - Cross interfaces

- Manufacturing Testing
  - Manufacturing variation
  - Production defects
  - QA test tools

- Life Testing
  - Time variation
  - MTBF

- Interop Testing
  - Define target space
  - Virtual & real test bed

19
Thanks

Granite River Labs

Sales and business inquiries
info@graniteriverlabs.com
Main Phone: +886 (2) 2657-2199
+886 (3) 552-6658
HDMI 2.0 and MHL 3.2 Test Environment Guideline

Simplay Labs Taiwan

iST宜特科技

Eric 余天華 / 首席技術顧問

www.hdmiatc-taiwan.com
Testing challenge

Maximum 8~10K times plugs

Module performance decaying

Frequent Environment Calibration

Better Environment arrangement
Major features in HDMI 1.4b

- **Electrical Phy test:**
  Maximum clock rate **340 MHz**
  Maximum Total throughput **10.2Gbit/s (3.4G/channel)**

- **Protocol test:**
  Character synchronize test.
  All video packet test.

- **Pixel coding:**
  RGB 4:4:4, YCbCr 4:4:4 (8-16 bits per component); YCbCr 4:2:2 (12 bits per component)

- **Video timing:**
  Deep color timing.
  3D Video timing (Top-bottom, side by side, frame sequential 1920P at 120Hz ).
  4K2K timing support 4096x2160/30Hz.

- **Audio coding:**
  High-bitrate audio (HBR) sampling up to **768 kHz**
  Maximum Audio channel 8 channel
  One bit Audio.

- **HDCP version :**
  Support HDCP 1.x
Major features in HDMI 2.0

- **Electrical Phy test:**
  - Maximum clock rate **600 MHz**
  - Maximum Total throughput **18Gbit/s. (6G /channel)**

- **Protocol test:**
  - Source Sink TMDS Protocol Scrambling test.
  - Sink Character Error Detection Tests (CED)

- **Pixel coding:**
  - Support 4:2:0 Chroma subsampling.
  - **4:2:0 deep color.**

- **Video timing:**
  - 2160p 24-bit Color Depth, Deep Color, 3D
  - Non-2160p 24-bit Color Depth, Non-2160p 24-bit Color Depth
  - Maximum resolution at 24 bit/px, 4096x2160/60Hz

- **Audio coding:**
  - HBR (high bit rate) Audio sampling up to **1536KHz**
  - Maximum Audio channel **32 channel**

- **HDCP version:**
  - Support HDCP 2.2 and 1.x

- **SCDC A8/A9 support test:**
  - CED (character error detect) support behavior test.
  - SCDC (Status and control data channel) behavior test.
Agilent ParBERT 81250 is a modular parallel electrical and optical bit error ratio (BER) test platform, which works up to 13.5 Gb/s, already provide the test capability for next generation.

- DSAX92004A Agilent Infiniium 20 GHz
- Agilent Technologies N5399C HDMI electrical performance validation and compliance software
Keysight other test equipment in Simplay Labs

HDMI 1.4b Protocol analyzer
U4998A

- E4887A-102 75MHz cable emulator.
- E4887A-103 Eq type cable emulator.
- E4887A-105 270MHz cable emulator.
- E4887A-106 742.5MHz cable emulator 2810mm. HDMI 2.0
Related HDMI 2.0 testing SW

Parbert automation: ValiFrame 5399 V2.23

Scope SW: 5990C

Scope InfiniiSim SW EQ
## HDMI 2.0 Keysight MOI/test items

<table>
<thead>
<tr>
<th>Test ID</th>
<th>items</th>
</tr>
</thead>
<tbody>
<tr>
<td>HF1-1_Agilent_MOI_v1.0a</td>
<td>6G – VL and Vswing</td>
</tr>
<tr>
<td>HF1-2_Agilent_MOI_v1.0a</td>
<td>6G – TRISE, TFALL</td>
</tr>
<tr>
<td>HF1-3_Agilent_MOI_v1.0a</td>
<td>6G – Inter-Pair Skew</td>
</tr>
<tr>
<td>HF1-4_Agilent_MOI_v1.0a</td>
<td>6G – Intra-Pair Skew</td>
</tr>
<tr>
<td>HF1-5_Agilent_MOI_v1.0a</td>
<td>6G – Differential Voltage</td>
</tr>
<tr>
<td>HF1-6_Agilent_MOI_v1.0a</td>
<td>6G – Clock Duty Cycle and Clock Rate</td>
</tr>
<tr>
<td>HF1-7_Agilent_MOI_v1.0a</td>
<td>6G – Clock Jitter</td>
</tr>
<tr>
<td>HF1-8_Agilent_MOI_v1.0a</td>
<td>6G – Data Eye Diagram</td>
</tr>
<tr>
<td>HF1-9_Agilent_MOI_v1.0a</td>
<td>6G – Differential Impedance</td>
</tr>
<tr>
<td>HF2-1_Agilent_MOI_V1.0a</td>
<td>6G – Min/Max Differential Swing Tolerance</td>
</tr>
<tr>
<td>HF2-2_Agilent_MOI_V1.0a</td>
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<td>HF2-4_Agilent_MOI_v1.0a</td>
<td>6G – Differential Impedance</td>
</tr>
<tr>
<td>items</td>
<td>Major equipment</td>
</tr>
<tr>
<td>--------------------------------------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>6G – VL and Vswing</td>
<td>Agilent DSO90000A or DSO-X or DSO-Q series Infinium Oscilloscopes</td>
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</tr>
<tr>
<td>6G – Min/Max Differential Swing Tolerance</td>
<td>Agilent M8190A or E4887A based Test Equipment</td>
</tr>
<tr>
<td>6G – Intra-Pair Skew</td>
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<td>Agilent M8190A or E4887A based Test Equipment</td>
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<tr>
<td>6G – Differential Impedance</td>
<td>E5071C ENA Series Network Analyzer</td>
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## HDMI 2.0 TP and testing SW

<table>
<thead>
<tr>
<th>Items</th>
<th>Test Point</th>
<th>Cable Emulator</th>
<th>SCDC Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>6G – VL and Vswing</td>
<td>TP1</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>6G – TRISE, TFALL</td>
<td>TP1</td>
<td>NA</td>
<td>NA</td>
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<td>NA</td>
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<td>6G – Clock Duty Cycle and Clock Rate</td>
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<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>6G – Clock Jitter</td>
<td>TP2_EQ</td>
<td>NA</td>
<td>NA</td>
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<tr>
<td>6G – Data Eye Diagram</td>
<td>TP2_EQ</td>
<td>NA</td>
<td>NA</td>
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<td>TP1</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>6G – Min/Max Differential Swing Tolerance</td>
<td>TP2</td>
<td>BitifEye BIT-1014-1000-0 HDMI 2.0 Cable emulator</td>
<td>BitifEye BIT-1016-0000-0 HDMI SCDC Controller Kit</td>
</tr>
<tr>
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<td>NA</td>
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</table>

iST proprietary and confidentiality
HDMI test environment setup
Keysight MHL 3.2 test equipment

ParBert
MHL 3.2 Sink Electrical test

High speed scope
MHL 3.2 Source Electrical test

AWG M8190
3.7.2.32 Differential input swing tolerance eCBUS-D BWD
3.7.2.33 Input DC voltage of eCCBUS-S BWD data
3.7.2.36 Jitter tolerance of eCBUS-S BWD Data
Simplay MHL3.2 test equipment

- **UTS 800 – 8 Slot Platform System**

- **SL-850 - UTS 800 MHL-CBUS Test Module**

- **SL-860/861 -UTS 800 MHL2.2 Rx/Tx System Analyzer Test Module**

- **SL-863 -UTS 800 MHL3.2 Rx/Tx System Analyzer Test Module**

- **SL-402 RELT relay board**

- **SL-403 CBUS Source/Sink Board**
New Fixtures for MHL3.2

100-1113-000 SMA to Type A

100-1114-000 SMA to MHL

Artek MHL3.0 cable emulator
MHL 3.2 test environment setup

example 4.7.2.24
Coupon

Expires
6/30/2015

3000 NTD OFF
HDMI or MHL Test

Contact Info.  Eva Tsai  Tel: (03)579-9909 # 8803  Email: eva_tsai@istgroup.com

1. This coupon is only valid for use at Simplay Taiwan lab.
2. This coupon must be presented before or at time of service contracted.
3. One coupon can be used for one project only.
4. This coupon is good for one time use only and cannot be combined with other discount.
5. Coupon has no cash value and is only valid for specific service printed.
6. Coupon must be stamped with official iST’s logo to take effect and cannot be duplicated.
7. Coupon is only valid for customers who submits “service application form” prior to the coupon’s expiration date.
8. iST reserves the right to adjust or void this coupon without further notice. For updated information, please visit www.istgroup.com.
Q & A

Thank You for Attention