Validation of DDR2/3 Designs
Overview

- DDR2 & 3 Design and Validation Challenges
- Probing as key to success
- Physical Layer Validation
- Protocol Layer Validation
- Q&A
DDR3 Key Characteristics

• DQ rates from 800-1600Mb/s (C/A rates from 400-800Mb/s)
• Differential strobes
• Dynamic ODT
• Independent CL for Reads and Writes
• Support for “fly-by” DIMM architecture
DDR2 and DDR3 DIMM Architecture

**DDR2 DIMM Architecture**
- T-branch topology balances the delay to each memory device, but makes reflections hard to manage.

**DDR3 DIMM Architecture**
- Fly-by topology improves C/A signal integrity but the signals from the memory controller arrive at each DRAM at different times.
Impact on Design and Validation

- Clock Speeds reaching 1GHz
- Parallel buses reaching the speeds of serial technology
- Tighter timing margins require calibration and bus training for DRAM, controller, and analyzer capture
- Crosstalk, impedance, EMI, and jitter management
- Noise susceptibility
- Probe load effects are critical

Benefits of good signal integrity

- Guarantees interoperability with different vendors
- Improved performance
- More design margin

“I’m becoming a microwave designer!”
DDDR2/3 Probing Requirements

- Stubs and capacitive loading must be minimized
- Access to all signals for protocol measurements
- Adequate bandwidth for parametric measurements
  - DDR2 – 2 Ghz
  - DDR3 – up to 6Ghz
  - Graphics DRAM may require up to 12.5Ghz!
Probe Impact on DRAM Signals

- DRAM Ball
- Jitter/Noise
- Load Isolation
- Probe Bandwidth
- Instrument
Probe Optimization

Signal Loading

Bandwidth
DDR2/3 Physical Layer Validation
Serial vs. DDR Technology and Signal Integrity

Signal integrity analysis is measured at Tx and Rx points.

Signal integrity is measured at the balls of DRAM where the JEDEC spec is defined upon. Signals of interest are usually:

- **CLK** (for jitter analysis)
- **DQS & DQ** (for signal quality and timing measurement. Read & write has to be separated to analyze signal independently driven from chipset and DRAM)
Probing methods for DDR signals

Probing at the via holes generally gives the best results since you are measuring signals closest to the balls of the DRAM (where the JEDEC spec is defined upon).

In general, probing on the DRAM side of the 22 ohm resistors will also give good results.
Probing from the System

Agilent InfiniiMax probe is flexible enough to probe at hard to reach and tight space.

The DIMM is plugged into the system.

DQS and DQ signals are measured.
You want to be able to easily separate the read-write bits so you can quickly test, debug and resolve signal issues.

DQS and DQ edges are aligned. The signals are driven from the DRAM. The DQS edge is 90-deg phase shifted from the DQ. The signals are driven from the chipset.

High-impedance mode. The voltage is floating.
DDR Signals in Infinite Persistence Mode

Scope triggers on DQS signal with both read and write cycles

DQ read and write cycles overlap each other. You cannot differentiate them.

There is no meaningful electrical measurement or timing relationship you can make between the DQ or DQS signal if they are not separated.
Separation Method #1: Preamble Width Trigger

Isolate write/read cycles

• Trigger on read or write pre-amble width

JEDEC SPEC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>DDR2-400</th>
<th>DDR2-533</th>
<th>Units</th>
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<tr>
<td></td>
<td></td>
<td>min</td>
<td>max</td>
<td>min</td>
</tr>
<tr>
<td>Read preamble</td>
<td>tRPRE</td>
<td>0.9</td>
<td>1.1</td>
<td>0.9</td>
</tr>
<tr>
<td>Write preamble</td>
<td>tWPRE</td>
<td>0.35</td>
<td>x</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Weakness:

• Exact value of write preamble depends on the Chipset or DRAM vendors. User has no control over this.

• Read/Write preamble can have the same width which makes separation impossible

• The write preamble can be similar to the data bit period.
Separation Method #2: Trigger On Amplitude

Trigger on larger strobe amplitude if either the chipset or DRAM is a stronger driver.

**Weakness:**
- The larger signal amplitude is not exclusive to read or write signal. It depends on the chipset or DRAM vendor implementation.
- What if both amplitudes are the same?

By setting the trigger threshold slightly above the smaller signal, you can trigger on READ only.

You cannot analyze the write because READ and WRITE will overlap.

Trigger on higher amplitude
Separation Method #3: Mixed Signal Oscilloscopes (MSO)

Connect the following signal to:

- **CLK** – Ch1
- **CKE** – Ch3
- **/WE** – D0, **/CAS** – D1
- **/RAS** – D2, **CS0** – D3
- **/CS1** – D4, **A10** – D5

**Analog Channels**

**Digital Channels**

**Trigger condition:**
- Read or Write Command Pattern

**Weakness:**

- MSO are **low bandwidth** scopes (<1GHz). They are suitable for lower data rate – DDR200/266.
- The challenge is using a higher bandwidth oscilloscope with limited 4 channels to separate read and write signals.

**MSO is a perfect solution for DDR validation but due to its limited bandwidth, it is only suitable for slower DDR data rate.**
Introducing InfiniiScan “Zone Qualify” mode

- Draw up to 4 zones of any sizes with “Must / Must Not Intersect” settings to track or remove signals.
- Using the zones, the signal can be isolated depending whether the waveform is intersecting or not intersecting the zones.

2 signals triggering at the same time. You can see its distinctive difference.

The distinctive difference you see can be tracked or removed by InfiniiScan “Zone Qualify” mode.
Use InfiniiScan to separate read and write signals

- There is no rule how to use the zones to separate the read or write signals. It depends on the silicon characteristics and DIMM loading which shows distinctive difference between the read and write signals.
Read-Write Separation – Step 1

A “Must Not Intersect” zone is drawn on the DQS waveform to discard the normal bits or idle state signals.

With the “Must Not Intersect” zone drawn, the scope consistently tracks the preamble bits of the read and write signals.

DQ signal is tracked at the beginning of the read or write burst, but no separated yet.
Read-Write Separation – Step 2

Read and write separation made easy with InfiniiScan. If you can see it, you can track it.
DDR2 Compliance with Agilent N5413A tool

Test Coverage:

Compliance Mode (based on JEDEC spec)
- Clock Jitter Tests
- Electrical Tests
- Timing Tests (Available soon)

Advanced Debug Mode
- Eye Diagram Analysis
- Mask Test
- Ringing Test

You can now use this DDR2 tool to characterize and validate your DDR2 signals without the hassle of making the measurement on your own.
Setting up the tool for measurements

Configure the scope and test setup.

Allow user to select which tests to be run.

Shows where the probes should be connected to the DDR device and scope.
Automated measurement, results and HTML report

The tool provides automated measurements.

A summary of the test results are displayed along with the margin analysis.

The tool auto-generates a HTML report with snapshots of the critical waveforms.
DDR2/3 Protocol Validation
Analyzer System Considerations

• High performance probing
  • System and embedded memory
  • Low load and high bandwidth

• Reliable data capture
  • Sampling close to center of small eye is crucial
  • Training essential to cover all system timing cases and enable functional validation in real systems

• Analysis of captured data
Memory Bus Probing Options

Direct Attach Probing
- Highest speed (to DDR3/1600), lowest loading
- Supports System and embedded designs
- Requires design-in of footprint

Jedec System Memory Probes
- Plugs into Jedec standard connector
- Slot extender and Validation DIMMs

Via, Pin, and BGA Probing
- Solder down attachment
- Low loading
- High Bandwidth
Traditional Analyzer Sample Calibration

Oversampled Capture

Analyzer Bit Error Rate explodes as sample rate -> tValid/3
Capture Calibration for Lowest BER

- Synchronous sampling uses same technique as controllers and DRAMs themselves
- Fine grained sampler positioning locates true center of eye
System and DIMM Architecture Timing Variance

Fly-by induced Skew (~1.25ns)

Cascade shift due to bus flight time
Protocol Aware Sampling

Fly-by induced Skew sets DQ Sample position

Identify system timing case from DRAM protocol

Only one analyzer channel required per data signal
Validation Tasks

**DRAM Validation**
- Write data
- Read data
- Cmd/Addr/Data post-reg timing
- Clock drive
- Frame $\Rightarrow$ DRAM cmd latency

**System Validation**
- Channel validation
- Channel Traffic trace
- Event Trigger
- Cross bus trigger
- System trace (multi-bus time correlated, multi/cross bus trigger)
State Analysis
Timing Analysis
Summary

• DDR2 and DDR3 speeds and architecture are driving new design and measurement technologies

• Superior signal integrity and probing technology is required for the most accurate DDR2/3 validation

• Validation that would have otherwise been very difficult are made easy thru addition of new instrument capabilities
  • Powerful triggering and signal processing
  • Automated testing of compliance thru SW applications
  • Protocol aware calibration and data capture
For Additional Information

Agilent’s DDR technology webpage:

www.agilent.com/find/ddr

N5413A DDR2 Compliance App Product Info:

www.agilent.com/find/n5413a

A Time-Saving Method for Analyzing Signal Integrity for DDR Buses Application Note:

http://www.techonline.com/learning/techpaper/199701791

InfiniiScan Product Info

www.agilent.com/find/InfiniiScan

Memory Solution with Logic analyzer:

http://www.home.agilent.com/USeng/nav/-536902586.0/pc.html