Closing the loop part 1: Why use simulation tools for high speed signal channel design?

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Application Engineer
Agilent EEsof EDA
High Speed Digital Design Flow

Pre-Layout w/Channel Sim
Analyze & Optimize

Pre-Layout w/Transient
Verify & Refine

Post-Layout
Assess Critical Nets & PDNs

Post-Layout
EM Models to Verify & Refine

Constraint Mgmt.
Design Rules to Constraint Editor

Layout
Constraint-Based Board Tool Layout

Physical Design
Pre-Layout HSD-Tools and Design Guides

- Accurate calculation of Zeven, Zodd, Zdiff and Zcom

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>70.00 μm</td>
<td>128.9</td>
<td>64.46</td>
<td>53.83</td>
<td>107.7</td>
</tr>
<tr>
<td>80.00 μm</td>
<td>123.9</td>
<td>61.94</td>
<td>51.25</td>
<td>102.5</td>
</tr>
<tr>
<td>90.00 μm</td>
<td>119.4</td>
<td>59.69</td>
<td>48.94</td>
<td>97.68</td>
</tr>
<tr>
<td>100.0 μm</td>
<td>114.4</td>
<td>57.22</td>
<td>46.72</td>
<td>93.44</td>
</tr>
<tr>
<td>110.0 μm</td>
<td>110.9</td>
<td>55.46</td>
<td>44.85</td>
<td>89.70</td>
</tr>
<tr>
<td>120.0 μm</td>
<td>107.7</td>
<td>53.86</td>
<td>43.14</td>
<td>86.29</td>
</tr>
<tr>
<td>130.0 μm</td>
<td>104.7</td>
<td>52.37</td>
<td>41.57</td>
<td>83.15</td>
</tr>
<tr>
<td>140.0 μm</td>
<td>102.0</td>
<td>50.99</td>
<td>40.12</td>
<td>80.25</td>
</tr>
<tr>
<td>150.0 μm</td>
<td>99.41</td>
<td>49.71</td>
<td>38.78</td>
<td>77.55</td>
</tr>
</tbody>
</table>

- Uses Method of Moment and FEM
  - Zdiff with solder mask
- TDR and Mixed Mode Analyzer
- Crosstalk
Impedance, TDR and Mixed Mode Analyzer

Runs Transient and S-Parameter Simulation

Microstripline Model MLSUBSTRATE2 (infinite GND)

DUT - Replace this circuit with your own circuit

Marker sv1

Mixed Mode Display

Agilent Technologies
**Balanced Topologies**

- Ideal balanced devices
  - Lower voltage requirements
  - Noise and EMI immunity

- Non-ideal devices are not symmetric
  - Can be identified by signal-conversions
    - Differential $\rightarrow$ Common
    - Common $\rightarrow$ Differential

- Mixed-Mode analysis tools are needed

![Balanced Structure Diagram](image1)

- **Balanced Structure**

![UnBalanced Structure Diagram](image2)

- **UnBalanced Structure**
Unbalanced Structures

- Undesirable signal conversions cause emission or susceptibility problems

**Differential-stimulus to common-response conversion**

- Imperfectly matched lines mean the electromagnetic fields of the signals are not as well confined as they should be – giving rise to generation of interference to neighboring circuits.

**Common-stimulus to differential-response conversion**

- Imperfectly matched lines mean that interfering signals do not cancel out completely when subtraction occurs at the receiver. Measured by stimulating common-signal to simulate interference.
Single-ended to Mixed-Mode $S$-Parameters

- **$S_{SE}$**
  - **Response**
  - **Stimulus**
    - $S_{11}$
    - $S_{12}$
    - $S_{13}$
    - $S_{14}$
    - $S_{21}$
    - $S_{22}$
    - $S_{23}$
    - $S_{24}$
    - $S_{31}$
    - $S_{32}$
    - $S_{33}$
    - $S_{34}$
    - $S_{41}$
    - $S_{42}$
    - $S_{43}$
    - $S_{44}$

- **$S_{MM}$**
  - **Port 1**
  - **Port 2**
  - **Differential Response**
    - $S_{DD11}$
    - $S_{DD12}$
    - $S_{DD21}$
    - $S_{DD22}$
  - **Common Response**
    - $S_{CD11}$
    - $S_{CD12}$
    - $S_{CD21}$
    - $S_{CD22}$
  - **Common Stimulus**
    - $S_{CC11}$
    - $S_{CC12}$
    - $S_{CC21}$
    - $S_{CC22}$

- **Naming Convention:**
  - $S_{mode$ meas., mode stim., port meas., port stim.
Pre-Layout Channel Modeling
Flexible Representation of Interconnect

- S-Parameters
- Built-in Multilayer Interconnect library
- Physical models from Momentum
- Physical models from FEM/FDTD
- Measurement based
- Lumped representation (Broadband SPICE)
- W-element (HSpice compatible)
Channel Simulator Methodology

Step response calculated using short SPICE-like transient simulation

Bit by bit mode: Superposition of bits

Statistical mode: Statistical techniques

No need to run millions of bits through SPICE-like simulation
Design Exploration with ADS Channel Simulator
Channel Simulation
Channel Simulation

88.7 Ohm

Mixed Mode S-Parameter

Channel Simulation

88.7 Ohm

Mixed Mode S-Parameter
Optimization of the Channel traces (w,s) and De-Emphasis

Improvement factor of:

<table>
<thead>
<tr>
<th>Eye Height</th>
<th>Jrms</th>
<th>Jpp</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Before Optimization</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>192</td>
<td>10.5psec</td>
<td>40.8psec</td>
</tr>
<tr>
<td><strong>Optimization of deemphasis and Traces</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>3.182psec</td>
<td>15.91psec</td>
</tr>
<tr>
<td><strong>Opt. Deemph. Traces and Matching</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>290</td>
<td>2.66psec</td>
<td>11.6psec</td>
</tr>
</tbody>
</table>
Channel Statistical and Crosstalk Analysis
Rx Equalization

Support three type of equalizations
- Continuous-time linear equalizer (CTLE): pole-zero
- Feed-forward equalizer (FFE)
- Decision-feedback equalizer (DFE)

Optimize the initial taps automatically
Adapt taps with LMS, RLS or ZF algorithm during the simulation
Save the optimized taps on file
Equalization Rx (FFE, DFE) Results

With Equalization

Without Equalization  With Equalization

<table>
<thead>
<tr>
<th>measurement</th>
<th>ff_Probe1 Summary</th>
<th>measurement</th>
<th>e_Probe1 Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level1</td>
<td>0.049</td>
<td>Level1</td>
<td>0.149</td>
</tr>
<tr>
<td>Level0</td>
<td>-0.029</td>
<td>Level0</td>
<td>-0.154</td>
</tr>
<tr>
<td>LevelMean</td>
<td>0.010</td>
<td>LevelMean</td>
<td>-0.002</td>
</tr>
<tr>
<td>Amplitude</td>
<td>0.079</td>
<td>Amplitude</td>
<td>0.303</td>
</tr>
<tr>
<td>Height</td>
<td>0.000</td>
<td>Height</td>
<td>0.229</td>
</tr>
<tr>
<td>HeightDB</td>
<td>0.000</td>
<td>HeightDB</td>
<td>-0.402</td>
</tr>
<tr>
<td>Width</td>
<td>3.50E-12</td>
<td>Width</td>
<td>8.37E-11</td>
</tr>
<tr>
<td>SNR</td>
<td>1.540</td>
<td>SNR</td>
<td>12.186</td>
</tr>
<tr>
<td>RiseTime</td>
<td>5.99E-11</td>
<td>RiseTime</td>
<td>5.71E-11</td>
</tr>
<tr>
<td>FallTime</td>
<td>1.250E-10</td>
<td>FallTime</td>
<td>5.68E-11</td>
</tr>
<tr>
<td>JitterPP</td>
<td>3.27E-11</td>
<td>JitterPP</td>
<td>4.125E-11</td>
</tr>
<tr>
<td>JitterRMS</td>
<td>0.000</td>
<td>JitterRMS</td>
<td>9.234E-12</td>
</tr>
<tr>
<td>WidthABER</td>
<td>-0.045</td>
<td>WidthABER</td>
<td>8.56E-11</td>
</tr>
<tr>
<td>HeightABER</td>
<td>0.000</td>
<td>HeightABER</td>
<td>0.286</td>
</tr>
<tr>
<td>CrossingLevel</td>
<td>0.005</td>
<td>CrossingLevel</td>
<td>-0.008</td>
</tr>
</tbody>
</table>
DDR Compliance Toolkit – Signal Name Assignment, Measurements, and Compliance Testing

Standard Compliance Testing and Margin Analysis
- Perform compliance test and margin analysis
- Start time: 3.0

Note: Compliance test limits are specified in an XML file located in the source/constraints directory of the design kit.
DDR Channel Simulation
Compliance report shows various compliance limits, timing and electrical violations
Excel sheet shows the summary of compliance measurements
High Speed Digital Design Flow

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Post-Layout
Assess Critical
Nets & PDNs

Post-Layout
EM Models to
Verify & Refine

Constraint Mgmt.
Design Rules to
Constraint Editor

Layout
Constraint-Based
Board Tool Layout

Physical Design
Post Layout Verification
CAD Integration with ADS

Cadence, Mentor, Zuken, Altium, …

Cadence Allegro PCB Link
ODB++ export -> Expedition, Altium

Advanced Design System design and simulation environment
EM Simulation

Choice of 3 EM technologies to best fit specific need:

- Momentum (Method of Moments) 3D Planar
- FEM (Finite Element Method) Full 3D
- FDTD (Finite Difference Time Domain) Full 3D
Complete Channel Verification

Built-in transistor models
HSPICE netlist
Spectre netlists
Verilog-A
C/C++
IBIS/IBIS-AMI

Add in Card

Package Model

• Bit-by-Bit or Statistical Simulation
• Crosstalk Analysis
IBIS-AMI (Algorithmic Modeling Interface) Models

- IBIS is a fast, industry-standard (ANSI/EIA-656B) model of a chip I/O electrical behavior
- IBIS 4.2 and below can only model analog I/O
- IBIS 5.0, adds AMI extension to model equalizers, clock/data recovery that are used by most multi-GB serial links
- ADS supports IBIS 5.0 models

- **New! IBIS 5.0 includes AMI**
- **New! IBIS 5.0 includes AMI**
- Lumped and distributed passive components (part of EDA tool: not part of IBIS)
IBIS-AMI model extraction solution using Agilent SystemVue

AMI Rx (Blind FFE, Blind DFE, CDR)
Assume NRZ
Power Integrity

1. Keep supply voltages arriving on chip within narrow range (typ. 5% “ripple”)
2. Keep synchronous switching noise (SSN) within spec
3. Meet EMC/EMI spec
Pwr/Gnd Return Current

The path of the return current will add additional inductance called loop inductance.

Large loop inductance will degrade signal quality and timing performance.

Complex Network → Model with EM Simulation
Bypass De-Coupling Capacitor

- Isolate power supply and IC against high frequency noise signals (bypass power supply noise)
- It acts as a charge reservoir and provides instantaneous current to fast switching devices when VRM is not able to deliver current fast enough to switching devices
- The de-coupling capacitor gets discharged when current is sunk by the switching transistor
- The de-coupling capacitor needs to charge back again when in order to supply current at the next switching cycle
De-Coupling Capacitor: Where and Why?

- Speed of signal in PCB is ~166ps/inch.
- Farther the de-coupling capacitor from the switching device, longer it will take to respond to current requirements
- Response time of ~1 nsec
- De-coupling capacitor has an effective operating radius (distance), outside which it cannot reduce power supply noise or provide instantaneous current to switching devices.
- Multiple de-coupling capacitors therefore are required to cover different switching devices on the board.
By-pass De-Coupling Capacitors in the Real-World Are Not Ideal Capacitors

- Intrinsic parasitics from the construction of the cap itself
- Extrinsic: There is added loop inductance due to mounting. The current must travel through planes and pwr/gnd vias

ESR : Equivalent Series Resistance
ESL : Equivalent Series Inductance

\( R = \text{ESR Ohm} \)
\( L = \text{ESL nH} \)
\( C = \text{C pF} \)

\( \text{ESR} \) vs. \( \text{freq} \)
\( \text{ESL} \) vs. \( \text{freq} \)
\( C \) vs. \( \text{freq} \)
Signal and Power Integrity Simulation (SIPI) Wizard

Guided EM simulation setup
Enables net based selection and simulation
Allows Port grouping/clustering
Computes PDN impedance
Provide current distribution with SMD components
SI/PI Analyzer Flow

SI/PI > Setup Wizard

EM Model Generation

SI/PI > Analyzer

Circuit Simulation

Net driven EM simulation setup...

Auto-generation of typical SI/PI analysis schematics

Current visualization including effect of SMDs
View Current Distribution
EMI Analysis

Observe hot-spot area closely, and identify root-cause

**Root-cause:**
There is small $\lambda/8$ power-plane patch that is radiating like patch-antenna

Use the Momentum-$\mu$wave EM-engine with Antenna-Gain parameter to measure the merit of the PCB as non-intended antenna

Develop EMI guidelines along with SI/PI Guidelines using Antenna-Gain Parameter to compare Layout guidelines
Simulation and Measurements

Measurements help simulation:

1. Measurement contributes measurement-based models to end-to-end simulations
2. Measurement verifies the base line simulation at conveniently probe-able and/or connectorized points

Simulation returns the favor in three ways:

1. **De-embedding**: Determine what the measurement would have been at difficult-to-reach points by use of an EM-based model
2. **Insight** through visualization: “See” invisible EM fields in full 3D. Think “electromagnetically”
3. **Virtual prototyping**: “What if…?” design space exploration by modifying the base line simulation models
De-embedding

2) See what the waveform would have looked like if you could get a probe in here.

1) Measure Here

Die → Bonding wire/pins → Pc transmission line → Standard connector → Cable → Standard connector → Pc transmission line → Bonding wire/pins → Die

Starts in here

Transmitter

Ends in here

Receiver

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Combine Measurement Instruments and Measurement Algorithms with Simulation

- Jitter decomposition algorithm (Agilent EZJit Plus)
- Eye diagram analysis tool (Agilent FlexDCA)
- DDR2 and DDR3 Compliance DesignKits
- Transformation of frequency-domain models into causal time-domain-models
  - Patented convolution with Kramers-Kronig causality and (optionally) passivity enforcement
- Interpolation and extrapolation of s-parameter data in Touchstone files
  - DC to 50 MHz info is often missing from VNA data
  - Frequency steps in the file often mismatched with steps in the sim
  - VNA data is band limited (typically 20 GHz or 50 GHz)
Broad HSD Application Support: ADS DesignGuides, DesignKits and Examples

PCI Express and de-embedding examples

USB3

DDR (DDR2, LPDDR2 and DDR3 Compliance DesignKits)

HDMI, 10Gigabit Ethernet, UHS-II

Differential and Single Ended (Coplanar) Impedance Calculation Design Guide
Summary

• Modern EDA tools make it easy to build accurate models from geometry and electromagnetic simulation

• When used with modern test equipment, these models let you:
  – Probe in a convenient place and then move the measurement plane
  – Explore the design space by varying a simulated “virtual geometry”

• Validate baseline simulations against actual measurements on a physical board