Agenda

» DisplayPort Introduction and Status Update

» Technical Overview
Introduction to DisplayPort

- DisplayPort is an open, digital display interface standard targeted at a broad range of applications.

- DisplayPort is a replacement to DVI, LVDS and VGA standards and unifies connectivity to External and Internal displays.

- Scalable, micro-packet architecture and robust 2-way communications for enabling new, enhanced features in Displays.

- DisplayPort provides a secure interconnect for Audio & Video.
# Comparison of Display Standards

<table>
<thead>
<tr>
<th></th>
<th>DisplayPort*</th>
<th>LVDS</th>
<th>DVI</th>
<th>VGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog support</td>
<td>None</td>
<td>None</td>
<td>Optional (DVI-I)</td>
<td>RGB</td>
</tr>
<tr>
<td>No. of data &amp; clock pairs</td>
<td>1 to 4 data pairs, no separate clock pairs</td>
<td>8 pairs - dual channel 2 clock pair – dual channel</td>
<td>3 or 6 data (two versions of same connector) 1 clock pair</td>
<td>3 pair for RGB H sync; V sync lines</td>
</tr>
<tr>
<td>Bit rate, per pair</td>
<td>1.62 or 2.7 Gbit/sec (fixed clock rate) Future extensible</td>
<td>945Mbit/sec (135Mhz clock)</td>
<td>Max. 1.65 Gbit/sec. (10x pixel clock, fixed at 165Mhz)</td>
<td>Depends on DAC speed</td>
</tr>
<tr>
<td>Total raw capacity</td>
<td>1.6 to 10.8 Gbit/sec</td>
<td>7.56Gbit/sec</td>
<td>4.95 (single link) to 9.9 (dual) Gbit/sec.</td>
<td>Depends on DAC speed</td>
</tr>
<tr>
<td>Clock</td>
<td>Embedded</td>
<td>Separate pair</td>
<td>Separate pair</td>
<td>Separate lines</td>
</tr>
<tr>
<td>Audio support</td>
<td>Full support</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Aux. channels</td>
<td>1Mbps AUX CH; extensible</td>
<td>None</td>
<td>DDC</td>
<td>DDC</td>
</tr>
<tr>
<td>Channel Coding</td>
<td>ANSI8B/10B</td>
<td>None</td>
<td>TMDS</td>
<td>None</td>
</tr>
<tr>
<td>Content protection</td>
<td>HDCP optional</td>
<td>None</td>
<td>HDCP optional</td>
<td>None</td>
</tr>
<tr>
<td>Protocol</td>
<td>Micro-Packet-based; extensible in future to add features.</td>
<td>Sequential data stream</td>
<td>Serial data stream at 10x pixel clock rate</td>
<td>Analog signal</td>
</tr>
<tr>
<td>Internal (notebook) use</td>
<td>Included in first release of spec.</td>
<td>De-facto notebook panel standard</td>
<td>None; no TMDS-based standards</td>
<td>None</td>
</tr>
<tr>
<td>Controlling authority</td>
<td>VESA</td>
<td>ANSI</td>
<td>Digital Display Working Group</td>
<td>IBM; VESA defines video modes and DDC</td>
</tr>
</tbody>
</table>
DisplayPort V1.1 Technology

- Scalable: 1, 2, or 4 lanes, for up to 10.8Gbps bandwidth
  - WQXGA, 30-bit color LCDs can be supported over one link
- Secure: HDCP 1.3 Content Protection
- AUX CH for 2-way communication
- AC-Coupled Interface
- Low Power
- Low EMI

<table>
<thead>
<tr>
<th>Lane Width</th>
<th>1.6 GHz</th>
<th>2.7GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-Lane</td>
<td>1080p-30bit</td>
<td>WQXGA-30bit</td>
</tr>
<tr>
<td>2-Lane</td>
<td>1080i, SXGA</td>
<td>WUXGA</td>
</tr>
<tr>
<td>1-Lane</td>
<td>XGA, SDTV</td>
<td>SXGA, 1080i</td>
</tr>
</tbody>
</table>
DisplayPort Benefits

**Reduced Complexity**
Direct drive architecture reduces cost of LCD displays, accelerating CRT transition

**Scalable High Performance**
Scalable 1-4 display lanes with embedded clocking deliver 2x the performance of DVI over smaller connector with reduced EMI

**Fewer Wires**
Fewer wires needed simplifies platform support for emerging applications

• 8 wires (DP) vs. 20 wires (LVDS) for WUXGA (1920x1200)

**New Features**
DisplayPort Benefits: Direct-Drive Monitors

Conventional Display Architecture

Desktop PC Graphics
- Northbridge
  - PLL
  - PCI-E
  - Graphics PLL
  - RAMDAC

Desktop Monitor
- ADC
- DVI/HDMI Rx
- Scaling
- OSD
- MCU
- LVDS Tx

VGA

DisplayPort Architecture

Desktop PC Graphics
- Northbridge
  - PLL
  - PCI-E

DisplayPort

Direct-Drive Monitor
- TCON

OSD and Scaling by PC
DisplayPort Benefits: Notebooks

GPU w/ LVDS Tx
Notebook PC Motherboard

- LVDS Panel
  - LVDS 20+ Wires

GPU w/ Display Port Tx
Notebook PC Motherboard

- DisplayPort Panel
  - DisplayPort 8 Wires
DisplayPort shows significant RFI advantages over TMDS

Simulation of Encoding, Clock Peak Spectra shows up to 30dB Advantage for DP over HDMI
DisplayPort EMI Performance

» Reduced Design Complexity
  » PCI-E compatible PHY layer
  » Unified signaling method for internal and external connectivity
  » Significant EMI reduction simplifies system design

Setup: PC, monitor with DP interface, video timing 1600x1200 -60Hz
Graphs: Horizontal Antenna; Vertical Antenna
Note: Failure points 1,2,3,4 - LVDS harmonics
Failure point 5 – GPU memory clock

Results achieved even without enabling DP spread spectrum clocking!
DisplayPort Market Momentum

» OEMs
  » DisplayPort is endorsed by Dell, HP, Lenovo

» Graphics IC Vendors
  » Intel announced DisplayPort support for external and internal displays for its 2008 Mobile and Desktop Chipsets [IDF San Francisco, September 2007]
  » AMD announced integrated DisplayPort Transmitters in its 2008 Radeon GPUs [August 2007]

» LCD Panel Vendors
  » Samsung announced 30” WQXGA DisplayPort LCD panel [June 2007]

» Ecosystem
  » Many vendors developing repeater, converter, switch, level shifter, receiver and transmitter ICs, cables and connectors
PHY and Link Layer Compliance Test Specification (CTS) documents officially adopted at VESA on 12-Sep-2007

DisplayPort-HDCP CTS published by Intel on 11-Sep-2007

Compliance Test Program kicks-off by early Nov 2007
  » Compliant products will be eligible to receive the DisplayPort logo
DisplayPort Deployment for PC Market

- **End Equipment**
  - Monitor with DP (High-end MFM) (Direct Drive Monitor)
  - PC with DP (High-end Desktop) (Notebook, Entry Desktop)
  - Panel with DP

- **Components**
  - Level shifters/converters
  - PC Graphics with integrated DPTX (Samples) (Production)
  - TCON with integrated DPRX (Samples) (Production)
  - Discrete DP1.0 TX/RX (Samples)
  - Discrete DP1.1 TX/RX (Samples) (Production)

- **Co-simulation**
- **Co-validation**

- **Standards/Interoperability**
  - HDCP1.3
  - VESA Workshop
  - DP V1.1 Adoption
  - Interop Guideline
  - CTS for PHY/Link
  - Compliance Program
  - Pilot Plugfest
  - Plugfest

- **Compliance Program**

- **Timeline**

- **Samples** (Notebook, Entry Desktop)
- **Production** (High-end Desktop, Direct Drive Monitor)
Summary

» DisplayPort is an open, scalable, secure, extensible, digital display standard providing a comprehensive solution for external and embedded display connectivity

» DisplayPort supports higher bandwidth at lower power and EMI than existing legacy standards

» DisplayPort reduces system, display, and cable complexity

» DisplayPort enables cool display designs

» VESA is leading interoperability and compliance to ensure ease of use for consumers
DisplayPort Technical Overview
Consists of AC-coupled, doubly terminated differential pairs (lanes)
  
  » AC-coupled to facilitate semiconductor process migration
  » 0.35 um to 0.045um (and finer)

Link rate: Either 2.7Gbps or 1.62Gbps per lane

» De-coupled from Pixel Rate
» Depends on required application bandwidth, Tx/Rx capability, and channel quality
Structure of Main Link

» Number of lanes: 1, 2, or 4 lanes
  » De-coupled from Pixel Bit Depth
    » Supports 6, 8, 10, 12, and 16 bpc (bits per component), in RGB, YCbCr444/422 colorimetry formats in Ver.1.1
    » Easily extended to any required bit depth or colorimetry
  » All lanes carry data (ANSI8B/10B, clock extracted from data)

» Lane count requirement
  » Source and Sink Devices allowed to support minimum number of lanes required for their needs
  » External cable-connector assembly required to support 4 lanes
Structure of AUX CH

» Half-duplex, bi-directional channel over AC-coupled, differential pair
  » Self-clocked data signal (Manchester II channel coding)
    » AUX SYNC pattern precedes each transaction
  » Source = Master, Sink = Slave
    » Sink may send IRQ (Interrupt Request) via HPD line to prompt AUX CH transaction

» Consistent bit rate over various cable lengths
  » 1Mbits/sec

» Minimal latency
  » Maximum transaction period < 500 µs
    » Sink Device must reply within 300 µs (Reply Timeout Period)
  » Burst data size equal to or fewer than 16 Bytes
  » Prevents one AUX CH application from starving others
Layered and Modular Architecture

**Source Device**

- **Stream Source(s)**
  - Stream Policy Maker
  - Link Policy Maker
  - EDID/MCCS/
  - Link Discovery/Init/Maintenance
  - Isochronous Transport Services
  - AUX CH Device Services
  - AUX CH Link Services

**PHY Layer**

- Main Link
- AUX CH
- HPD

**Link Discovery/Init/Maintenance**

**Sink Device**

- **DPCD**
  - Link Policy Maker
  - EDID
  - Link Discovery/Init/Maintenance
  - EDID/MCCS/
  - Isochronous Transport Services
  - AUX CH Link Services
  - AUX CH Device Services

**Isochronous Transport Services**

**Link Layer**

**Hot-Plug Detect signal**

**Command/Data**

**<-Status/Data**

**Serialized/Encoded**
Recent Milestones

DPCD (DisplayPort Configuration Data)

» Required on DisplayPort Devices with Sink Function

» Used for:
  » Link capability
  » Link configuration
  » Link/Sink status
  » Sink control

» Mapped to 20-bit DisplayPort address space
  » Accessed via native AUX CH transactions

» No overlap with EDID
  » EDID describes the Sink capability
Link Layer

» Isochronous Transport Services
   » Maps stream data into Main Link lanes

» Link and Device Services
   » Link management
   » Device control
<table>
<thead>
<tr>
<th>Number of Lanes</th>
<th>Pixel Steering ((N&gt;=0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Pixel 4N to Lane 0</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+1 to Lane 1</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+2 to Lane 2</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+3 to Lane 3</td>
</tr>
<tr>
<td>2</td>
<td>Pixel 2N to Lane 0</td>
</tr>
<tr>
<td></td>
<td>Pixel 2N+1 to Lane 1</td>
</tr>
<tr>
<td>1</td>
<td>All pixels to Lane 0</td>
</tr>
</tbody>
</table>
Data Packing

» Data Packing and Symbol Stuffing
» Packed into Micro-Packet
  » “Transfer Unit”, 32 ~ 64 symbols long per lane
» Ratio of Valid Data to Stuffing Data function of ratio between packed data stream rate and link rate
» Terminated at the end of the active horizontal video period
  » Marked by BS insertion on all lanes
» Establishes the link upon Hot Plug Detection (HPD)
   » Source Device reads DPCD of DisplayPort receiver in Sink Device via AUX CH
   » Link configured through Link Training
      » Proper number of lanes enabled at proper link rate via AUX CH write
      » Proper voltage swing and equalization level set via Link Training procedure
   » Link status monitored
      » Sink Device notifies Source Device of link status change via IRQ_HPD pulse
      » “Close-loop” operation enhances the robustness and interoperability
Two phases
- Phase 1: Repetition of D10.2 for link clock recovery
- Phase 2: 10-symbol sequence including K28.5’s for EQ adjustment, symbol boundary detection, and inter-lane alignment

Full Link Training
- Link Training performed with AUX CH handshake between Source and Sink Devices
- Required on all Box-to-Box DisplayPort connection

Fast Link Training (Optional)
- Link Training performed without AUX CH handshake
- Uses the last-known good link setting
- Support indicated in DPCD
- For Box-to-Box DisplayPort connection, the very first Link Training must be Full Link Training
Device Services

» EDID for Sink Device capability
» MCCS support for Sink Device control (Optional)
» DPCD for Sink Device power state control
  » Source Device sets Sink Device power state via AUX CH write to
    DPCD address 600h
  » D0 and D3

» Other controls
  » Both Source-to-Sink and Sink-to-Source (Sink Event Notification)
    » Used for compliance test automation
    » Vendor-specific control
PHY Layer

» Logical sub-block
  » Scrambling/de-scrambling of data for Main Link
  » Inter-lane skew insertion/removal
    » 2 Link Symbols of skew between adjacent lanes
  » Encoding/Decoding
    » ANSI8B/10B for Main Link
    » Manchester II for AUX CH

» Electrical sub-block
  » SERDES (Serialization/De-serialization)
  » Differential current driving/receiving
  » Pre-emphasis/equalization for Main Link
  » Link CDR (Clock-to-Data Recovery) by DisplayPort Receiver in Sink Device
20-pin connector
- Symmetrical between Source and Sink
- Compact
  - Four connectors fit in PCI-e card bracket
  - Fits in the back of ultra-slim notebook PC

DP_PWR output pin
- Both on Source and Sink
- DP_PWR wires absent from standard cable-connector assembly

Optional latch
- Prevents “cable fall-off”
» **DP_PWR output**

  » Required for a Box-to-Box receptacle connector (pin 20)
    » Both on Source and Sink Devices
    » 1.5W minimum
  » Optional on a plug connector tethered to Sink Device

» **DP_PWR wire**

  » Allowed only for custom cable-connector assembly
    » Tethered to DisplayPort Device
    » Has a custom plug connector on one end
  » Standard DisplayPort cable connector assembly must not have DP_PWR wire
Thank you!
# DisplayPort & HDMI

## HDMI

- **Raster Scan**
  - Digital CRT like
  - Single pixel stream only
  - Audio in blanking interval

- **HDTV interface**
- **External display connectivity**
- **Two way transmission with CEC**
- **Supports audio and HDCP**
- **CRT like with separate RGB and clock lines**
- **Replaces S-Video**

## DisplayPort

- **Micro-packet**
  - Pixel & audio data in packets
  - Two way communications
  - Device addressing possible

- **Display Interface... all display timings & usages**
- **Internal & external display connectivity**
- **Two way transmission via Aux Channel**
- **Supports audio and Aux Channel**
- **Scalable lanes 1-4; embedded clock reduces EMI**
- **Replaces VGA, LVDS, DVI**

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*limited to 100kbps*  
*extensible well beyond 1Mbps*