SuperSpeed USB 3.0 Technology Overview and Industry Update

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Agenda

• USB Overview
• Synchronizing traces from protocol to electrical
• Transmitter testing
• Receiver testing
• Agilent solutions

• Demo
Worldwide shipment of USB-enabled Devices

USB installed base is 10+ billion units and growing at 3+ billion units a year

Source: In-Stat, May 2011
SuperSpeed USB Timeline

**Product Development**

- **USB 3.0 Electrical Compliance Test Specification**
- 0.9RC

**Initial Deployment**

- SSIC spec Work started

**Broad Deployment**

- 1.0 Test Spec – Pending ECN updates

**Compliance Program/Industry Enabling Development**

- 2011
- 2012
# What is different for USB 3.0

## USB 2.0 High-Speed
- 480Mbps
- NRZI, Half Duplex
- 4 signals (Dp, Dm, VCC, GND)
- Cable $L_{\text{max}}= 5\text{ meter}$
- $I_{\text{configLP/FP}} = 100\text{mA}/500\text{mA}$
- $I_{\text{suspend}} = 500\text{uA}$
- No SSC
- TX SQ at Near End
- No Host RX testing

## USB 3.0 SuperSpeed
- 5 Gbps
- 8B/10B PRBS, Full Simplex
- 8 signals (4 USB2, 4 SS Signals)
- Cable $L_{\text{max}}= 3\text{ meters}$
- $I_{\text{configLP/FP}} = 150\text{mA}/900\text{mA}$
- $I_{\text{suspend}} = 2.5\text{mA}$
- SSC
- TX at End of Channel (Far end)
- RX Jitter tolerance

![Diagram](attachment:diagram.png)
Analyzing USB 2.0 and 3.0 Mass Storage traffic

Requires simultaneous capture of simultaneous USB 2.0 and 3.0 traffic to diagnose fallback issues.

USB 3.0 cables are two completely independent cables in one shielded shell.

The USB analyzer can capture all traffic from device communication.
Synchronizing the USB analysis traces from Protocol to Electrical
Agilent USB 3.0/2.0 Protocol Analyzer & Jammer

- Find & Fix the most complex problems
  - Most advanced triggering on the market
  - Deepest trace buffers on the market by far
  - The only USB Jammer on the market!

- See your DUT, not the instrument
  - Auto-detect instruments on LAN
  - Quick first-screen display
  - Fastest processing of “whole trace,” too
    - E.g. histogram view of 18GB trace in 16 seconds
  - Clean, intuitive GUI, with multiple viewing options to ease migration
    - Drill down into packet details, with “data sheet” graphical views of bit fields, etc.

**KEY SPECS**

<table>
<thead>
<tr>
<th>Simul. USB 3.0 &amp; 2.0 capture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Up to 18GB trace buffer</td>
</tr>
<tr>
<td>4 sequencers, 16 states each</td>
</tr>
<tr>
<td>- 4 timers, 4 counters</td>
</tr>
<tr>
<td>Host I/F: GbE, PCIe X4</td>
</tr>
<tr>
<td>Cascadable with SAS/SATA</td>
</tr>
<tr>
<td>Configurable from $7k - $31k</td>
</tr>
</tbody>
</table>
Flexible Trace Views, from High-Level to Detailed

- **Transaction view**
- **Packet Detail view**
- **Histogram view**
Histograms are processed in under 1s/GB, allowing them to be used more frequently and in new ways.

Quickly zoom in and pan out of the trace. Click on histogram activity to immediately sync to the other trace views to gain additional insight (transaction view, spreadsheet, protocol, etc.)
USB 3.0 Jammer

- Can be used to create a variety of errors in a real OS environment that cannot necessarily be created by a generator
- Standalone unit (does not require analyzer)
  - Example error types, events, packet modification, etc.
    - LGOOD_n / LCRD_a out of order
    - Corrupted ordered sets, LMPs, etc.
    - CRC-5/16/32 errors
    - LBA out of range
    - Link connect / disconnect
    - Power up / down (bus powered devices only)
    - Missing or corrupt frames
    - BOT or UAS Sense IU / Response IU errors

- The jammer can inject errors, modify or delete packets, or even turn off Vbus and turn it back on again
Transmitter Tests

TX tests:
• LFPS (Near end)
• SSC (Near end)
• TX (Far End: TP1)
  • Eye Pattern
  • Tj, Rj, Dj
  • Amplitude

“Embedded channel” automatically tested using Agilent U7243A compliance software
U7243A USB 3.0 TX Compliance Application
TX Testing Requirements: Polling.LFPS to compliance mode

Table 6-7. Compliance Pattern Sequences

<table>
<thead>
<tr>
<th>Compliance Pattern</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP0</td>
<td>D0.0 scrambled</td>
<td>A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences</td>
</tr>
<tr>
<td>CP1</td>
<td>D10.2</td>
<td>Nyquist frequency</td>
</tr>
<tr>
<td>CP2</td>
<td>D24.3</td>
<td>Nyquist/2</td>
</tr>
<tr>
<td>CP3</td>
<td>K28.5</td>
<td>COM pattern</td>
</tr>
<tr>
<td>CP4</td>
<td>LFPS</td>
<td>The low frequency periodic signaling pattern</td>
</tr>
<tr>
<td>CP5</td>
<td>K28.7</td>
<td>With de-emphasis</td>
</tr>
<tr>
<td>CP6</td>
<td>K28.7</td>
<td>Without de-emphasis</td>
</tr>
<tr>
<td>CP7</td>
<td>50-250 1’s and 0’s</td>
<td>With de-emphasis. Repeating 50-250 1's and then 50-250 0's.</td>
</tr>
<tr>
<td>CP8</td>
<td>50-250 1’s and 0’s</td>
<td>With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.</td>
</tr>
</tbody>
</table>

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.
Toggling USB 3.0 TX test modes

- Connect Aux Out to DUT SSRX+ to toggle test modes.
Transmitter test requirements

The eye diagrams are to be measured into 50-Ω single-ended loads.

Table 6-12. Normative Transmitter Eye Mask at Test Point TP1

<table>
<thead>
<tr>
<th>Signal Characteristic</th>
<th>Minimal</th>
<th>Nominal</th>
<th>Maximum</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Height</td>
<td>100</td>
<td>1200</td>
<td>mV</td>
<td>2, 4</td>
<td></td>
</tr>
<tr>
<td>Dj</td>
<td>0.43</td>
<td>UI</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rj</td>
<td>0.23</td>
<td>UI</td>
<td>1,2,3, 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tj</td>
<td>0.66</td>
<td>UI</td>
<td>1,2,3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(TX Far End)
TX Compliance Pitfalls

- SSC modulation
- SSC deviation
- High Rj (flicker Jitter)
- Poor de-emphasis
  - Cause eye failure at end of channel
Tx testing emulated through s-parameters

 Embed Channel File “DEVICE_3MCABLE.s4p”

 Agilent J-BERT N4903B 5Gbps Output

 Agilent T-Rex DSA91304A

 Compliance board and cable

 S-para Emulation by InfiniiSim

 Validation with InfiniiSim of DSA91304A
Transmitter testing uses embedded compliance channel.
Cable and Connectors Compliance

Time Domain

Frequency Domain
Receiver Test Procedure

External Error Counter

Turn on loopback by sending LFPS and required training sequences

The receiver stress pattern is BDAT with SKPs inserted as described in the standard.

The pattern checker receives the looped stress pattern BDAT and recognizes bit errors

After sufficient test time the error counter of the pattern checker is read

Pattern Generator: J-BERT, ParBERT

Pattern Checker: USB Protocol Analyzer; Ellisys USB Explorer and NOW JBERTB SER
Typical SuperSpeed Link Turn-on Sequence
RX Compliance Pitfalls

• Loopback issues
  • Dut needs custom sequence
  • DUT drops out easily

• Calibration issues
  • Inconsistent
  • Poor Sj/Rj mod
  • Automation of Cal

• SSC deviation

• invalid de-emphasis
  • Great impact on TJ

• Jitter tolerance failures
  • 10MHz, 20MHz, 33MHz
N5990A Test Automation Software

Automated instrument control for:

- Setup calibration
- Compliance test
- Characterization test
- Support for debugging

Operator guidance

Sophisticated test reports

Supports full product characterization including transmitter measurements.
Agilent’s USB 3.0 – Total Solution

**Transmitter Test**
- N8805A USB3.0 Protocol decode & triggering SW
- U7243A USB Compliance Test Software
- DSOX90000A Infiniium real time scope
- or
- DSO91304A Infiniium real time scope
- U7242A USB 3.0 Test Fixture

**Signal Conditioning**
- U7242A USB 3.0 Test Fixture

**DUT**
- Tx

**Interconnect Test**
- E5071C Option TDR
- ENA Network Analyzer
- Bit-USB-CBL-0001 from BitifEye
- Cable

**Receiver Test**
- N5990A Automatic SW for USB compliance
- N4903B J-BERT
- High-Perf Serial BERT
- with
- De-emph
- N4916A or
- N4916B or
- N4903B-002
- U7242A Test Fixture
- USB3ET from USB-IF

**Protocol Test**
- (link/transaction layers)
  - U4612A Jammer
  - U4611A/B USB 3.2/1.1 Analyzer

**Fixture**
- Test Fixture

**HW**

**SW**

**Agilent Technologies**
Backup
Agilent Digital Test Roadmap
Covering all key technologies in the computing ecosystem

DVI → DP & HDMI
- Display Port 1.1 → 1.2
- HDMI 1.3 → HDMI 1.4

USB 2.0 → USB 3.0 (5Gb/s)

Faster DDR3
- DDR3 moving to 2133MHz
- DDR4 expected in 2010+

SATA 3G → SATA 6G

PCle 2.0 → PCle 3.0 (8GT/s)

Faster font-side buses
- forwarded clocking
- QPI at 9.6 Gb/s and higher

USB Flash | SD-Movie | USB Flash | HD-Movie
----------|----------|-----------|--------
1 GB      | 6 GB     | 16 GB     | 25 GB  |
22 min    | 2.2 hr   | 5.9 hr    | 9.3 hr |
33 sec    | 3.3 min  | 8.9 min   | 13.9 min |
3.3 sec   | 20 sec   | 53.3 sec  | 70 sec |
Same Setup Supports Multiple Standards

J-BERT, oscilloscope and test automation software also cover

- PCI Express 1.1, 2.0
- SATA 1.5, 3, and 6Gb/s
- DisplayPort 1.1

Note: Additional applications may require additional instruments and accessories