ADS2009
High Frequency and High Speed Co-Design Platform
1. Co-Design, What is it?
   - Case Study: RFIC differential power amplifier

2. Complete Co-Design for 4G LTE application
   - Ptolemy system level co-design
   - X-Parameters
   - Integrated 3DEM
   - ADS/EMPro Co-Design for Improving Handset Performance

3. Summary
Co-Design, Why is it?
- The Trends in High Frequency and High Speed Electronic Designs

Market pressures in consumer wireless electronics are driving exponential growth in functionalities that must be integrated into the same sized and same priced packages.

- Much closer proximity, embedded passives – increased parasitics, couplings
- Multichip modules, and stacked die become more common - forcing IC, package, and board designers to work together more closely
- Multiple available technologies are integrated onto the PCB as shown instead of designing all onto an IC

Chip/package/module/board co-design from the beginning of design process is inevitable!
Motivation for Co-Design: Reducing risk of designing in isolation

90% x 90% x 90% = 73% chance of integration success

Risk increases when more components are integrated
Another View of Co-Design

Sequential Design Process

Project Start → DR1 → DR2 → DR3 → DR4 → Integration

Ex: EEsof Build Process

Con-current Co-Design Process

Project Start → DR1 → DR2 → DR3 → DR4 → Done

Ex: EEsof Build Process
Chip/Pkg/Module/Board Co-Design Case Study
RFIC Differential Power Amplifier Test Board

- Bondwires
- Single Ended PA Output
- PCB
- LTCC Balun
- Si PA
- LTCC Balun
- Single Ended PA Input
- Package

Developed Feb 2009
Let’s Prove Whether The Integration Works
RFIC PA + Balun

RFIC PA, integrated with Ideal and LTCC Balun, meets the performance goals.
Let's Prove Whether The Integration Works
Final Integration of Balun + RFIC PA + Package

DFN Package

LTCC Balun

S-PARAMETERS

SP1

Start: 1.5 GHz
Stop: 3 GHz
Step: 0.01 GHz

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Unexpected or Unpredicted Parasitic Resonance Caught in Last Minute Final Integration Test!

Unexpected parasitic resonance around 1.7GHz

How will this unexpected or unpredicted behavior impact on the development schedule?
Last Minute Design Failure Could Impact Greatly on Design Wins and Time to Market

What if, this is a design failure to meet the spec?
So, will you re-spin the chip? $$$ & TTM
Or re-spin the package? $$$ & TTM
Or bandage the design or just blame others?
Agenda

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   – Ptolemy system level co-design
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3. Summary
Designing for The Single Goal, LTE

- IC Design
- RFIC
- MMIC
- Pkg Design
- Package
- LTCC Balun
- Module Design
- Ant Design
- Board Design
- Duplexer
- RF LNA
- LTCC LPF
- RF Power Amp
Why Not Verify and Test The Designs Against The Targeted System, LTE

As realistic as possible!

As harsh as possible!

We want every circuit, component, even for sub-system designer to use ADS Ptolemy to verify and test their designs under a true co-design environment

So don’t over or under-design circuits, components, or even sub-systems
System Design – LTE Front-End Co-Design

Ptolemy system level co-design allows designers to

• Find problems that will degrade the system’s performance
• Reduce risks inherent in making RF hardware work within a PHY
  – Optimize RF HW to work well with PHY baseband algorithms and HW

Why choose LTE? Why does LTE need Co-Design?

• 3.9G on to 4G standard in same small form-factor to co-exist with existing 2G-3G HW – multiplies the risk
• Challenging RF HW design due to modulation, multiple bands, MIMO, power

ADS2009 has LTE library that is fully framed and coded, supports TDD mode, same algorithms as instruments with full MIMO Tx/Rx and can demodulate faded MIMO channel
ADS 2009 front-end Co-Design infrastructure

1. Simulation platform for multi-technology
   - Faster, higher capacity multi-threaded simulators
   - Acceleration with graphics processors
   - Parallel simulation on compute clusters
   - Intelligent algorithms for increased capacity and accuracy

2. Model support for multi-technology
   - X-parameters non-linear models from measurement
   - 3D electromagnetic components for package, antennas, shields
   - Behavioral & transistor level models
   - Netlist compatibility with HSPICE and Spectre
   - Signal stimulus data to and from instruments

3. Interoperability with back-end co-design platforms from Cadence and Mentor
LTE Front-End Co-Design Flow and Enabling Technologies

Spectrasys, WhatIF

Create candidate architecture
Analyze for noise, spurs, leakage
Validate frequency plan

Validate Tx, Rx w/behavioral models, generate component specs
Re-validate each change w/LTE test benches

Replace behavioral models with component designs

Trade-off and optimize components, add packages, modularize
Re-validate w/LTE test benches

Perform validation of final design; substitute measured components as they become available

Design Flow

- Spectrasys
- WhatIF
- Genesis Synthesis
- Circuit Tools
- Links to ADS (Ptolemy, Test)

- Flexibility
- Diagnostic Speed
- Ease-of-Use
- Analog Effects

- Co-Verification
- Design Flow Integration
- IP Across Simulation Domains

- Ptolemy
- LTE Wireless Library
- Circuit Envelope Co-Simulation
- Simulation consistent with Agilent VSA/Instruments

- Integrated 3D EM
- 3D Components
- Antenna Modeling

- X-Parameters
- Connected Solutions

= Lockout

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LTE Architectural Design – SpectraSys and WhatIF

Spectrasys root-cause analysis capability accounts for all frequencies at all nodes as well as all mismatches and all possible signal or leakage paths across any arbitrary nodes.

WhatIF for frequency planning

• Finds Tx, Rx or Tx/Rx spur-free zones, spurs near desired IF or RF.
Spreadsheets Enough? – Toxic Approximation

Create candidate architecture

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<th>Parts ()</th>
<th>CF (MHz)</th>
<th>CP (dBm)</th>
<th>GAIN (dB)</th>
<th>CGAIN (dB)</th>
<th>COMP (dB)</th>
<th>CNP (dBm)</th>
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Target Pout: 23.072

- Avoid unnecessary over-specification causing design delays and increased component costs

- “Traditional Spreadsheet” Gain is 9 dB too high – will cause miss-specification and force a re-spin

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Circuit/System/EM Co-Simulation Co-Validates Candidate System to LTE Specs

Fully framed and coded, bit accurate LTE UL source; set frequency and power.

Validate Tx, Rx w/behavioral models, generate component specs.

LTE measurements use same algorithms as Vector Signal Analyzer / Instruments.

Circuit-Level Components in Uplink:
1. Gilbert Cell Mixer
2. PC Board Amps
3. LTCC Low-Pass Filter
4. X-Parameter Driver Amp
5. Packaged MMIC PA
6. Tunable antenna match

Replace behavioral models with component designs.
Breath and Depth of ADS Co-Design
LTE Transmitter Sub-System Test Bench

Board AMP
RFIC
LTCC LPF
MMIC
Antenna

Constellation for First Frame Data
Real Time Ptolemy Co-simulation with VSA for TX
Chip/Packet Co-Design in MMIC PA

S11 < -15 dB
S22 < -15 dB
Gain > 20 dB

LTE SPECS
Transmitter Pout = 23 +/- 2 dBm
PA Pout = 24.5 +/- 2 dBm
Duplexer + Coupler loss 1.5 dB
Completed MMIC PA with DFN Package + Bondwire

True MMIC Design Verification prior to Manufacturing is done by Co-simulating the MMIC inside the package and with bond wires using 3D EM simulation in ADS.
MMIC PA Verification With/ Without Package + Bondwires

Large Signal Gain of MMIC PA without Package and without Bondwires

- S21 Spec > 20 dB

Large Signal Gain of MMIC PA with Package and with Bondwires

- S21 Spec > 20 dB

A slight drop in gain (.12 dB) is due to the bond wire and Package effects.
LTE Wireless library Verification in ADS

**ADS**
- True Circuit Level Co-Simulation with Fast Verification modeling (AVM)
- CE ties the circuit with Ptolemy
- Able to optimize for ACPR, EVM...
- Accounts for the Frame structure
- Identical to the real Wireless signal
- True and Accurate verification

LTE: Uplink transmitter EVM measurement
LTE Wireless library Verification in ADS

- Gating “ON” on a typical wireless signal: “Measures on the burst” Fully compliant with wireless stds
- Gating is “OFF” Not accurate & not compliant with wireless standards

Other EDA Tools

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Simple Simulation Based X-Parameter Extraction in ADS 2009

In ADS 2009, you will be able to create simulation based X Parameters for your circuits. You can then use these X parameters in X-Parameter model to do higher level simulations to understand more about your design.

X Parameters in ADS
1. Insert X Parameter template which is already setup for the extraction.
2. Connect your DUT.
3. Modify Power levels and frequencies as needed.
4. Simulate.
What are X-Parameters?

Parameters that capture non-linearties of amplitude and phase at specified harmonics

Extracted either from measurement or simulation

- Easy extraction of parameters based on automated NVNA
- New devices, for example GaN, with inaccurate models can be easily characterized
- Drag and Drop-in ADS X-Parameter models

Tuners that covers all regions on the Smith Chart (all Impedances)

Cable / connectors

Source Pull Tuner

Load Pull Tuner

NVNA Measures X-Parameters

Bias System

MDIF File

PHD model generation for ADS

ADS

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LSOP In Our Example

Voltage @ DC-bias port

Current @ DC-bias port

Input incident

Output incident

Input reflected

Output reflected

x_1_AmpDUT

Amp1
Breakthrough Non-Linear X-Parameters

Value for Co-Design:
• PA vendors can offer X-parameters to the system integrators such as mobile phone manufacturing companies for an evaluation from the early stage of design process
• PA vendors can protect the design IP (Intellectual Property)
Validate Candidate Rx in MIMO Configuration

Dual handset antennas with correlation, from EMPPro FDTD

Perform validation of final design; substitute measured components as they become available

Only ADS can test this 2X2 MIMO configuration for the one performance spec that really matters: BER/PER with channel fading
Breath and Depth of ADS Co-Design

Receiver Sub-System Test Bench
Real Time Ptolemy Co-simulation with VSA for RX
Breath and Depth of ADS Co-Design

LTE Top Level System Test Bench

Entire system simulation that includes Tx, Channel, and Rx

- Fully framed and coded, bit accurate LTE UL source; set frequency and power

- LTE measurements use same algorithms as Vector Signal Analyzer / Instruments
Real Time Ptolemy Co-simulation with VSA for Whole System
Integrated 3D EM is the Key to Co-Design

Integrated 3D EM is essential technology to Co-Design as demonstrated

Integrated 3D EM also saves cycle time on the EM front-end process

Reducing “EM front-end process”, the process from entering the design geometry to being ready for the simulation, could save hours of simulation setup time (1hr +) and also on CAD resources.
3DEM Co-Design With FlipChip IC Packaging

**Our value:** Greatly reduce the risk that comes with the final integration by co-designing the circuit, package, and board interface together. Create 3D components, like solder bumps (with EMPro UI) and use them in ADS to get the most accurate prediction of the overall behavior.

**Application Area:** Package/Board interface with Solder Bumps
3DEM Co-Design With RF/MMIC QFN Packaging

Microstrip Line on ThinFilm Substrate
Chip
Board Microstrip Feed
Board
Double Bonding Wires

Improved Package Transition

Cyan & Dark Green: Original Design

dB(S21) dB(S11)

freq, GHz

Cyan & Dark Green: Original Design
3DEM Co-Design With Mechanical Shield

Our value: RF Designers can create EM shielding in minutes – No need to waste time redraw difficult 2-D layout, set up layers, material parameters, ports, boundary conditions, etc. in standalone 3DEM tools just to see what happens when you place a shield on top.

No more approximation! What you see is what you get (WYSIWYG)
ADS/EMPro Co-Design for Improving Handset Performance

- Adaptive Antenna Matching Co-Design using EMPro – ADS

- Co-Design and Optimization of Switched WLAN antenna using EMDS G2, Momentum G2 & Circuit Simulation

- Calculate Antenna Diversity for Use in LTE MIMO Channel Simulation Using EMPro & Ptolemy
Co-Design with Adaptive Antenna Matching

Tuning Time Const

VSWR

GSM_antenna Signal

Adaptive BST

VSWR block

Time Switch Between 2 Antenna Configurations

Tuning Network

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EMPro Antenna Diversity calculations and MIMO System Simulations

Solve The Multiple Reflection Problem For Increased Bandwidth

EMPro Assures Antenna Diversity In All Environments

Indoor Environment

Outdoor Environment
ADS 2009 enables frontend Co-Design with:

**Signal Integrity**
- Channel Simulator
- GPU Accelerated Transient Simulator
- New, fast eye diagram measurements
- Djordjevic loss model for fast, causal multilayer models
- Causality-corrected microstrip and stripline models
- Threaded impulse characterization for faster convolution

**Momentum G2 Planar 3DEM**
- Improved meshing
- Improved resistance modeling
- Port re-sequence for easy S-Parameter interpretation
- Substrate stack driven viewing utilities
- Enhancements to Broadband Spice Model Generator for passivity and causality

**Physical Layout**
- DRC for Flattened Layout
- DRC 3rd-party integration (Assura, Calibre, MailDRC)
- PDK Builder for Schematic
- Enhanced layout and SMT connectivity transfer from Allegro PCB, APD and SIP

**Simulation**
- Support HSPICE .pat statement
- Arbitrary Jitter Analysis
- Multi-threaded harmonic balance
- Improved Passive Circuit Design Guide
- Wireless Libraries (WiMedia v1.2, 3GPP/LTE MIMO v8.3.0 & v8.4.0)
- Pole-zero custom frequency-dependent voltage and current sources

**Usbility**
- AEL Debugger for ADS customization
- Data Display snap-to-grid alignment
- New 50 ADS examples
- Direct drawing of pass-fail limit lines on plots
- Fast variable setup tab for statistics and DOE simulation

**EMDS G2 full 3DEM**
- 3D parameterized components
- Improved mesher and solver
- Fast frequency sweep for iterative solver
- Symmetry planes
Summary

ADS 2009 enables front-end Co-Design with:

1. Multi-Technology Simulation Platform
   - Multi-threading
   - Acceleration
   - Channel Simulator
   - LTE, Wimax, WiMedia verification libraries

2. Multi-technology Model Support
   - X-parameters
   - 3D EM integration

3. Interoperability with backend design platforms