

## ***ADS USERS' GROUP MEETING***

***A 8W, High efficiency X-band  
Power PHEMT amplifier  
designed with ADS Agilent software***

**June 16, 2009**

**T. Huet, C. Byl, V. Serru**

**UMS is a company of THALES and EADS**

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**\*UMS GmbH:** Wilhelm Runge Strasse 11, 89081 Ulm, GERMANY

# Outline

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- Motivation
- ADS AGILENT software & UMS design kits
- Considerations on HPA
- UMS PPH25X technology
  - ◆ Transistors characterization
- Design methodology
- 2-stage HPA
  - ◆ Harmonic Balanced Simulations (standard + 3D planar)
  - ◆ Measurements
  - ◆ Main performances and layout
- Conclusion

# Motivation

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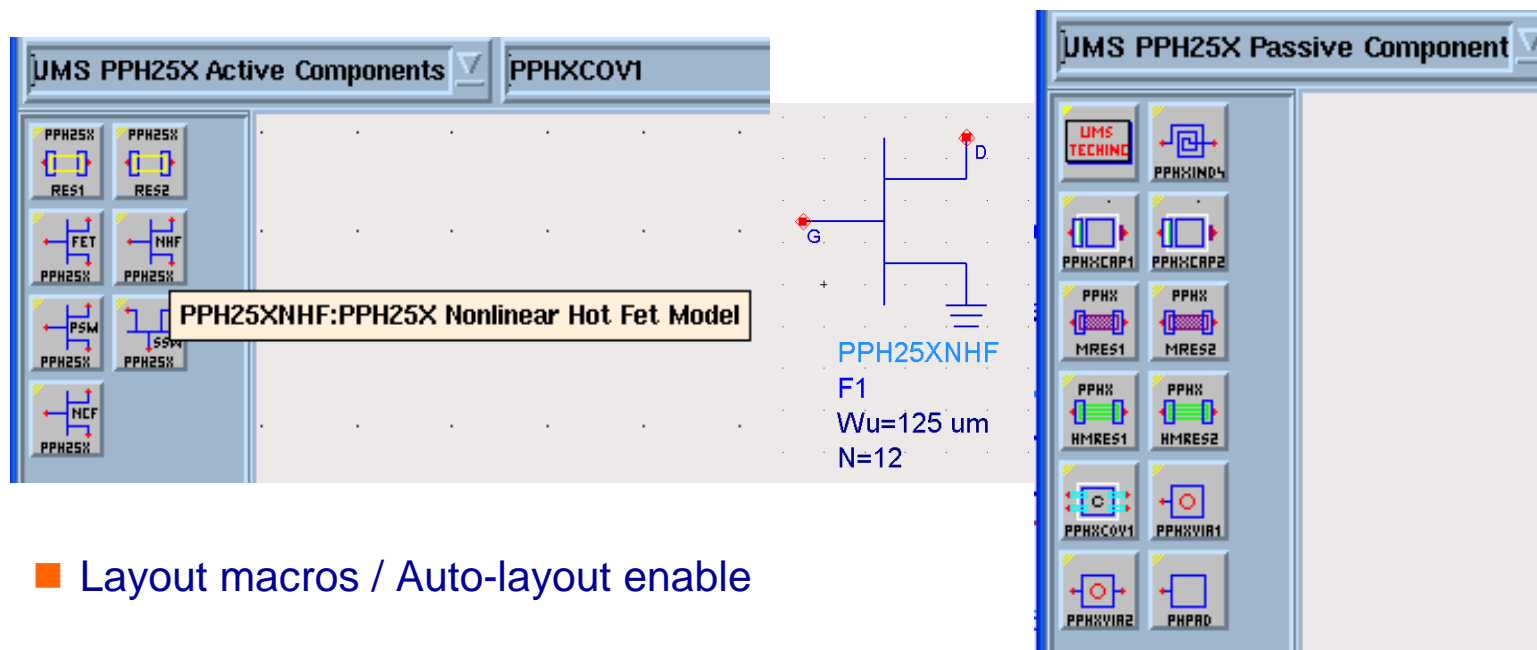
Monolithic Microwave Integrated Circuits HPAs based on Gallium Arsenide are dedicated to T/R modules for Phased Array radars. Very high efficiency and high power are required for these X band applications.

The design goal was to demonstrate that the UMS Power PHEMT technology (PPH25X) enables the generation of robust HPAs using the “Advanced Design System” software from Agilent.

# Agilent Software

- Available on Agilent Software:

- Customized environment
- Linear and non linear electrical transistor models
- Passive components electrical models



- Layout macros / Auto-layout enable

- User's manual and installation guide

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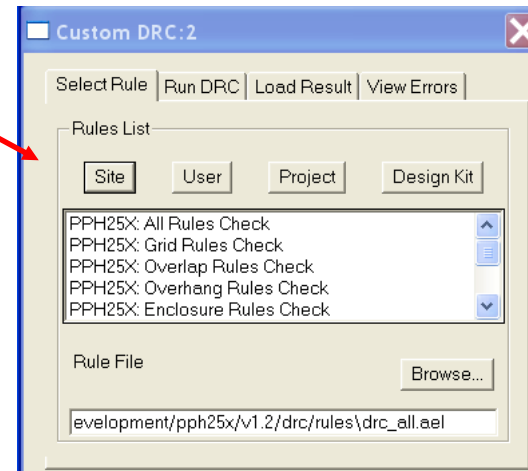
# Agilent Software

- **New structure for UMS Design Kit since ADS2003:**

- Based on the infrastructure officially supported by Agilent
- Easy to install (no more system variables to set)

- **New available features:**

- Dynamically Linked Library (Linux and Windows)
- Integrated statistical model definition for Monte Carlo analysis
- Design Rule Checker (DRC)
- Alphabet layout macro



# Agilent Software

- **Schematic entry:**

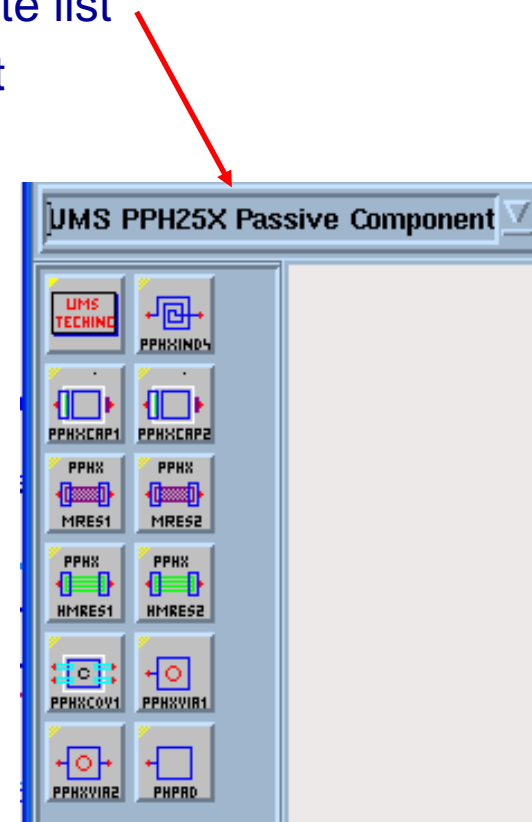
- Components accessible from the library or palette list
- Specific symbol and bitmap for each component
- Spread parameters
- Parameters for physical layout

- **Electrical models:**

- User defined and C compiled models

- **Layout macros:**

- Fixed artwork for RF and DC pads
- AEL language for all scalable components



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# Agilent Software dedicated to UMS PPH25X technology

The screenshot displays the Agilent software interface for UMS PPH25X technology. The main window shows a toolbar at the top with various icons. Below the toolbar, a dropdown menu labeled "UMS PPH25X Active Components" is highlighted with a red oval. The main workspace contains a schematic diagram of a transistor circuit with nodes labeled 'G' and 'D'. Below the schematic, the following parameters are listed:

- PPH25XFET
- F1
- Wu=125 um
- N=12
- Vds=7.0

A dialog box titled "PPH25X Nonlinear Hot Fet Model" is open in the foreground. It contains the following information:

- Instance Name (name[<start:stop>]): F1
- Select Parameter: Wu=125 um, N=12, ( dVt=dvt\_PPH25X ), ( Bcb="no" )
- Parameter Entry Mode: Standard
- Wu: 125 um
- Buttons: Equation Editor..., Tune/Opt/Stat/DOE Setup...

Another window titled "UMS PPH25X Active Components" is also visible, showing a dropdown menu for "PPH25XNHF" and a schematic diagram of a transistor circuit with nodes labeled 'G' and 'D'. Below the schematic, the following parameters are listed:

- PPH25XNHF
- F1
- Wu=50 um
- N=4

Below this schematic, a resistor component is shown with the following parameters:

- PPH25XRES2
- R1
- R=500 Ohm
- L=100.0 um
- T=293.0

A red oval highlights the "UMS PPH25X Active Components" dropdown menu in this window as well.

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# Agilent Software dedicated to UMS PPH25X technology

The screenshot displays the Agilent software interface for UMS PPH25X technology. The main workspace shows a schematic with several components:

- PPHXCAP2 C1**: Capacitor with  $C=2.5\text{ pF}$ ,  $FG=1.0$ ,  $WB=20.0\text{ }\mu\text{m}$ , and  $ANG=0$ .
- PPHXIND4 L1**: Inductor with  $L=1.0\text{ nH}$ ,  $W=5$ ,  $ANG1=0$ ,  $H=10.0\text{ }\mu\text{m}$ , and  $Ldrawn=0.92\text{ nH}$ .
- PPHXVIA1 V1**: Via component.
- PPH25XNHF F1**: Transistor with  $Wu=130\text{ }\mu\text{m}$  and  $N=12$ .
- PPHXCOV1 C2**: Capacitor with  $C=2.5\text{ pF}$ .
- PPH25XRES1 R2**: Resistor with  $R=500\text{ Ohm}$ ,  $W=20.0\text{ }\mu\text{m}$ , and  $T=293.0$ .
- PPHXMRES1 R1**: Resistor with  $R=30\text{ Ohm}$ ,  $W=10.0\text{ }\mu\text{m}$ , and  $T=300.0$ .

An **Inductor** dialog box is open, showing the configuration for **PPHXIND4**. The **Instance Name** is **L1**. The **Parameter Entry Mode** is set to **Standard**. The **Select Parameter** list includes **L=1.0 nH**, **W=5**, **( DL=dl\_Ind4 )**, **( DR=dr\_Ind4 )**, **ANG1=0**, **H=10.0 um**, **( Bcb='no' )**, and **( Ldrawn=0.92 nH )**. The **L** parameter is currently set to **1.0** with units of **nH**. The **Display parameter on schematic** checkbox is checked.

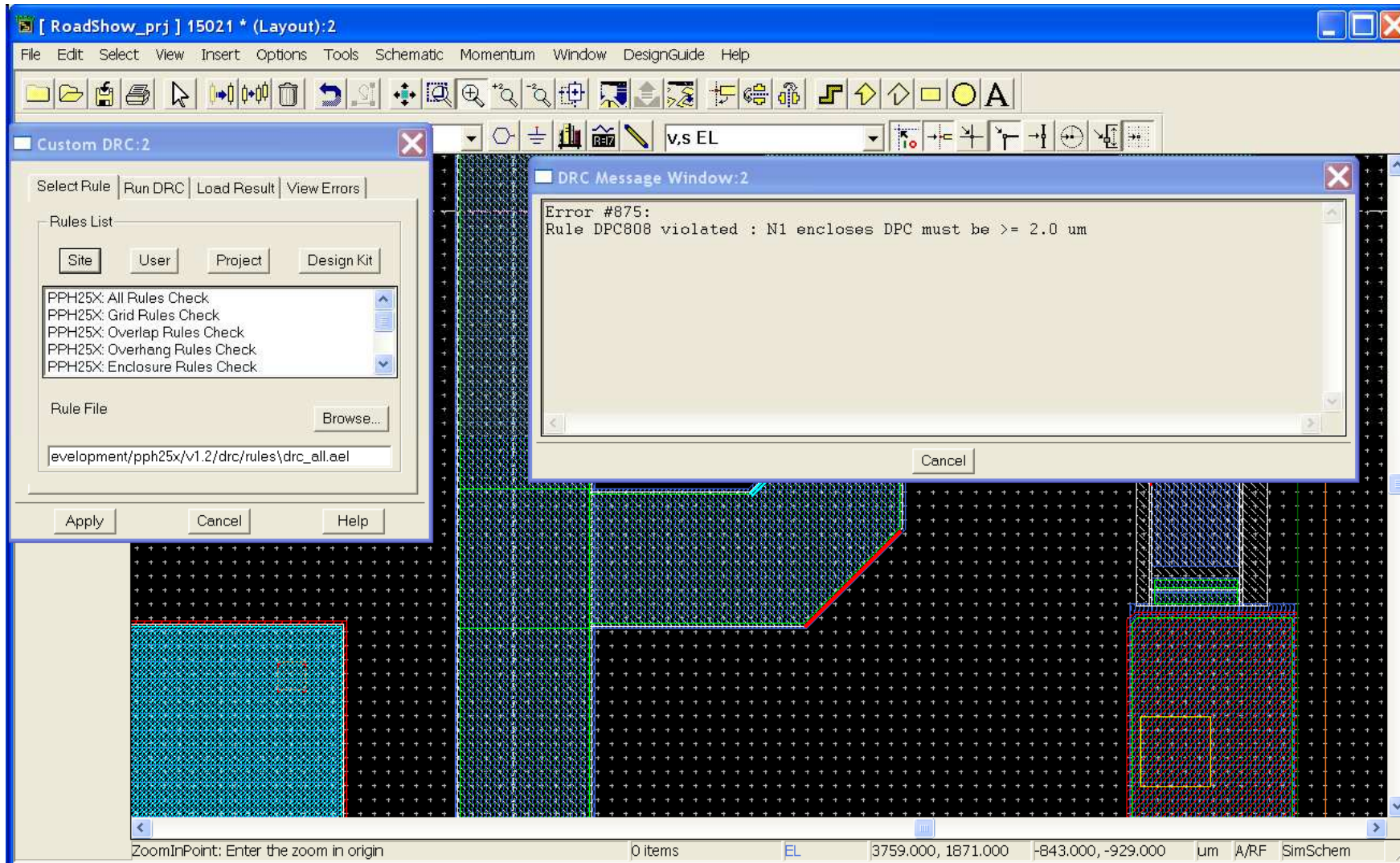
*Hot transistors, MIM Capacitors (standard + over Via) Inductors, Resistors and VIA Models used in UMS PPH25X Design KIT*

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# Agilent Software dedicated to UMS PPH25X technology

*UMS PPH25X Design KIT: Design Rules Checking available*



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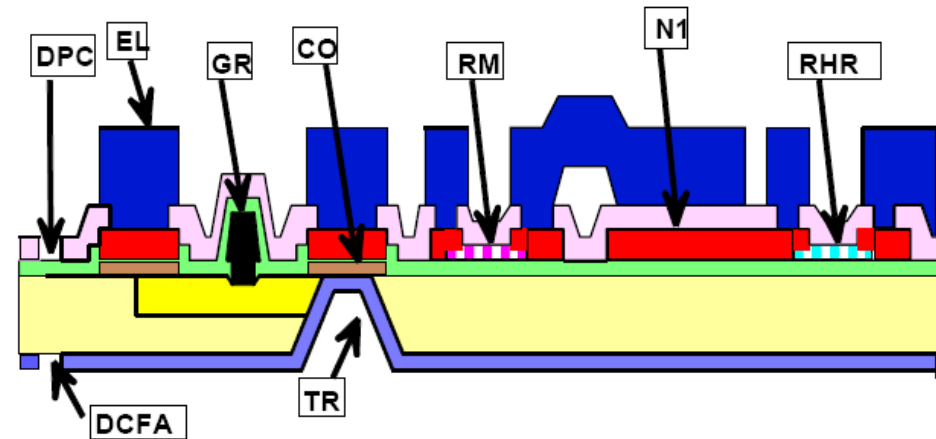
# ***APPLICATION TO THE DESIGN OF A HIGH POWER AMPLIFIER***

**June 16, 2009**

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# UMS PPH25X Technology

## MAIN FEATURES



- Space evaluated technology (ESA)
- Double recess 0.25  $\mu\text{m}$  gate length
- High power density ( 0.85W/mm )
- High gain (16dB at 10 GHz for power cell 12X130 $\mu\text{m}$ )
- High breakdown voltage (  $V_{bds} \sim 20 \text{ V}$  )
- Over vias MIM Capacitors
- 70  $\mu\text{m}$  substrate thickness with small via-holes

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# Transistors Characterisation

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- In order to reach good performances at HPA level, a good knowledge of the transistors is required.
- Transistors accuracy is based on standard measurements:
  - S parameters measurements:
  - Pulsed I-V measurements:
  - Load pull measurements:
    - To define transistor optimum loads for output power, PAE and drain current.

# Design methodology

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- **Class A-B amplifier**
- **Choose the transistor size and optimum load impedance taking into account:**
  - Linear gain, Pout, PAE
  - Frequency band
  - Output mismatch (VSWR=2:1)
  - Safe operating area (robustness)
- **HPA matching network (output combiner,...)**
- **Non linear stability analysis (odd and even mode)**

# Tools for HPA designs

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- **Load pull simulations**
- **Optimization/Tuning**
- **“Standard” simulations**
  - Small signal simulations (S parameters)
  - Harmonic balanced simulations (non linear simulations)
  - Time domain simulations (switching time specifications)
- **EM simulations for passive networks: Momentum simulations to check coupling effects, symmetries and proximities.**
- **Statistics:**
  - Technological spread analysis to check design sensitivity and give expected electrical yields
- **Auto-layout generation and Design Rules Checker**

# Transistors selection: Loadpull by simulation

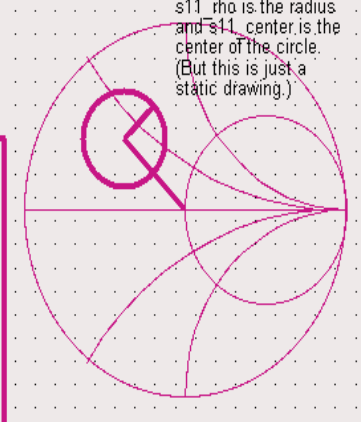
One Tone Load Pull Simulation; output power and PAE found at each fundamental load impedance

Specify desired Fundamental Load Tuner coverage:  
 $s_{11\_rho}$  is the radius of the circle of reflection coefficients generated. However, the radius of the circle will be reduced if it would otherwise go outside the Smith-Chart.  
 $s_{11\_center}$  is the center of the circle of generated reflection coefficients.  
 $pts$  is the total number of reflection coefficients generated.  
 $Z0$  is the system reference impedance

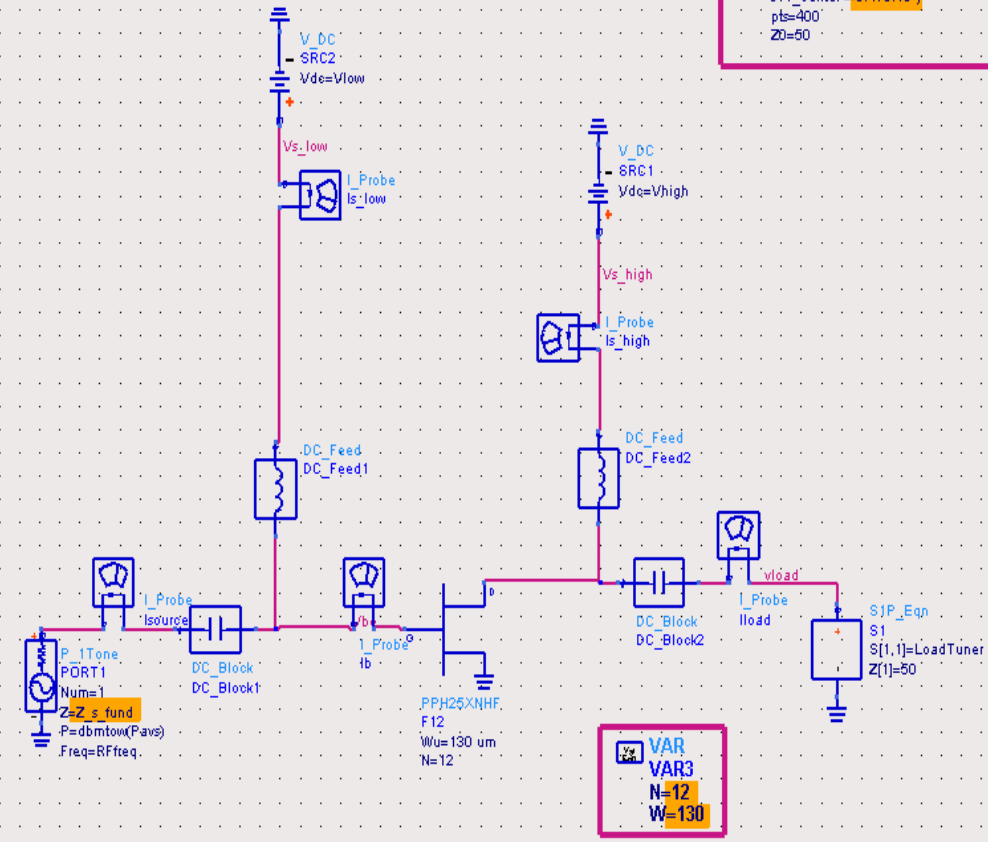
```

VAR:
SweepEquations
s11_rho=0.45
s11_center=0.4+0.15j
pts=400
Z0=50
    
```

$s_{11\_rho}$  is the radius and  $s_{11\_center}$  is the center of the circle. (But this is just a static drawing.)



Refer to the data display file "ReflectionCoefUtility" for help in setting  $s_{11\_rho}$  and  $s_{11\_center}$ . Also, refer to the example design file: examples/RF\_Board/LoadPull\_prj/HB1Tone\_LoadPull\_eqns for details about how this simulation is run.



```

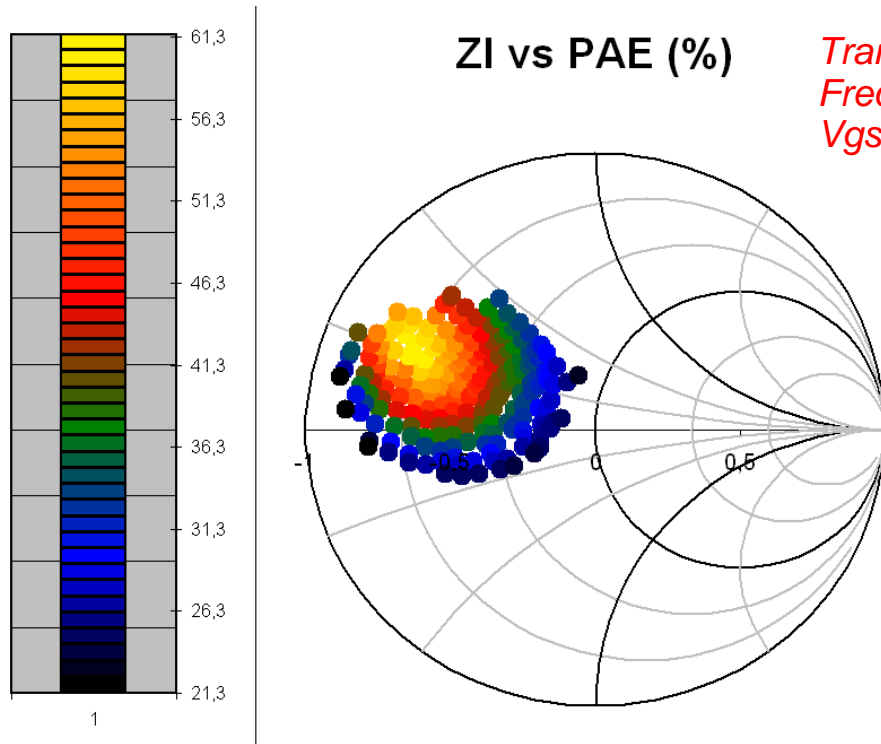
VAR
VAR3
N=12
W=130
    
```

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# Transistors selection : Loadpull by simulation

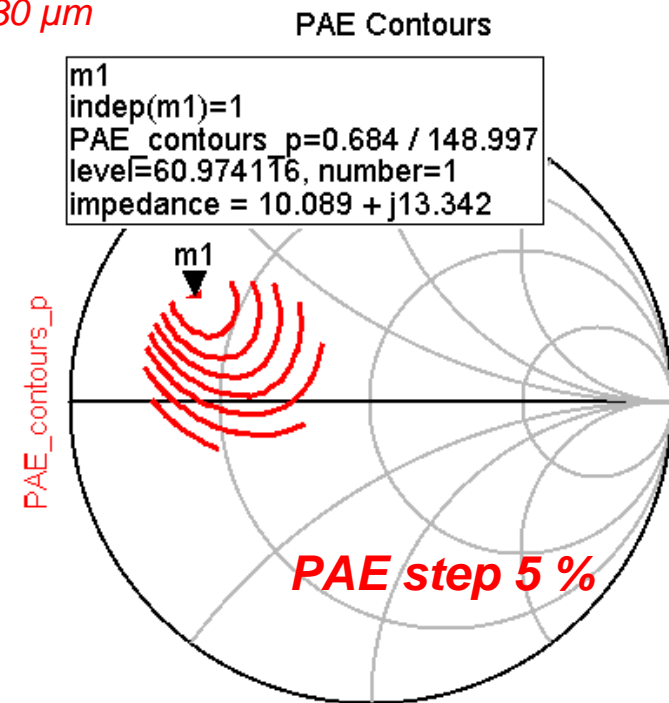
## Load pull for PAE contours

**Good accordance between Measurements and simulation**



Load pull Measurements on PPH25X transistor

Transistor size: 12 x 130  $\mu\text{m}$   
Frequency = 10 GHz  
 $V_{gs} = -0.35\text{V}$ ,  $V_{ds} = 8\text{V}$



Simulation with ADS software using UMS transistor model

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# Transistors selection

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The HPA was developed in the frequency Band: 8.5-11.5 GHz.

## □ 2-STAGE VERSION

*Design goal @25°C: Pout>8W, PAE>35%, Linear Gain= 20 dB*

*Pulse conditions for drain: 25μs, 10%*

*No specifications on linearity*

*Chosen topology :*

First stage: 2 power cells (12x130 μm)

Second stage: 8 power cells (12x130 μm)

# 2-stage HPA: Combiner optimisation

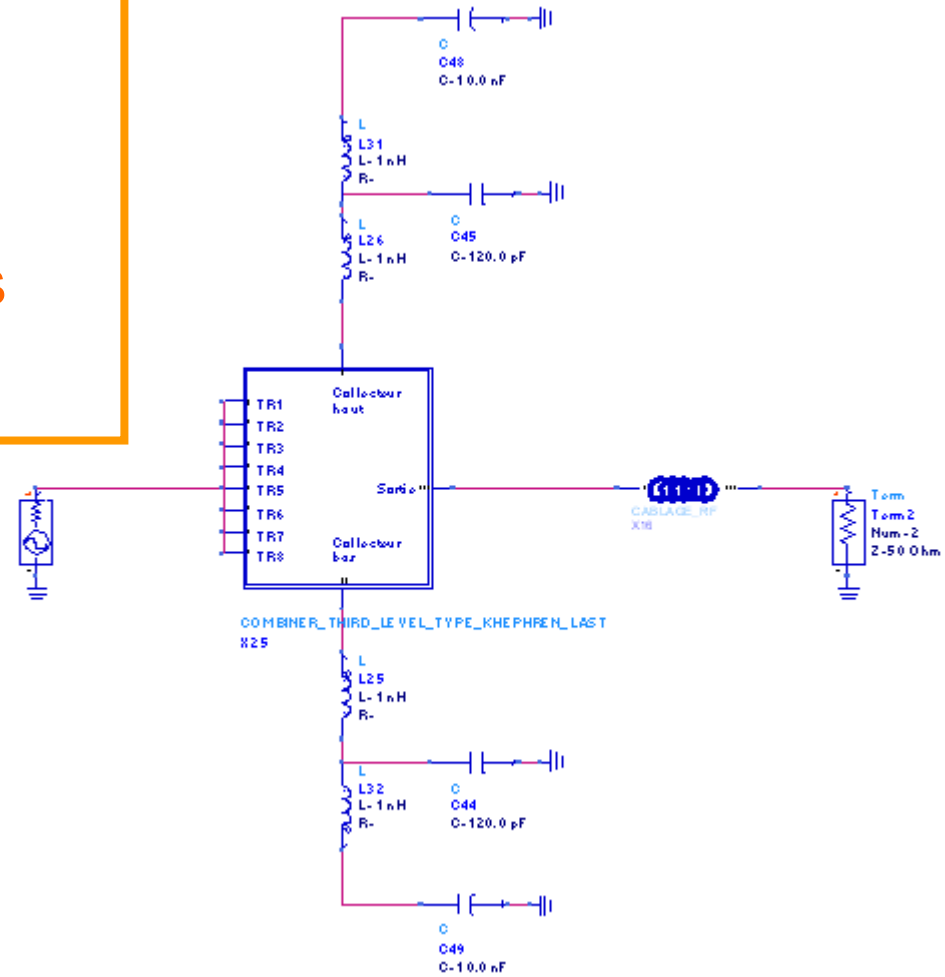
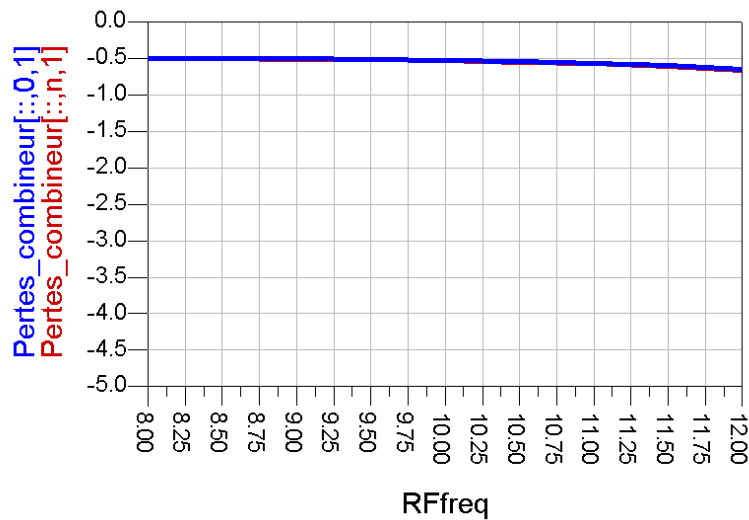
## Combiner optimisation

8-12GHz

Low insertion losses

UMS passive components

Agilent microstrip models



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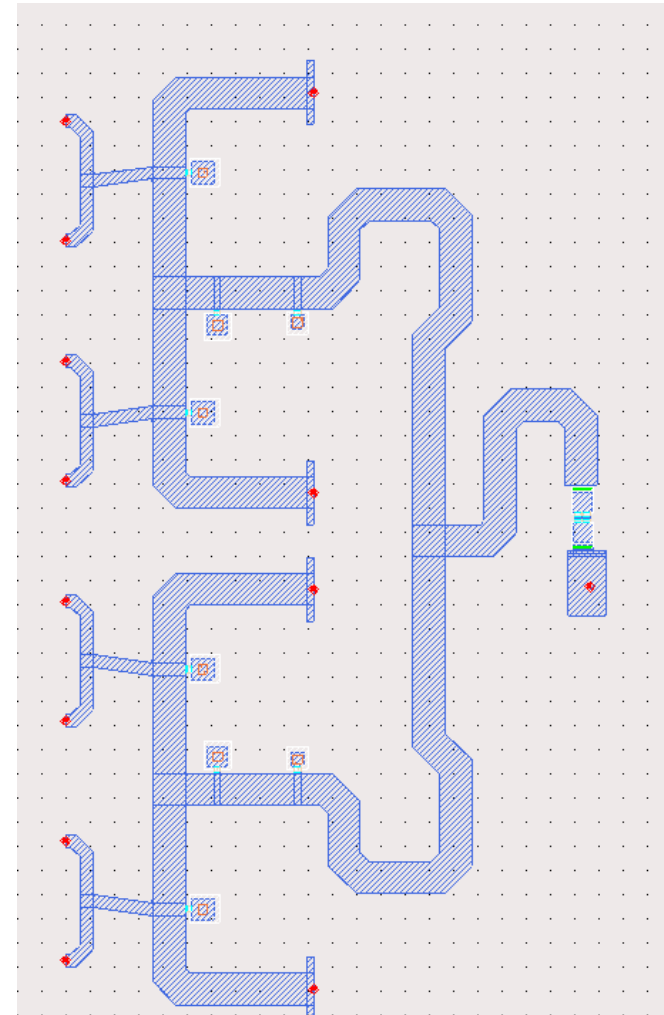
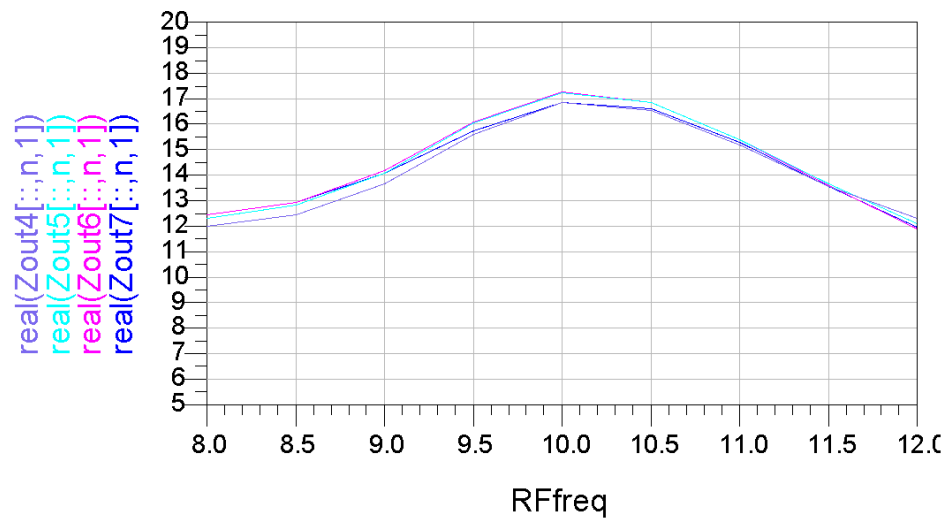
# 2-stage HPA: Combiner checking

## Combiner symmetry

8.5-11.5GHz

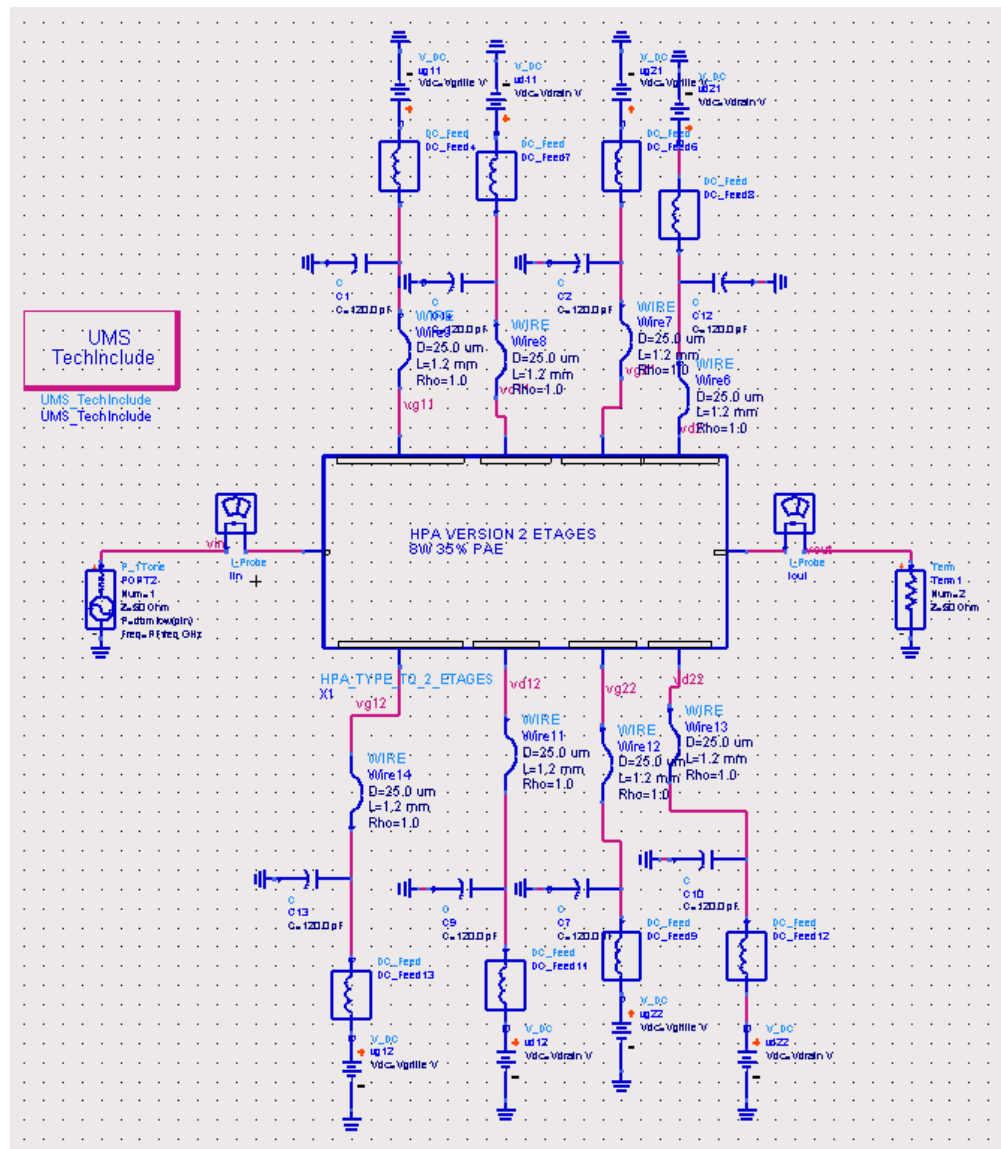
Low insertion losses

Agilent 3D planar momentum



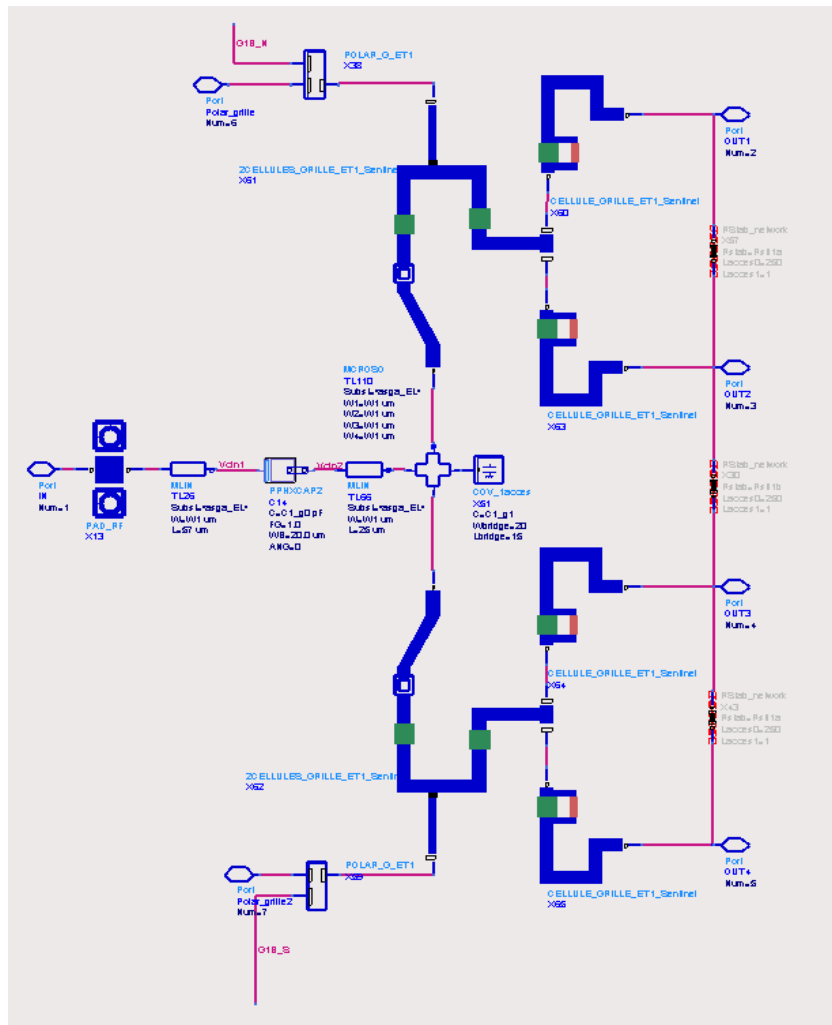
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# 2-stage HPA: simulation with ADS software

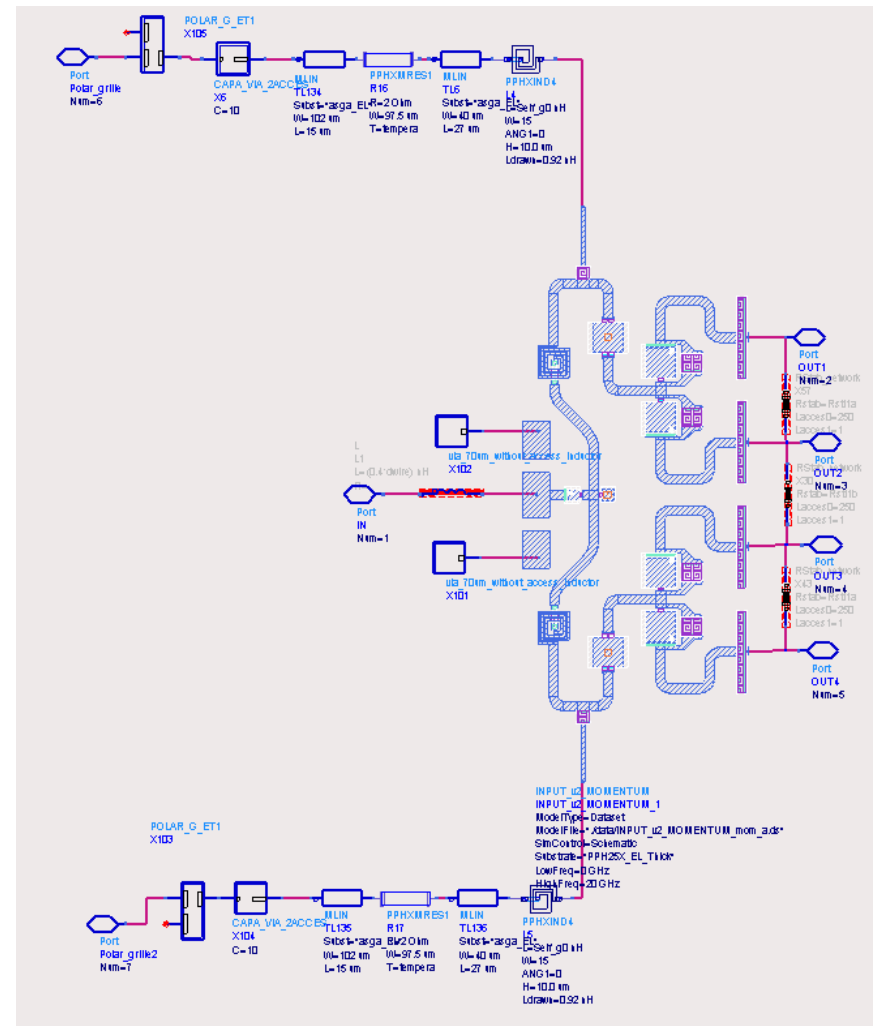


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# 2-stage HPA: simulation with ADS software



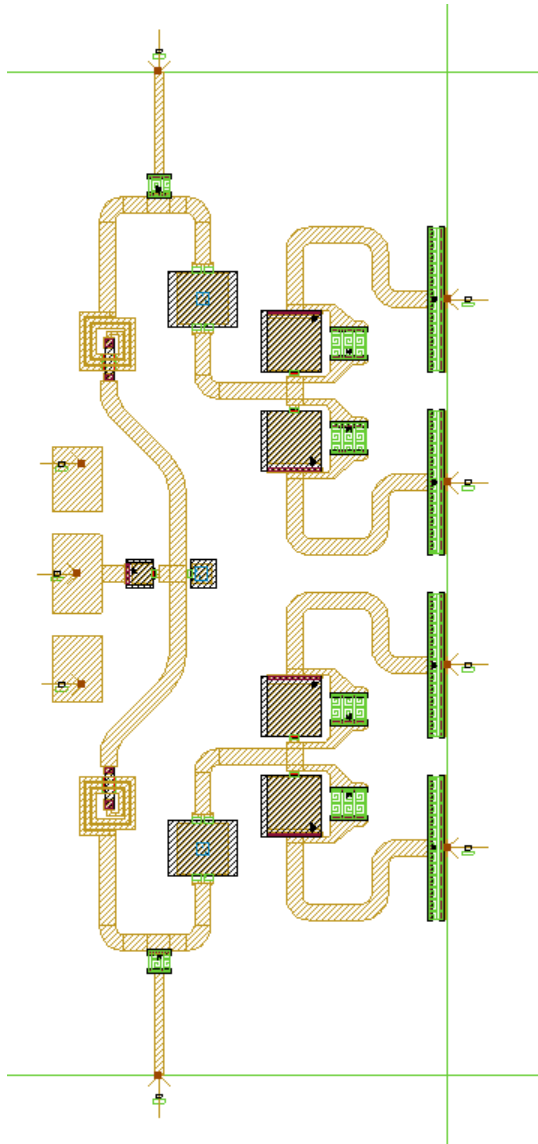
ADS components from UMS PPH25X design Kit and ADS libraries



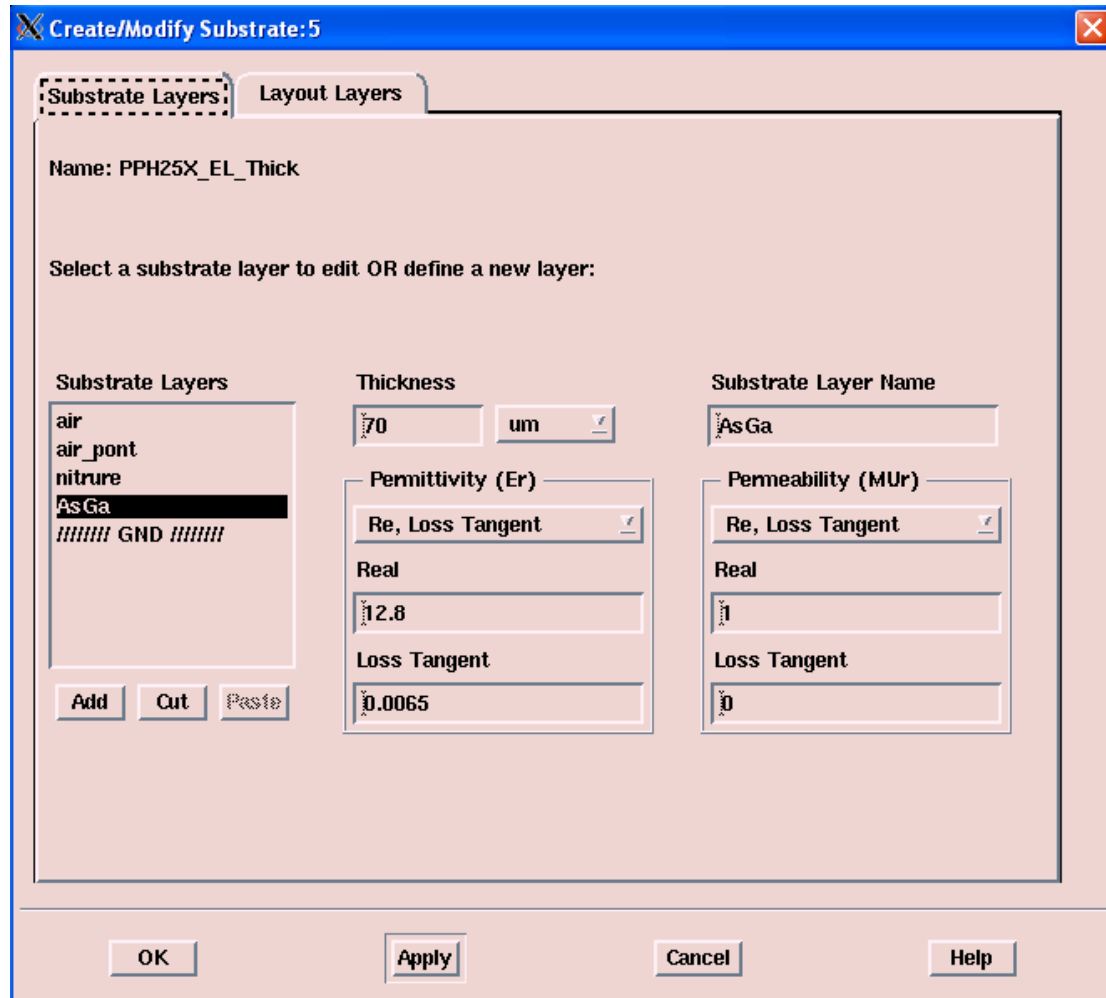
ADS components from UMS PPH25X design Kit and ADS libraries + 3D planar momentum Simulation

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# 2-stage HPA: simulation with ADS software

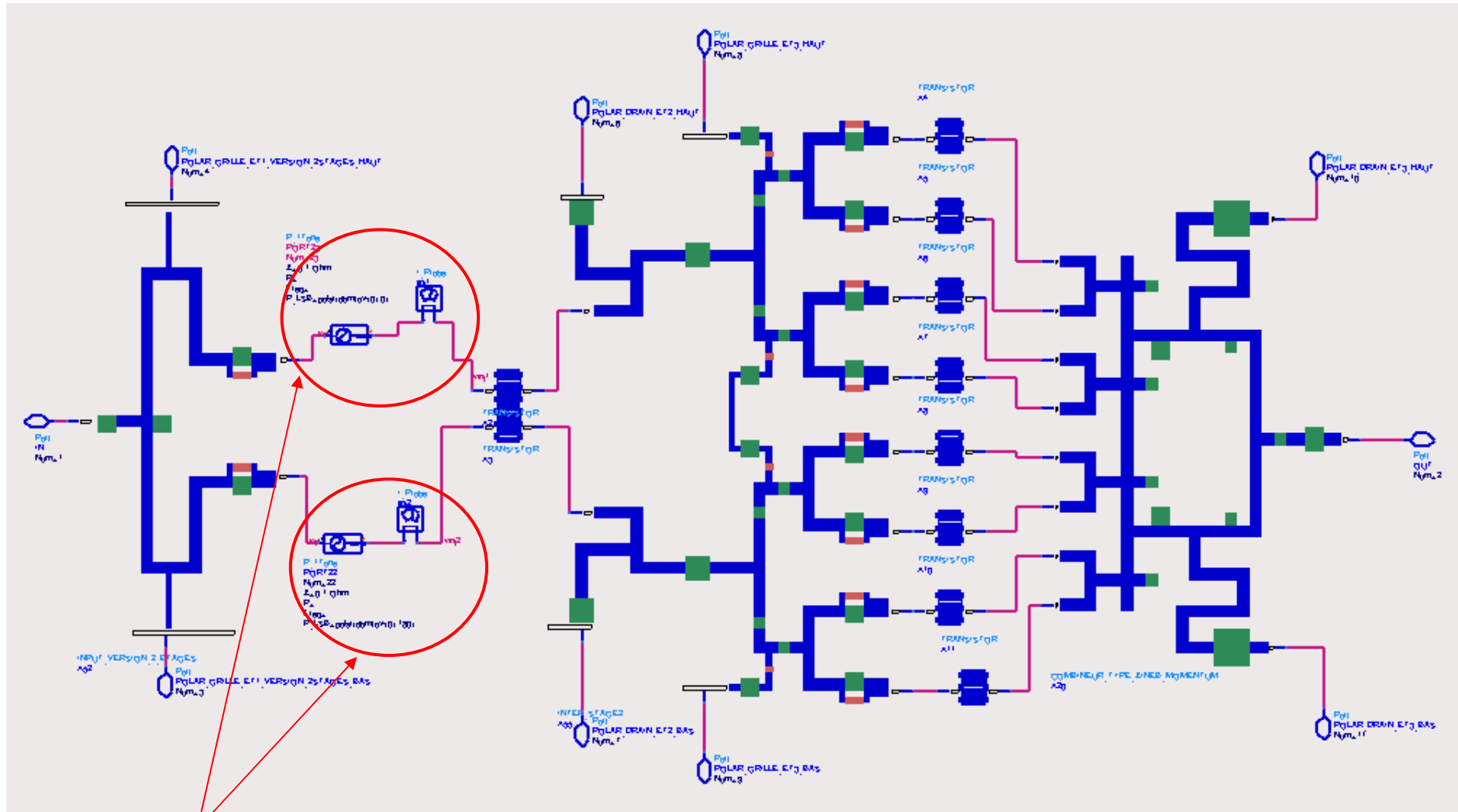


3D planar momentum Simulation for Passive Networks:  
SUBSTRATE DEFINITION FOR PPH25X TECHNOLOGY



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# 2-stage HPA: Stability analysis



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*Components used for non linear stability analysis*

# 2-stage HPA: Stability analysis

## Stability

Wide band stability checking  
vs Frequency band & Input  
power



### HARMONIC BALANCE

```
HarmonicBalance
HB3
MaxOrder=5
Freq[1]=RFfreq
Order[1]=5
SS_MixerMode=yes
SS_Plan=
SS_Start=
SS_Stop=
SS_Step=
Start=1.01e9
Stop=30.01e9
Step=300078153
Pt=
```



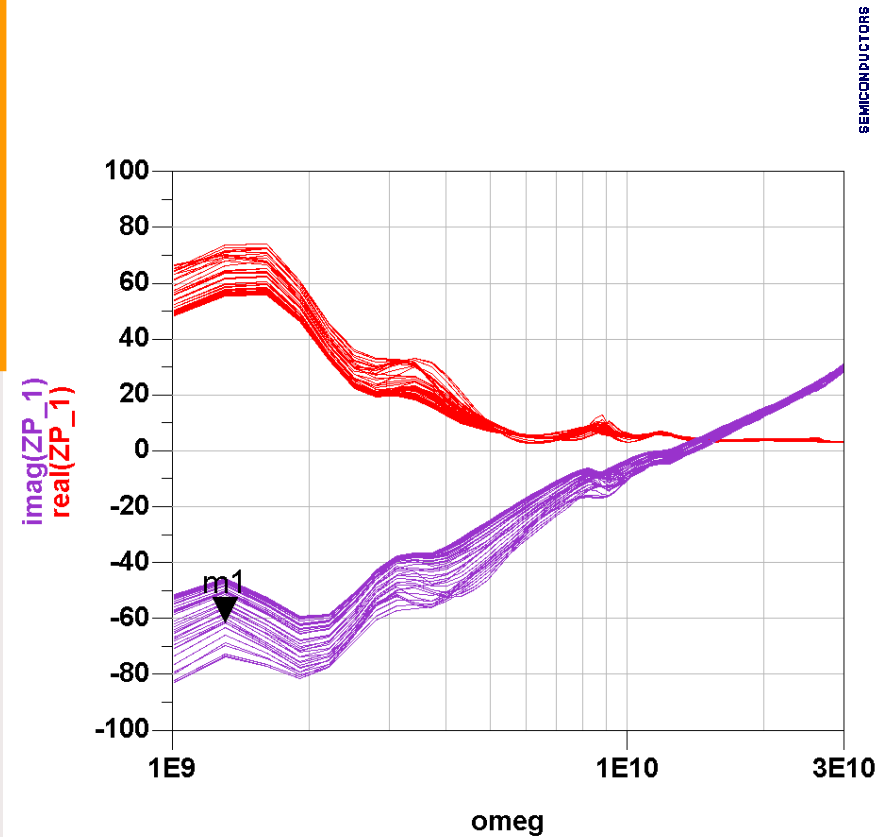
### PARAMETER SWEEP

```
ParamSweep
VarOm
SweepPlan="VarPe"
SweepVar="Pin"
Pt=20
```



### PARAMETER SWEEP

```
ParamSweep
fr_sw
SweepPlan="SwpPlan1"
SweepVar="RFfreq"
Start=2e9
Stop=8e9
Step=1e9
```

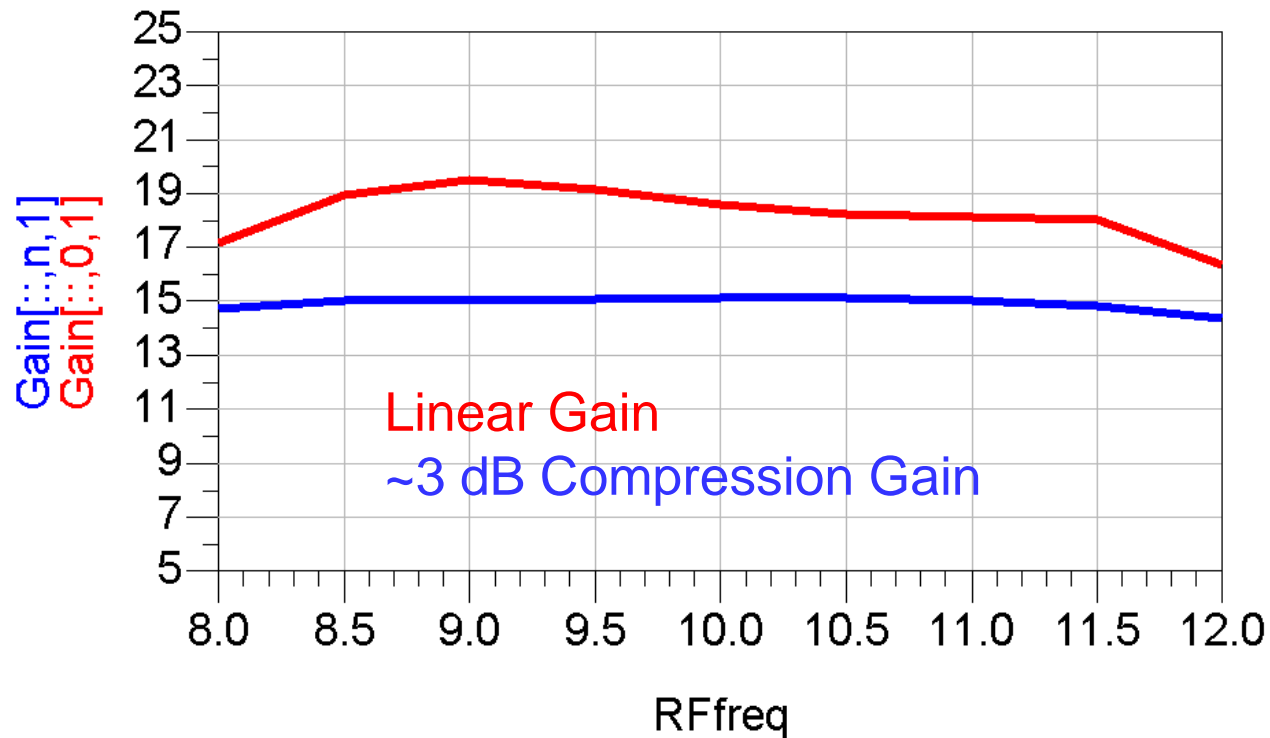




# 2-stage HPA: simulation with ADS software

**Linear Gain and compressed gain  
@3dB compression vs frequency  
@20°C**

Drain voltage= 8V  
Quiescent current= 2A

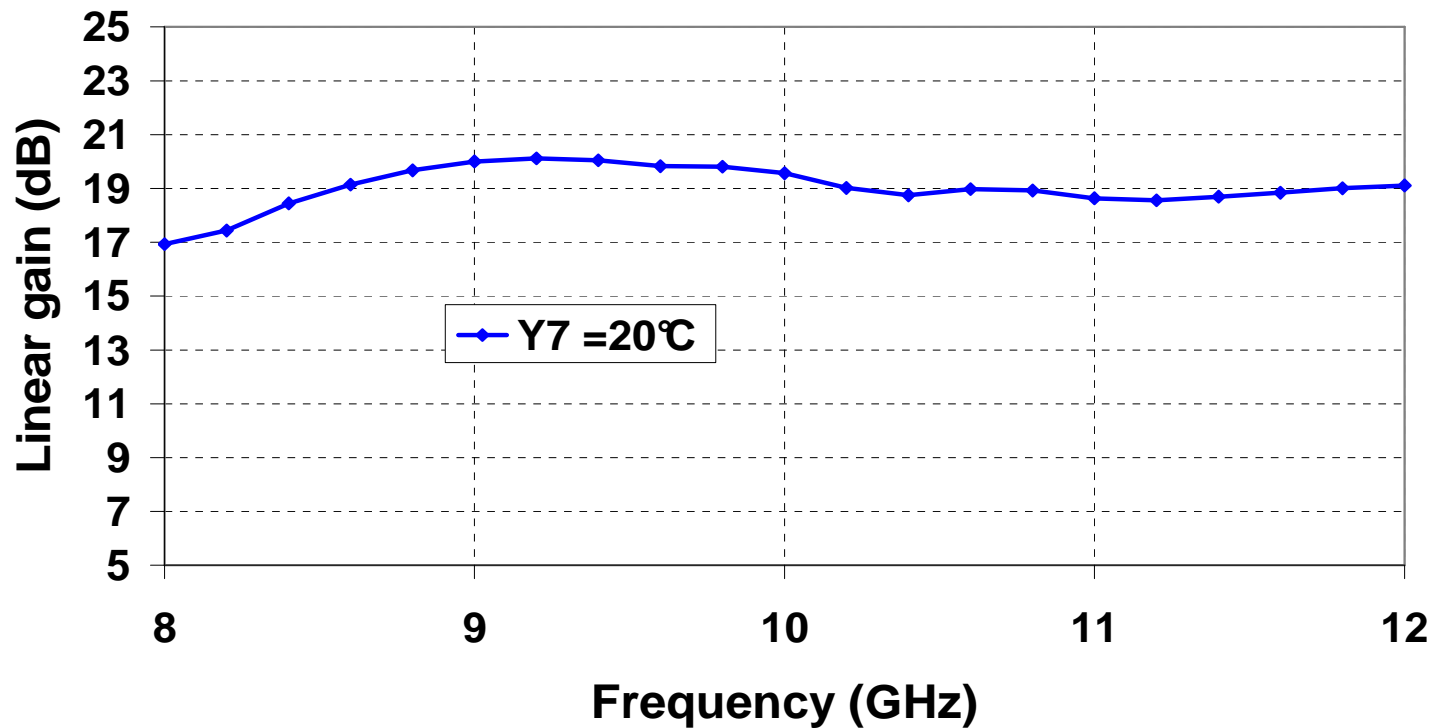


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# 2-stage HPA: measurements

## Linear Gain vs Temperature

Pulsed drain measurements: 8V  
Quiescent current= 2A  
Pulse width= 100 $\mu$ s  
Duty cycle= 30%

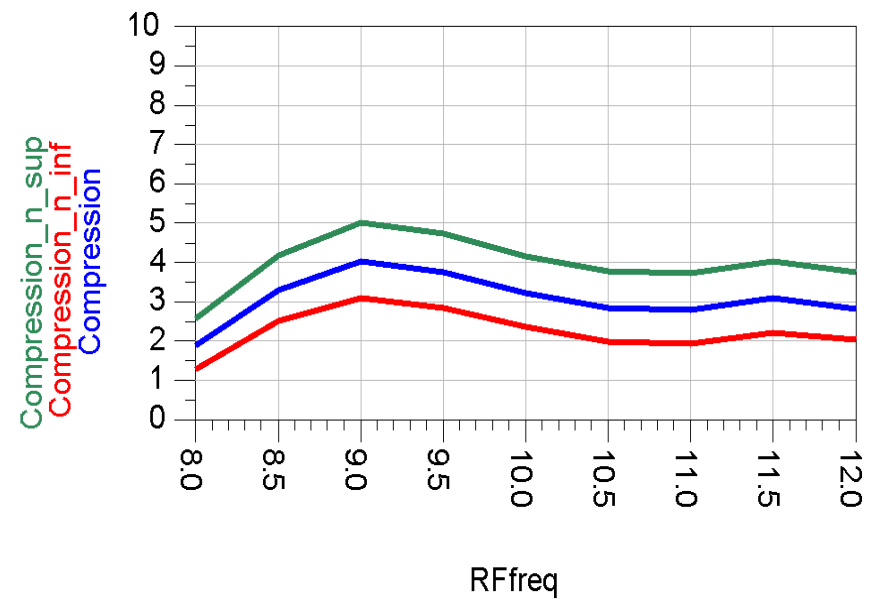
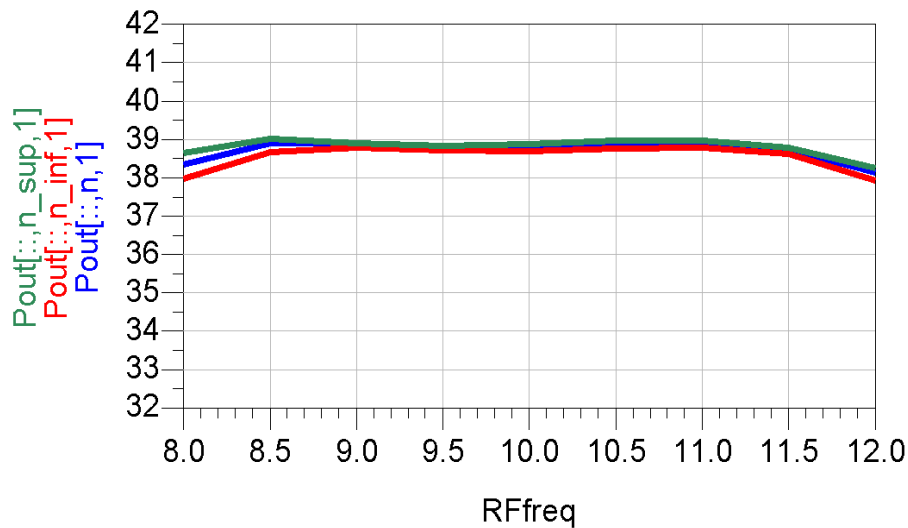


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# 2-stage HPA: simulation with ADS software

## Output Power for 3dB comp. vs Pin

Drain measurements: 8V  
Quiescent current= 2A

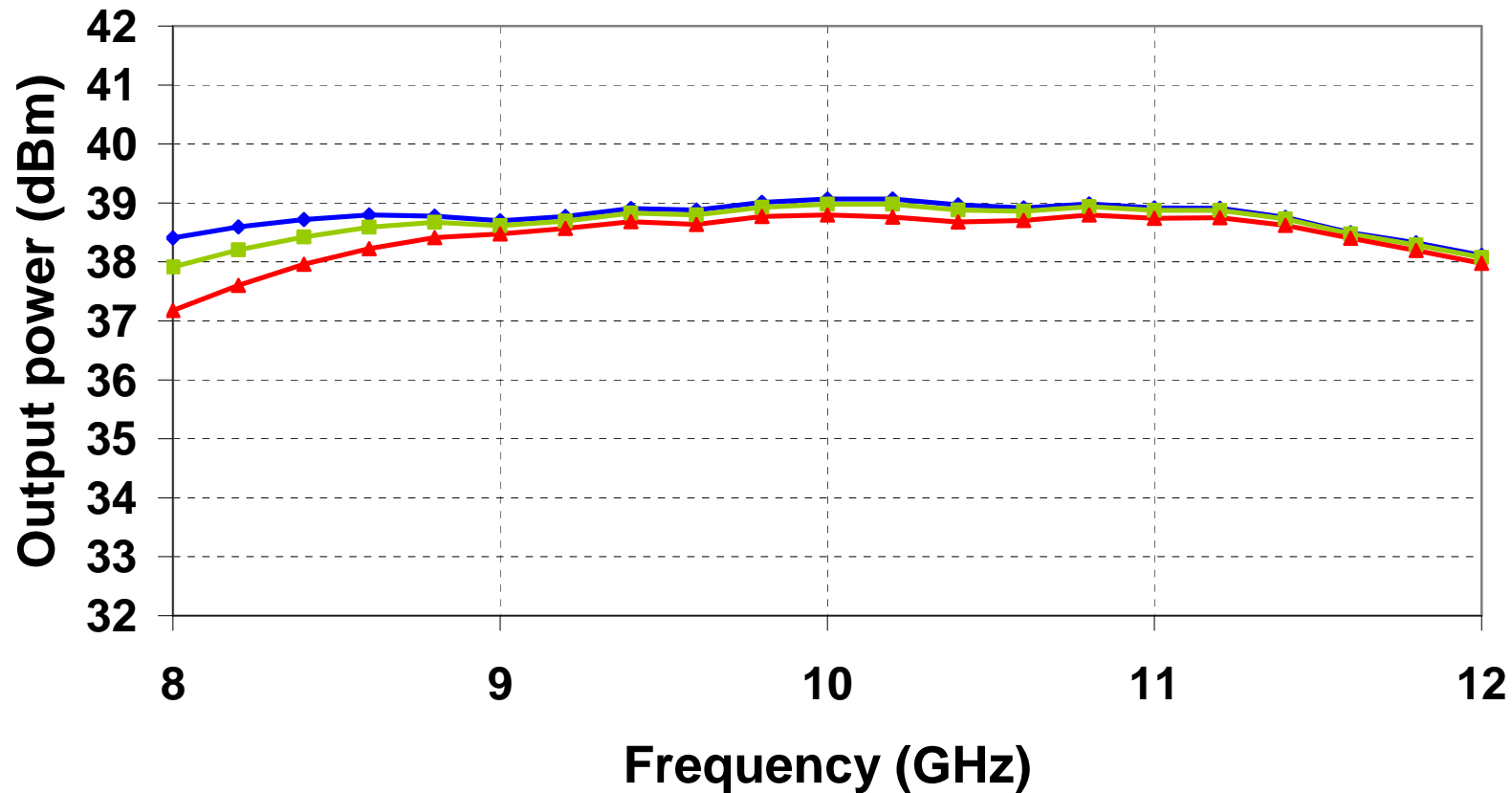


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# 2-stage HPA: measurements

Output Power for 3dB comp. vs Pin

Pulsed drain measurements: 8V  
Quiescent current= 2A  
Pulse width= 100µs  
Duty cycle= 30%

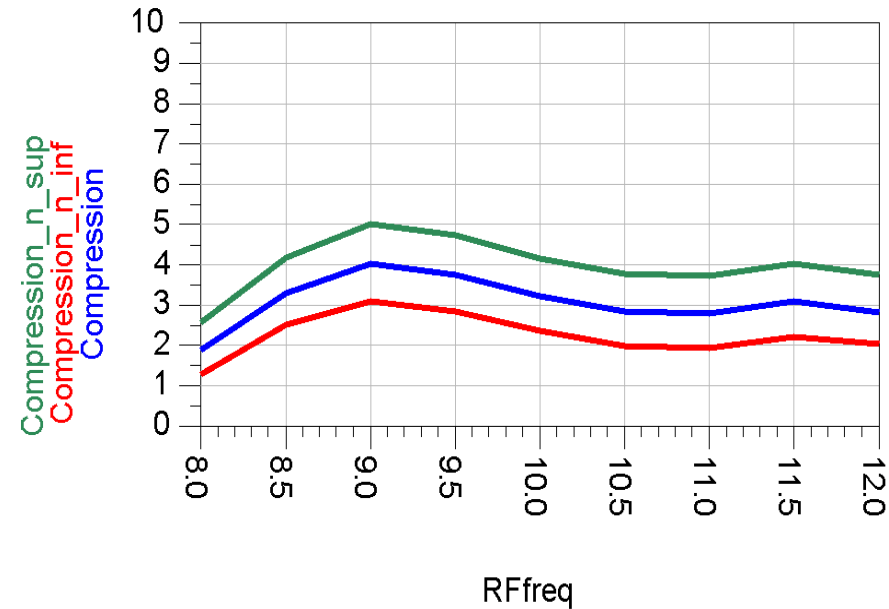
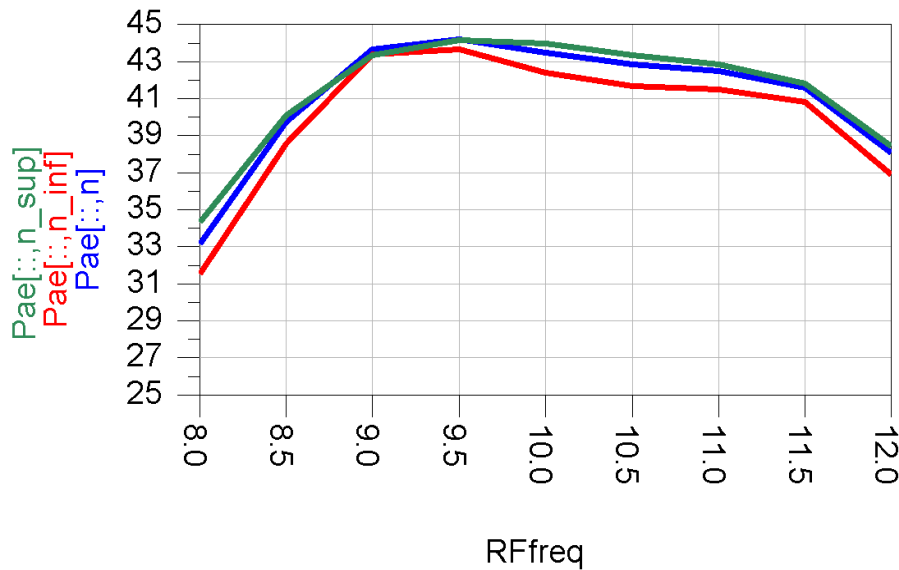


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# 2-stage HPA: simulation with ADS software

PAE for 3dB comp. vs frequency  
@+20°C

Drain voltage= 8V  
Quiescent current= 2A

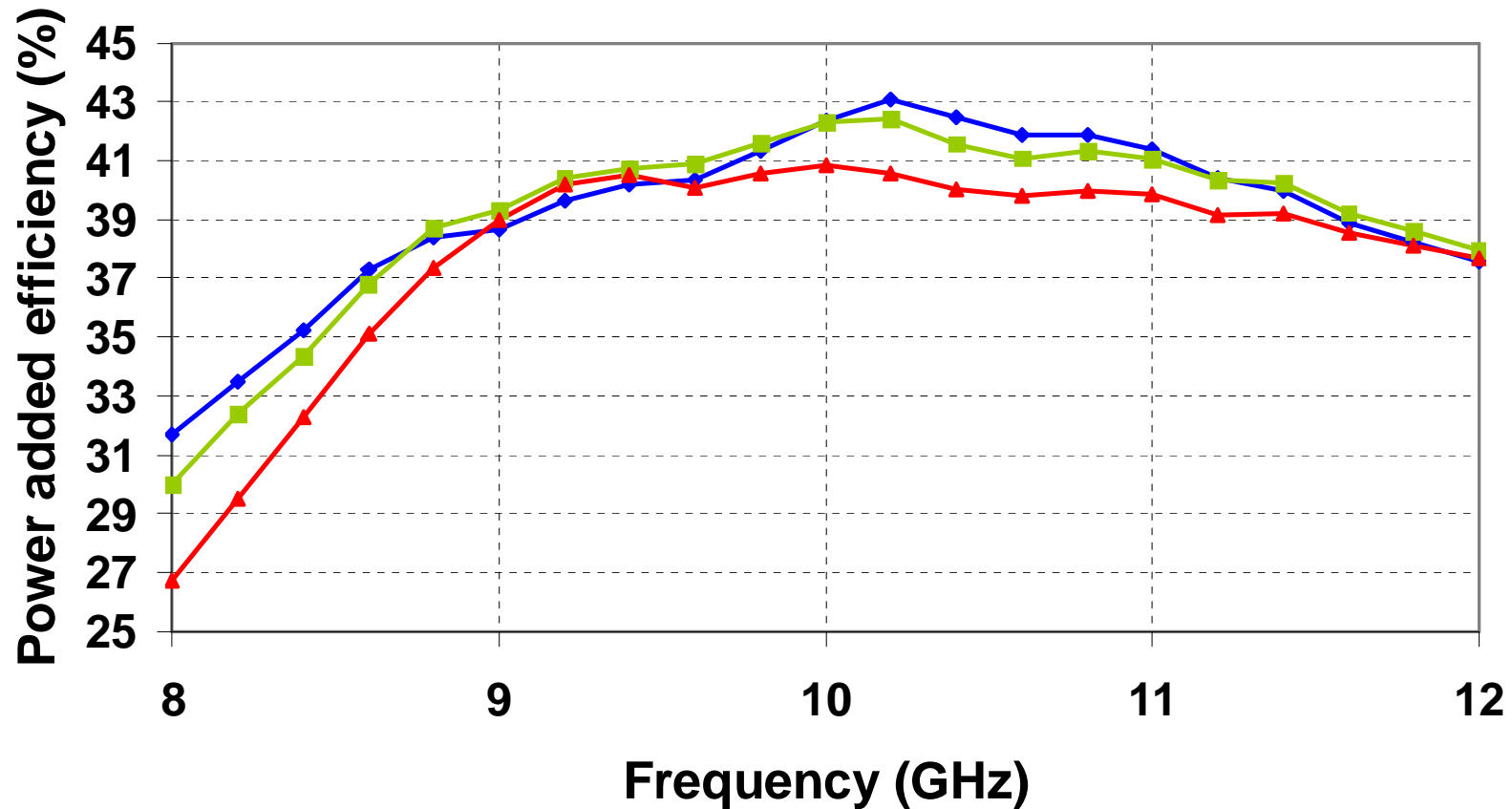


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# 2-stage HPA: measurements

PAE for 3dB comp. vs Pin

Pulsed drain measurements: 8V  
Quiescent current= 2A  
Pulse width= 100μs  
Duty cycle= 30%

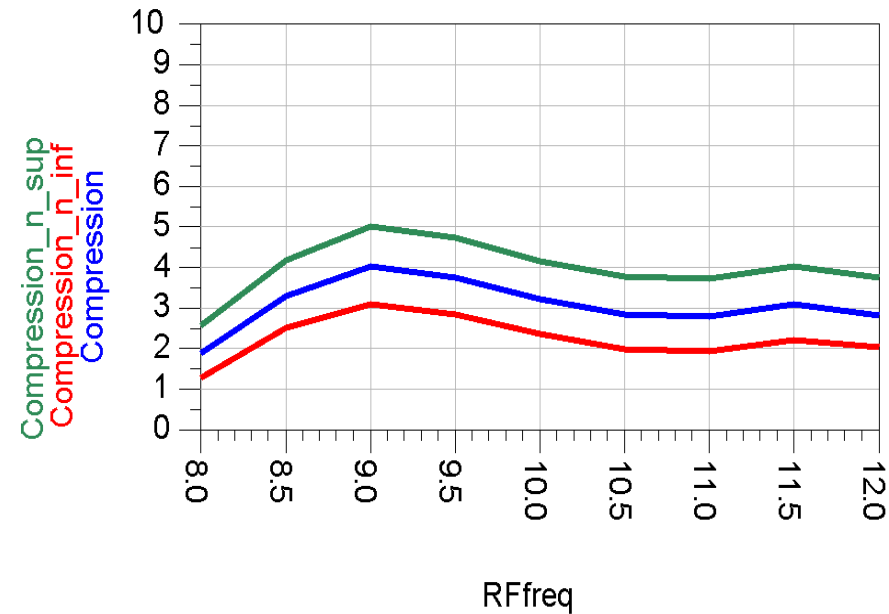
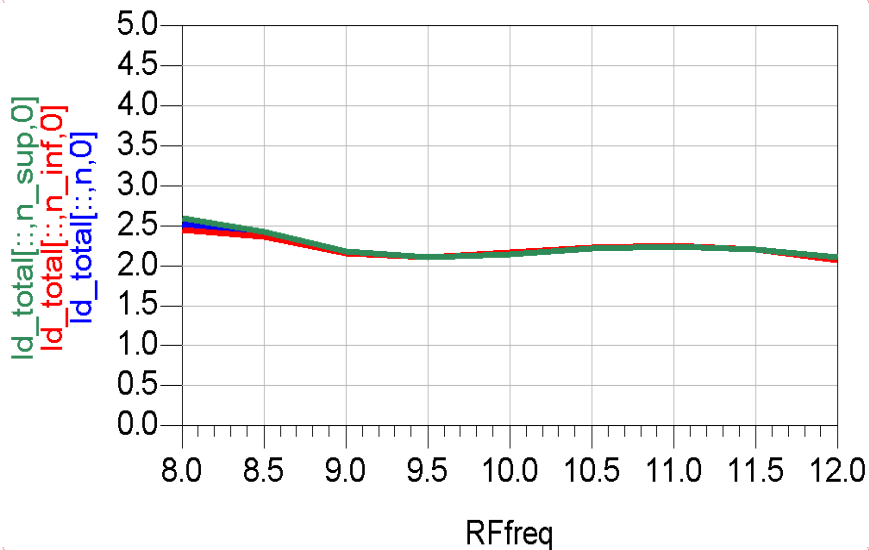


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# 2-stage HPA: simulation with ADS software

Id for 3dB comp. vs frequency  
@+20°C

Drain voltage= 8V  
Quiescent current= 2A

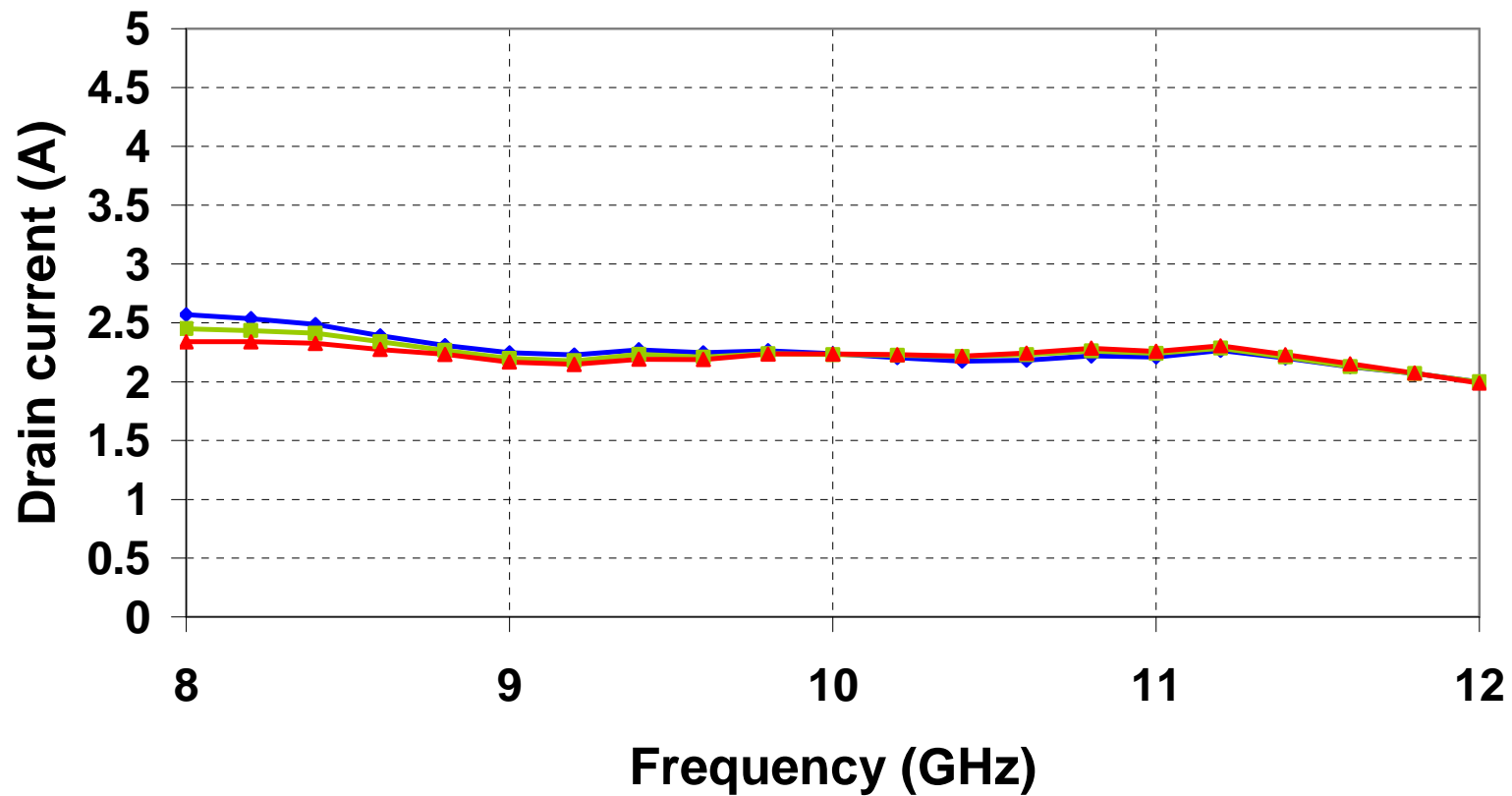


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# 2-stage HPA: measurements

**Id for 3dB comp. vs Pin**

Pulsed drain measurements: 8V  
Quiescent current= 2A  
Pulse width= 100µs  
Duty cycle= 30%



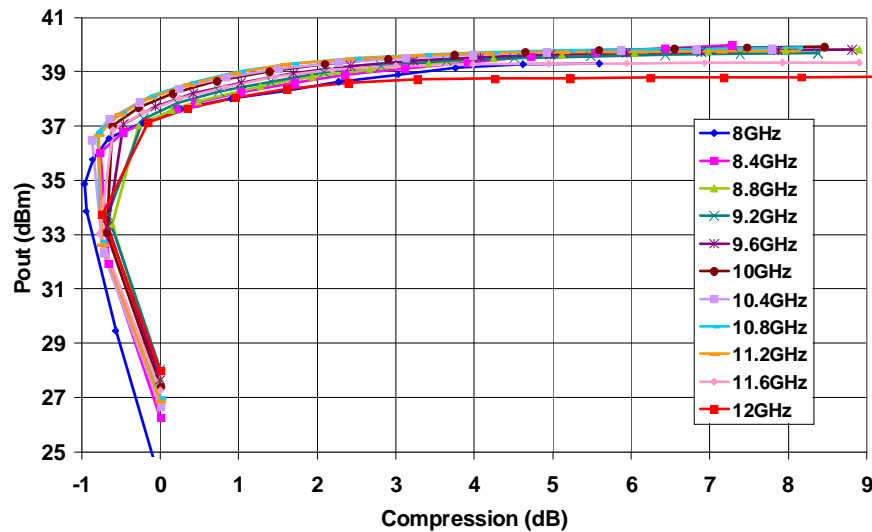
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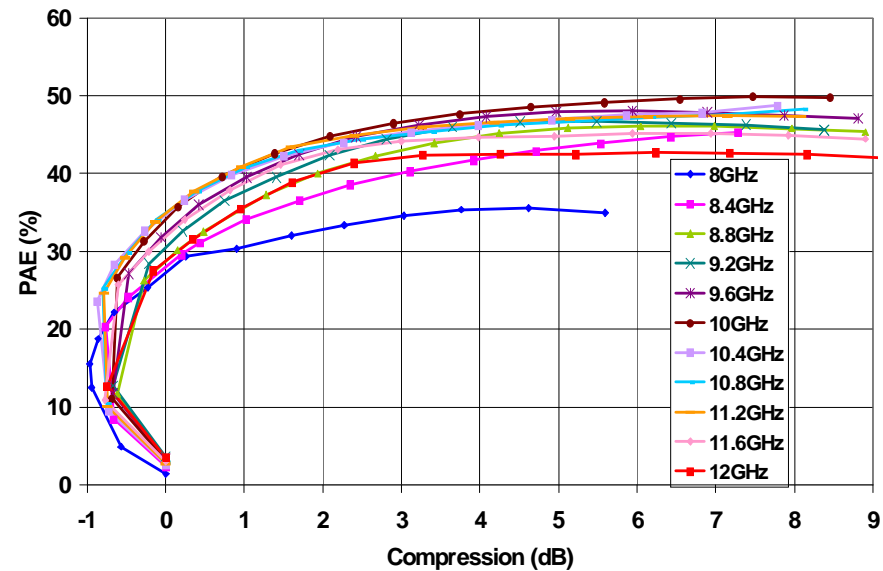
# 2-stage HPA: measurements

**Output power @20°C  
vs compression**

Pulsed drain measurements: 8V  
 Quiescent current= 2A  
 Pulse width= 25μs  
 Duty cycle= 10%



**PAE @20°C  
vs compression**



## Robustness test vs overdrive

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# 2-stage HPA: measurements

## Robustness test in worst cases

### Conditions:

Bandwidth: 8.5-11.5 GHz

→ Drain voltage 8V

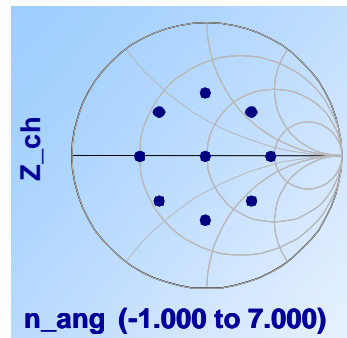
→ VSWR 2:1

→ 8 Phase states

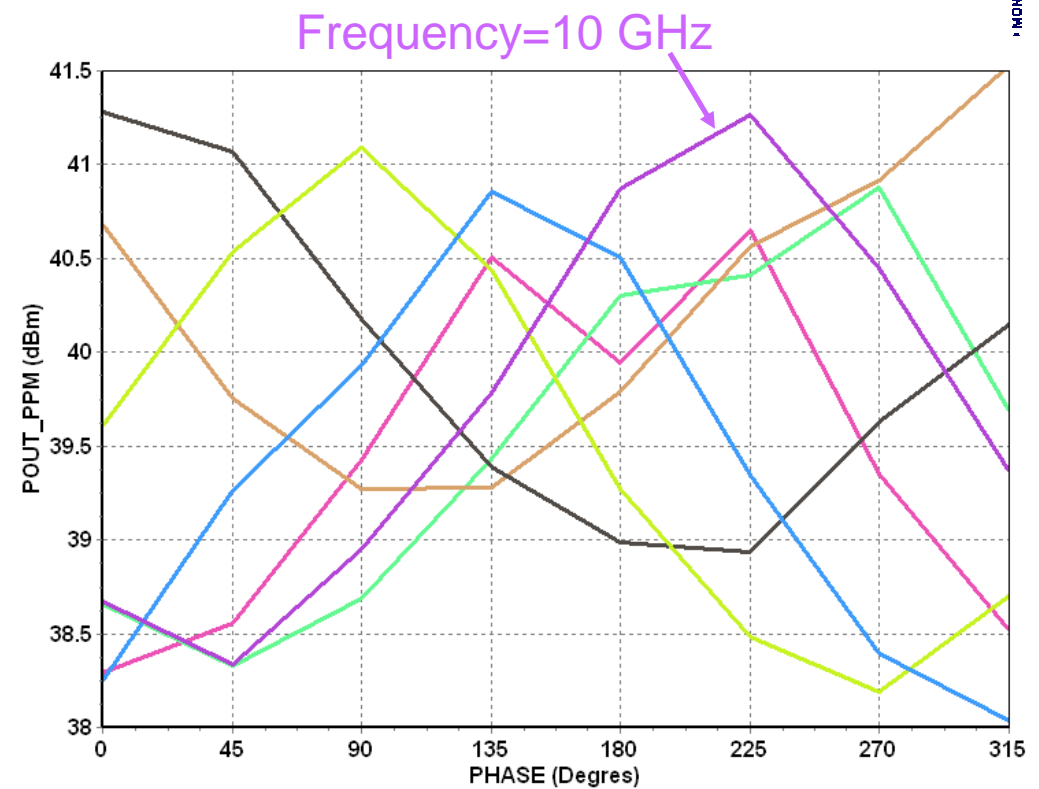
→ Short Pulses

→ - 40°C

→ 6dB gain compression



### Output power vs phase state



No degradation after stress test

# 2-stage HPA: main performances and layout

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## Performances

8.5-11.5 GHz

Small signal gain 19-20dB

Sat. output power: >8W

Sat. PAE: > 40%

## Features

DC Power consumption: 18.4W

Chip size : 4.41x 3.31x 0.07mm

Chip area: 14.6 mm<sup>2</sup>

# Conclusion

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- The development of robust HPAs with high level of PAE and high output power has been presented on about 30% of frequency Band thanks to “Advanced Design System” from AGILENT.
- Based on this good accuracy between simulation and measurements, a new portfolio of HPA is under development
  - C Band , Pout >10 W , PAE=40%
  - X Band, Pout >10 W, PAE=40%

# Thanks

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**Thank you for your attention**

**Any question ?**

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