ADS USERS' GROUP MEETING

A 8W, High efficiency X-band Power PHEMT amplifier designed with ADS Agilent software

June 16, 2009

T. Huet, C. Byl, V. Serru

UMS is a company of THALES and EADS
UMS SAS: Rte dépt. 128, BP46, 91401 ORSAY Cedex, FRANCE
*__UMS GmbH:__ Wilhelm Runge Strasse 11, 89081 Ulm, GERMANY

Outline

- Motivation
- ADS AGILENT software & UMS design kits
- Considerations on HPA
- UMS PPH25X technology
  - Transistors characterization
- Design methodology
- 2-stage HPA
  - Harmonic Balanced Simulations (standard + 3D planar)
  - Measurements
  - Main performances and layout
- Conclusion

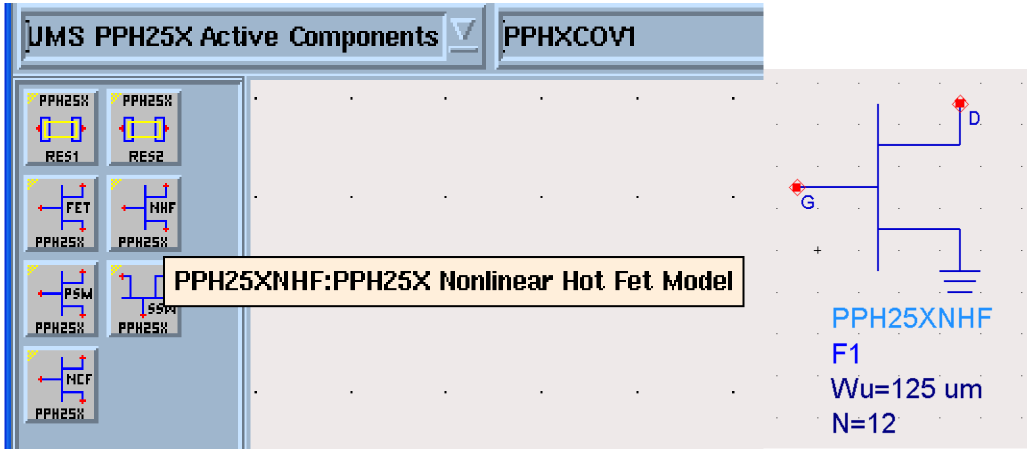
Motivation

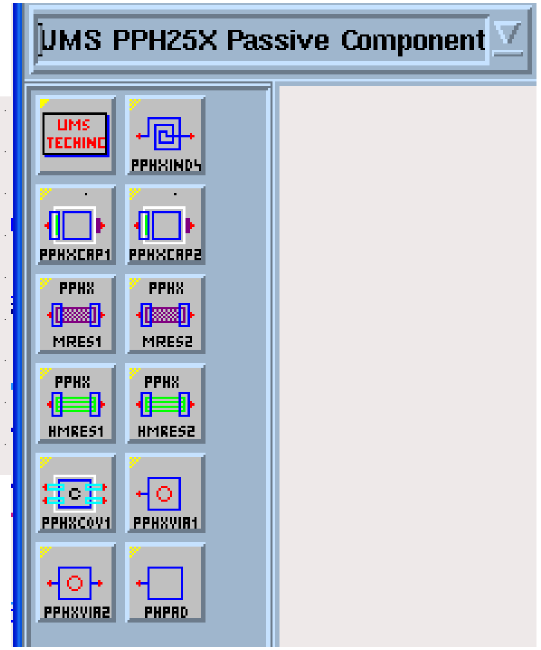
Monolithic Microwave Integrated Circuits HPAs based on Gallium Arsenide are dedicated to T/R modules for Phased Array radars. Very high efficiency and high power are required for these X band applications.

The design goal was to demonstrate that the UMS Power PHEMT technology (PPH25X) enables the generation of robust HPAs using the “Advanced Design System” software from Agilent.

Agilent Software

- **Available on Agilent Software:**
  - Customized environment
  - Linear and non linear electrical transistor models
  - Passive components electrical models





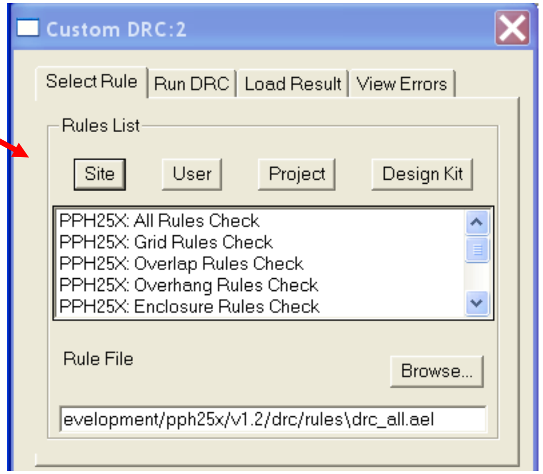
  - Layout macros / Auto-layout enable

- **User's manual and installation guide**

Agilent Software

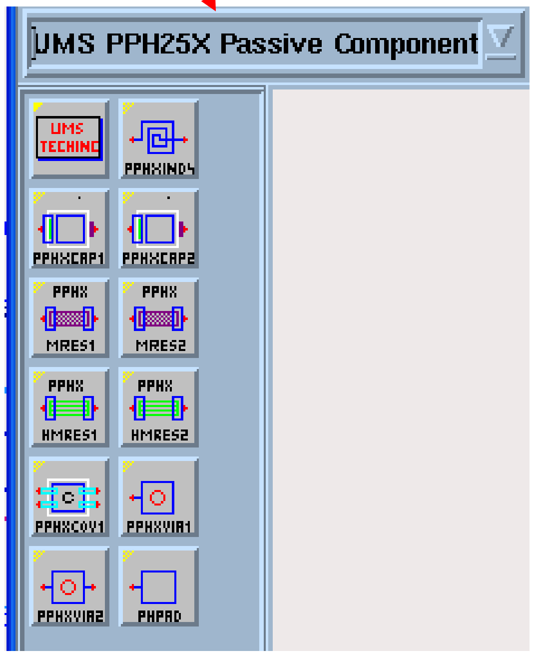
- **New structure for UMS Design Kit since ADS2003:**
  - Based on the infrastructure officially supported by Agilent
  - Easy to install (no more system variables to set)

- **New available features:**
  - Dynamically Linked Library (Linux and Windows)
  - Integrated statistical model definition for Monte Carlo analysis
  - Design Rule Checker (DRC)
  - Alphabet layout macro



Agilent Software

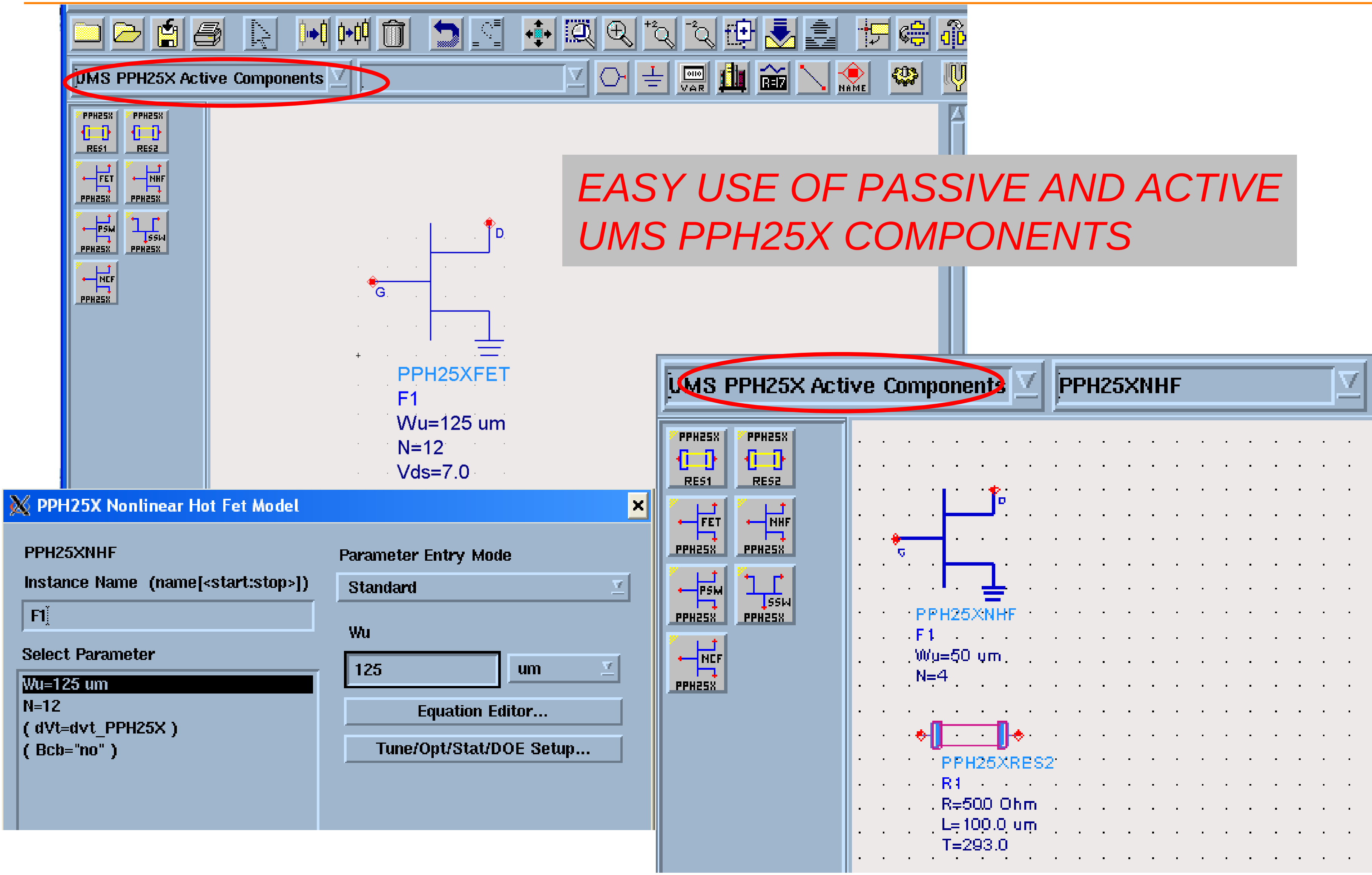
- **Schematic entry:**
  - Components accessible from the library or palette list
  - Specific symbol and bitmap for each component
  - Spread parameters
  - Parameters for physical layout



- **Electrical models:**
  - User defined and C compiled models

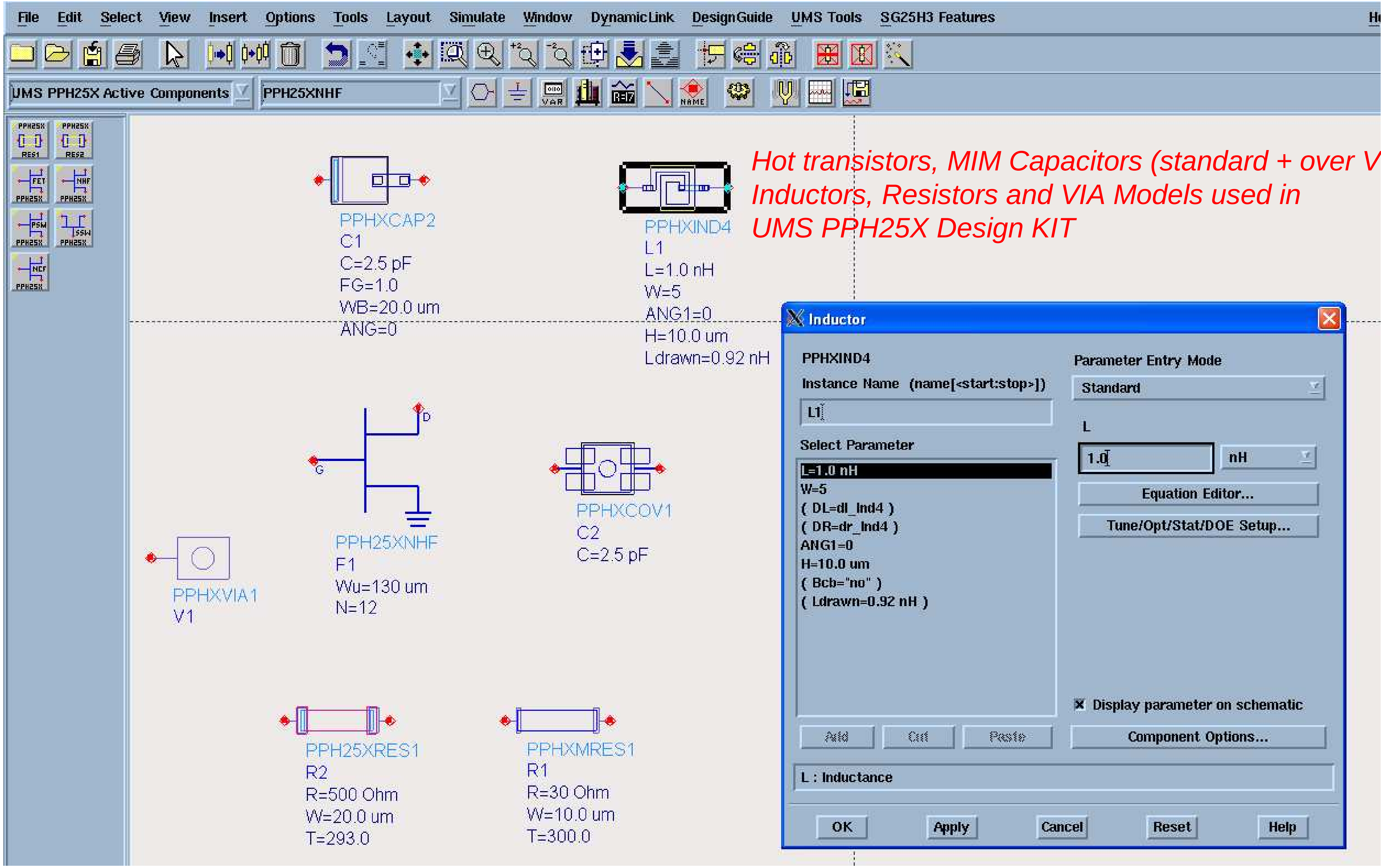
- **Layout macros:**
  - Fixed artwork for RF and DC pads
  - AEL language for all scalable components

Agilent Software dedicated to UMS PPH25X technology



EASY USE OF PASSIVE AND ACTIVE UMS PPH25X COMPONENTS

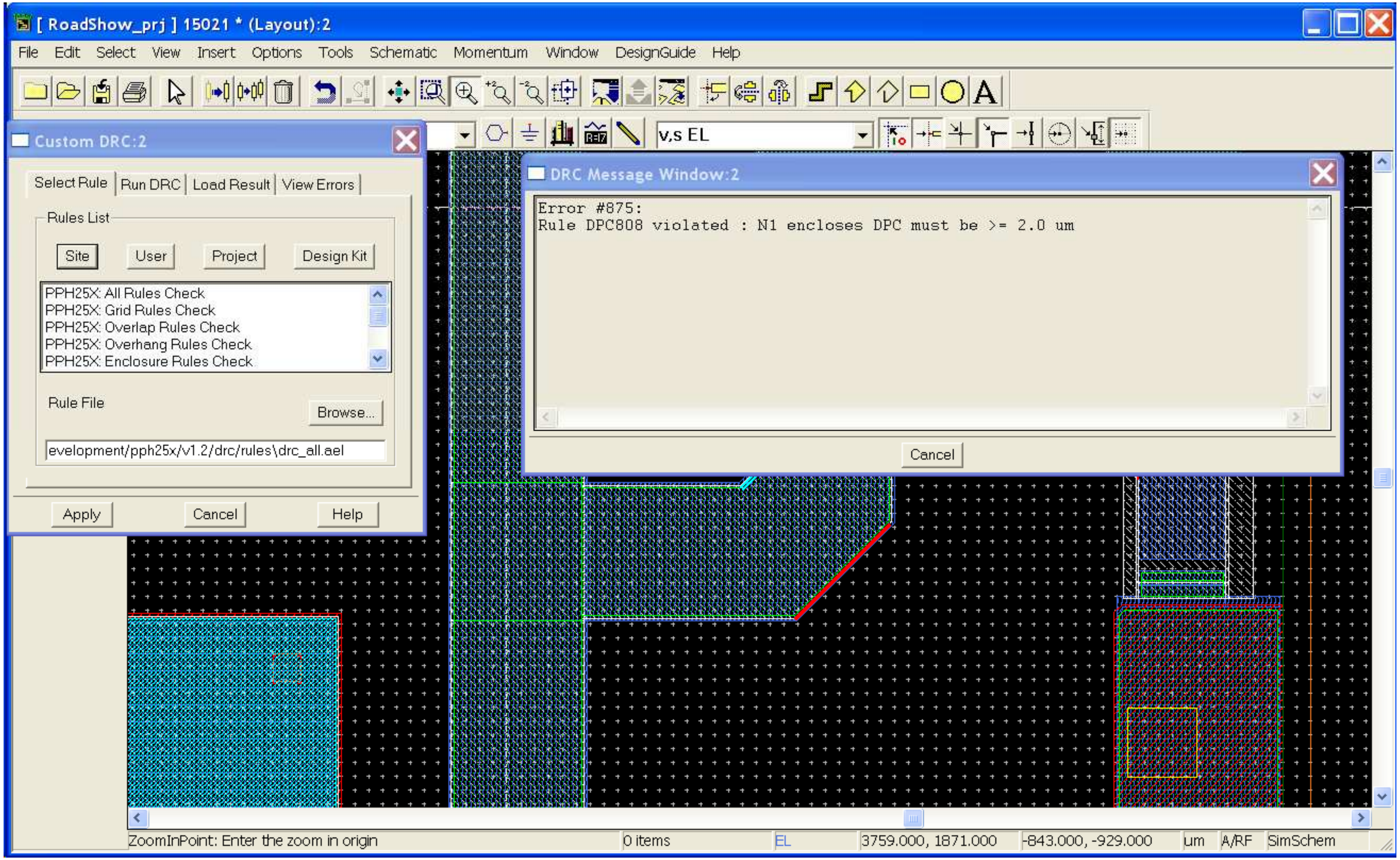
Agilent Software dedicated to UMS PPH25X technology



Hot transistors, MIM Capacitors (standard + over Via) Inductors, Resistors and VIA Models used in UMS PPH25X Design KIT

Agilent Software dedicated to UMS PPH25X technology

UMS PPH25X Design KIT: Design Rules Checking available

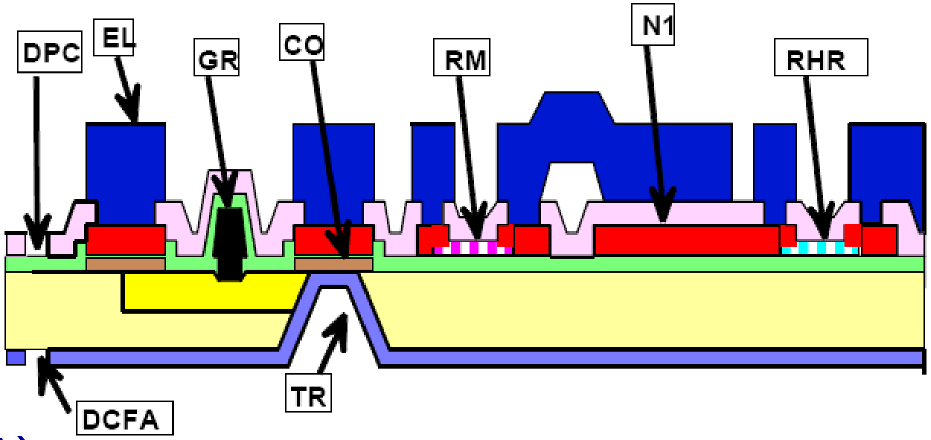


APPLICATION TO THE DESIGN OF A HIGH POWER AMPLIFIER

June 16, 2009

UMS PPH25X Technology

MAIN FEATURES



- Space evaluated technology (ESA)
- Double recess 0.25 µm gate length
- High power density (0.85W/mm)
- High gain (16dB at 10 GHz for power cell 12X130µm)
- High breakdown voltage (Vbds ~ 20 V)
- Over vias MIM Capacitors
- 70 µm substrate thickness with small via-holes

Transistors Characterisation

- **In order to reach good performances at HPA level, a good knowledge of the transistors is required.**

- **Transistors accuracy is based on standard measurements:**

➔ **S parameters measurements:**

➔ **Pulsed I-V measurements:**

➔ **Load pull measurements:**

- To define transistor optimum loads for output power, PAE and drain current.

Design methodology

- **Class A-B amplifier**

- **Choose the transistor size and optimum load impedance taking into account:**
  - Linear gain, Pout, PAE
  - Frequency band
  - Output mismatch (VSWR=2:1)
  - Safe operating area (robustness)

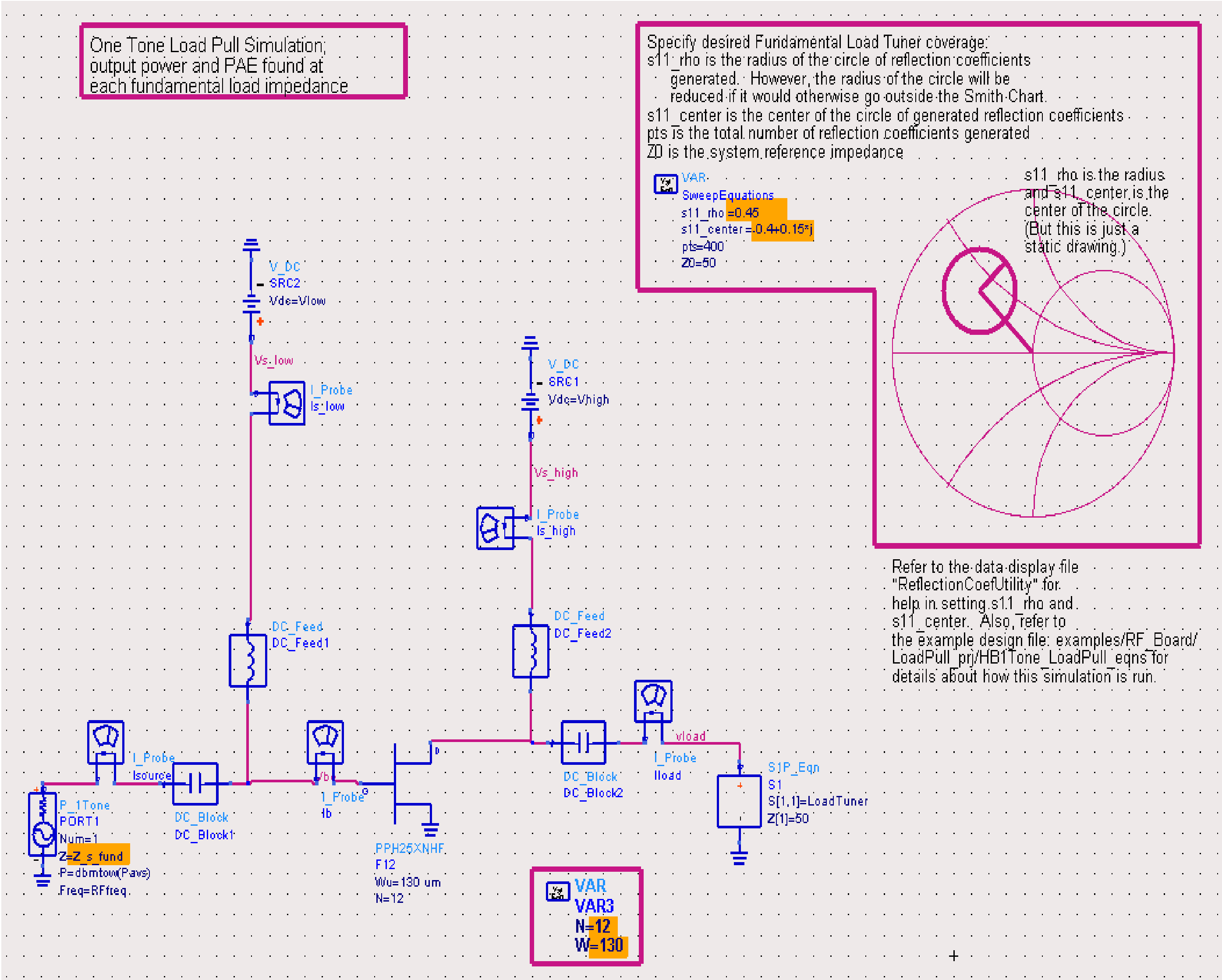
- **HPA matching network (output combiner,…)**

- **Non linear stability analysis (odd and even mode)**

Tools for HPA designs

- **Load pull simulations**
- **Optimization/Tuning**
- **“Standard” simulations**
  - Small signal simulations (S parameters)
  - Harmonic balanced simulations (non linear simulations)
  - Time domain simulations (switching time specifications)
- **EM simulations for passive networks: Momentum simulations to check coupling effects, symmetries and proximities.**
- **Statistics:**
  - Technological spread analysis to check design sensitivity and give expected electrical yields
- **Auto-layout generation and Design Rules Checker**

Transistors selection: Loadpull by simulation

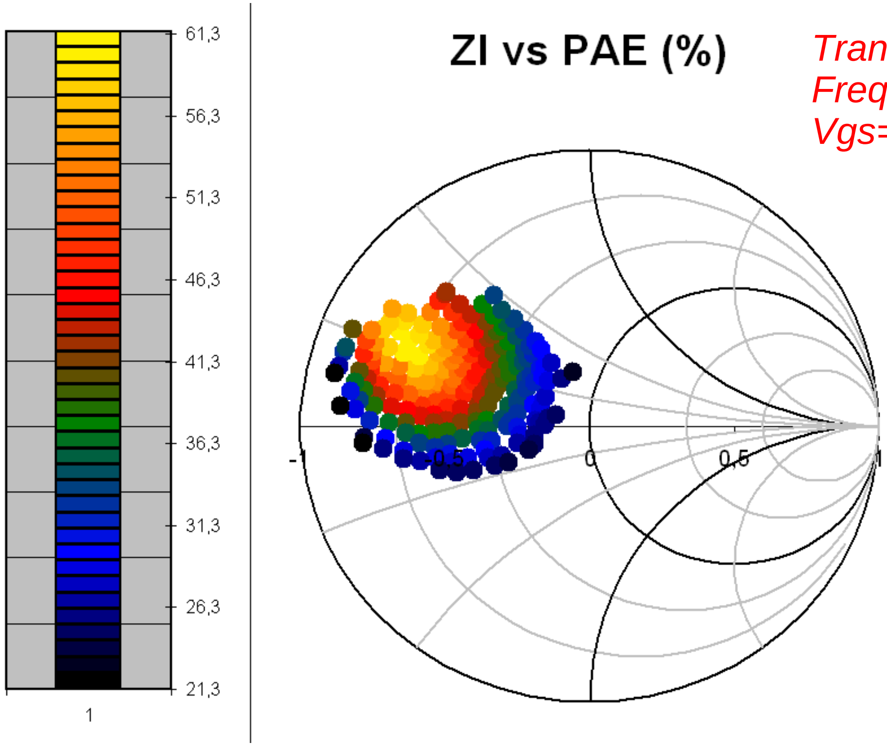


Transistors selection : Loadpull by simulation

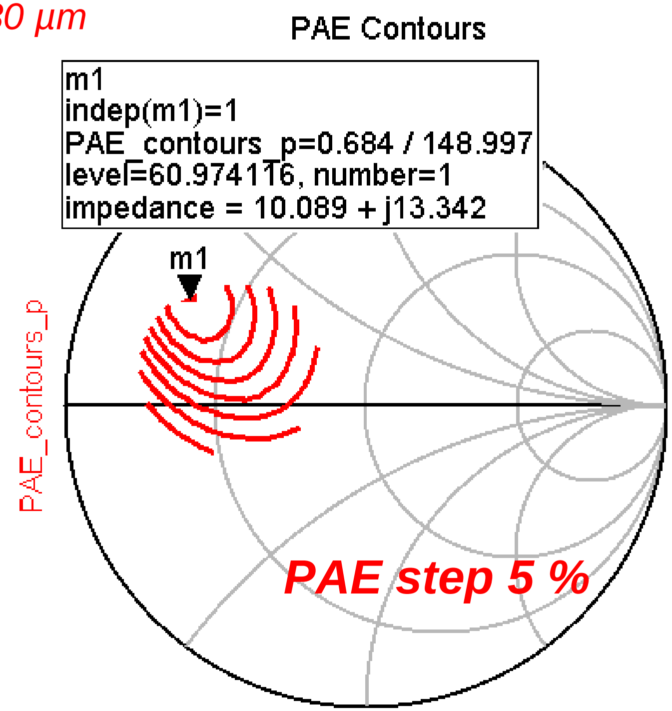
Load pull for PAE contours

Good accordance between Measurements and simulation

Transistor size: 12 x 130 µm
Frequency = 10 GHz
Vgs=-0.35V, Vds=8V



Load pull Measurements
on PPH25X transistor



Simulation with ADS software
using UMS transistor model

Transistors selection

The HPA was developed in the frequency Band: 8.5-11.5 GHz.

- **2-STAGE VERSION**

  Design goal @25°C : Pout>8W, PAE>35%, Linear Gain= 20 dB

  Pulse conditions for drain: 25µs, 10%

  No specifications on linearity

  Chosen topology :

  First stage: 2 power cells (12x130 µm)

  Second stage: 8 power cells (12x130 µm)

2-stage HPA: Combiner optimisation

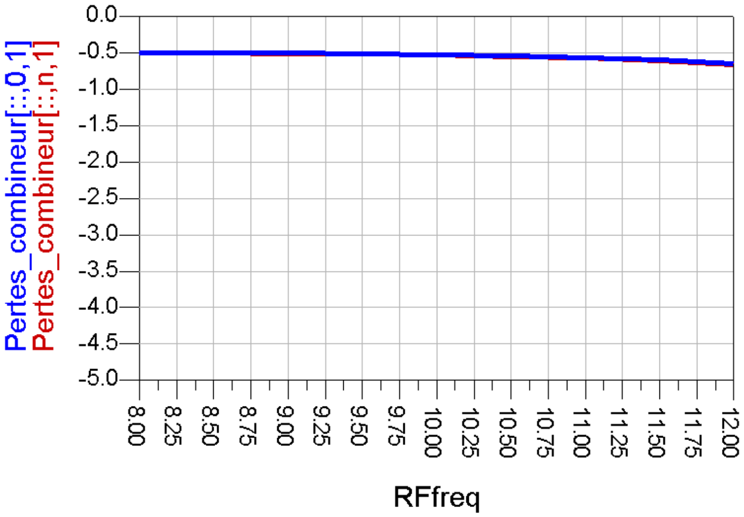
Combiner optimisation

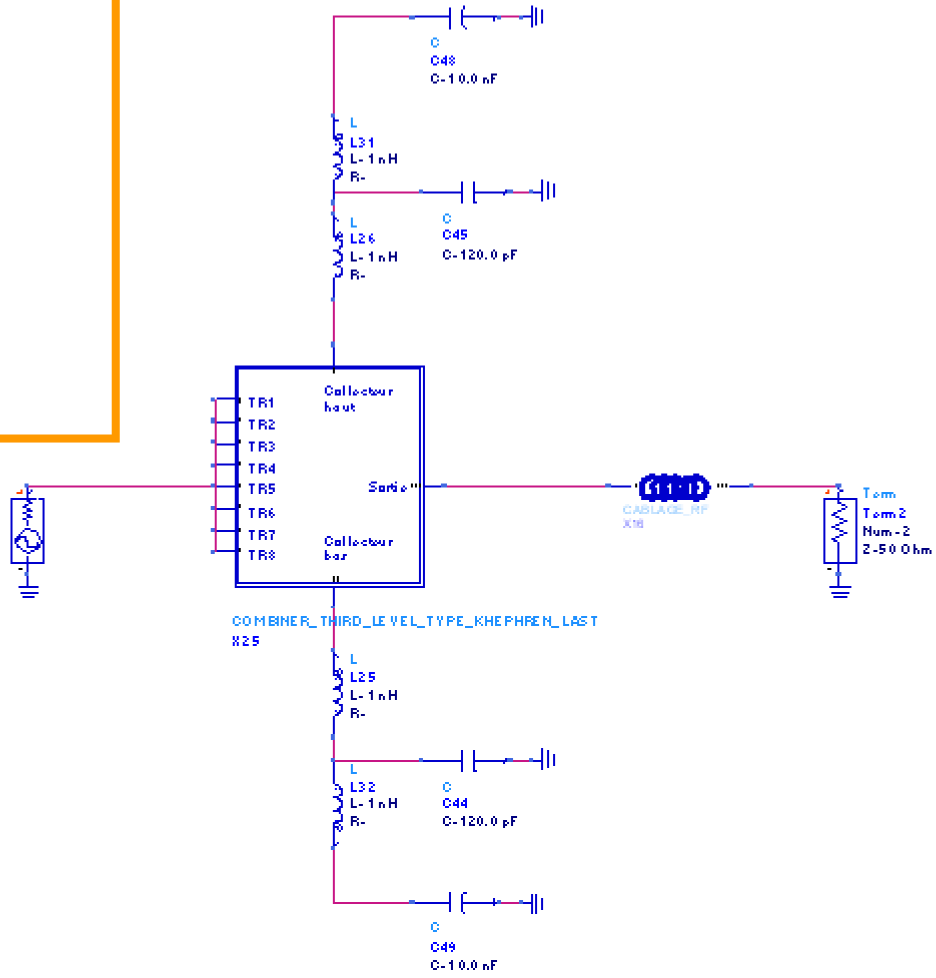
8-12GHz

Low insertion losses

UMS passive components

Agilent microstrip models





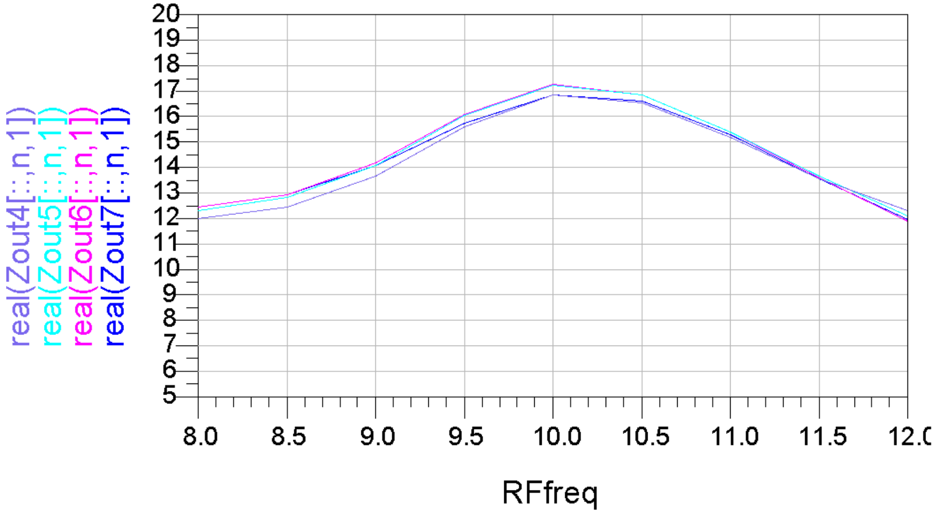
2-stage HPA: Combiner checking

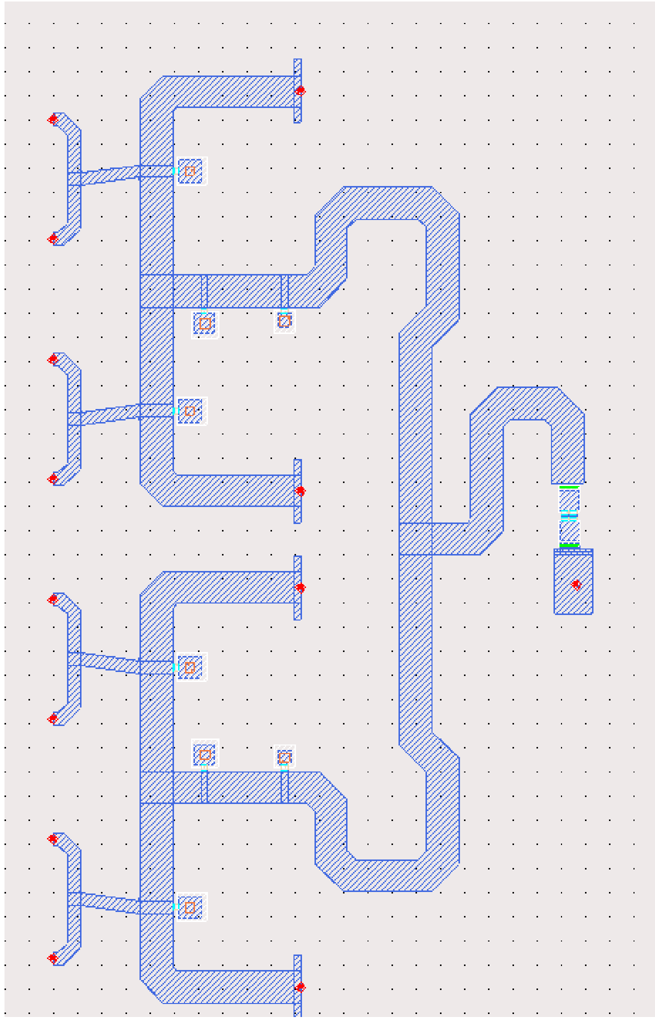
Combiner symmetry

8.5-11.5GHz

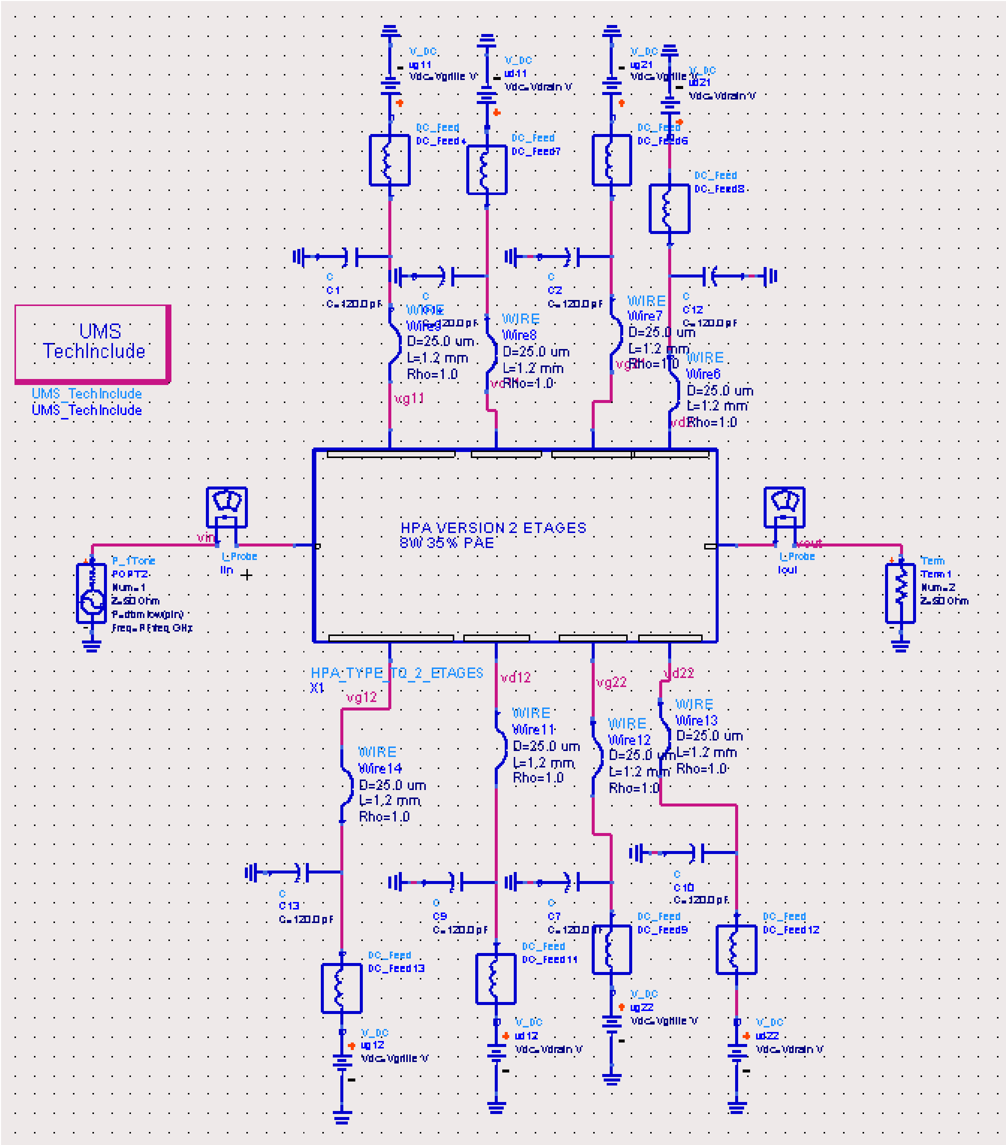
Low insertion losses

Agilent 3D planar momentum

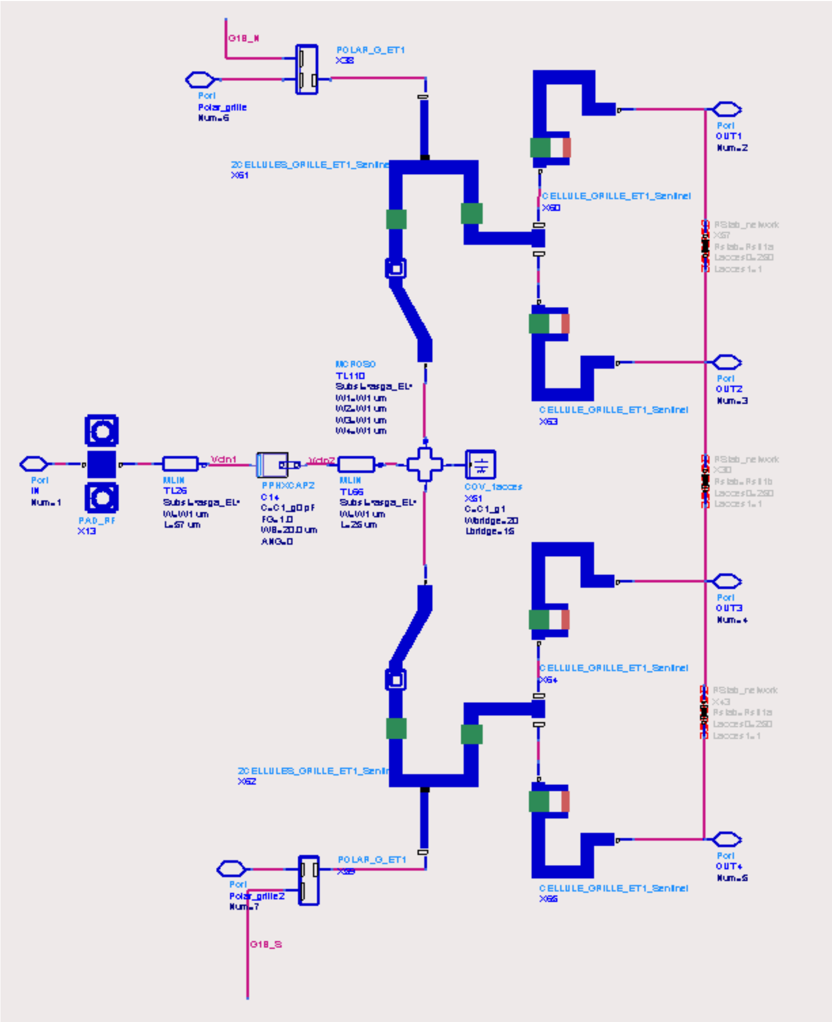




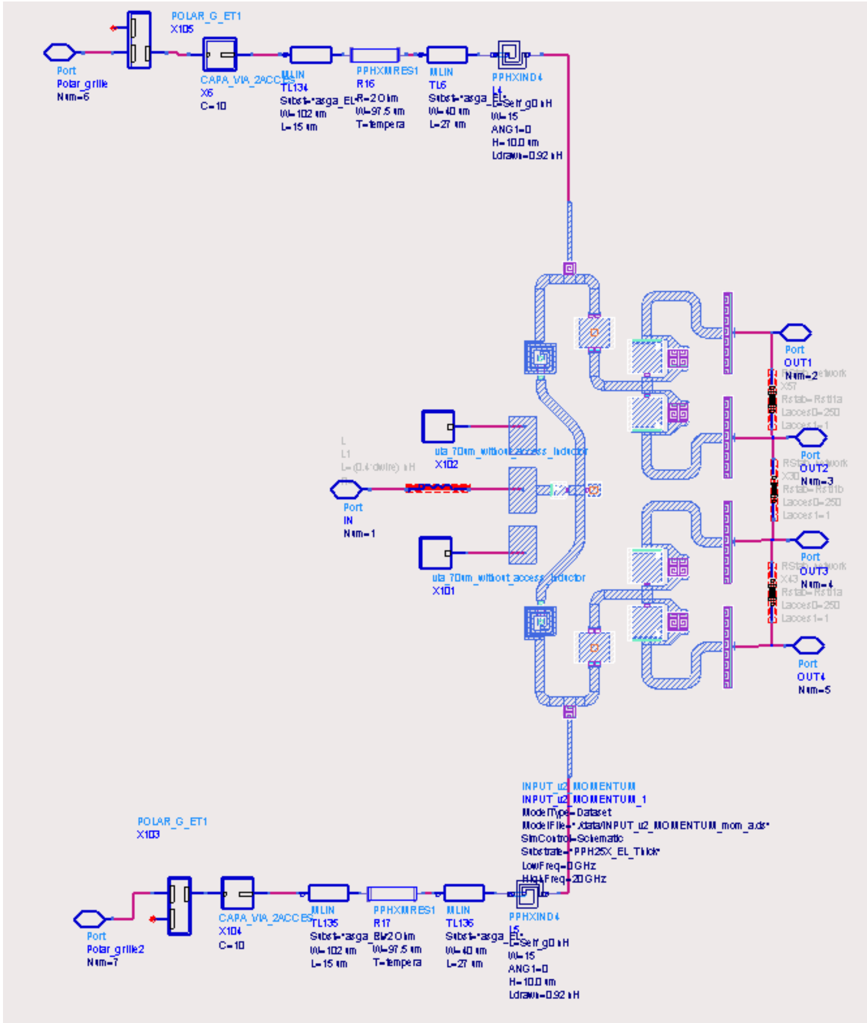
2-stage HPA: simulation with ADS software



2-stage HPA: simulation with ADS software

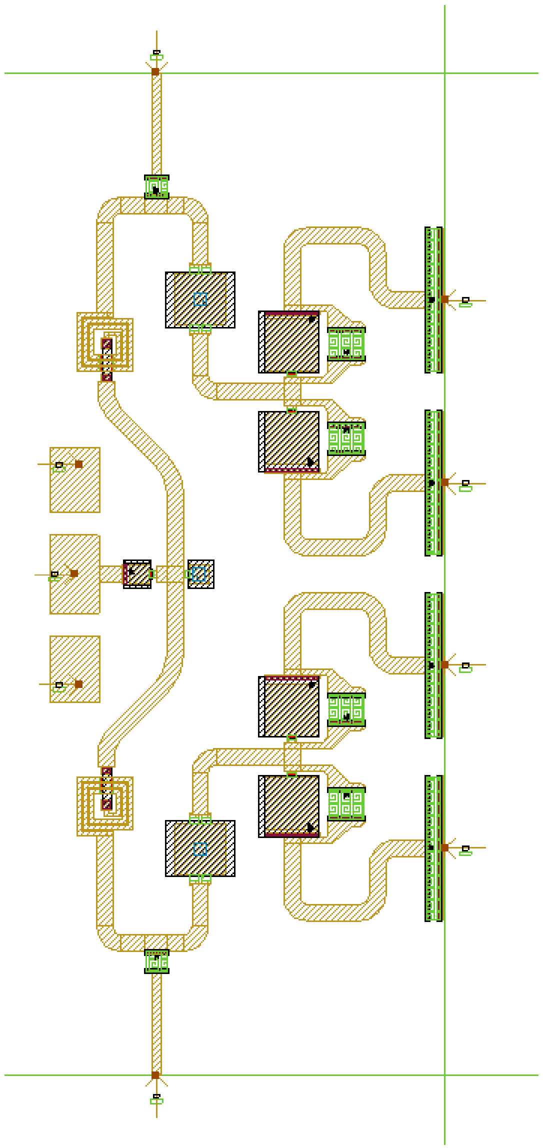


ADS components from UMS PPH25X design Kit and ADS libraries

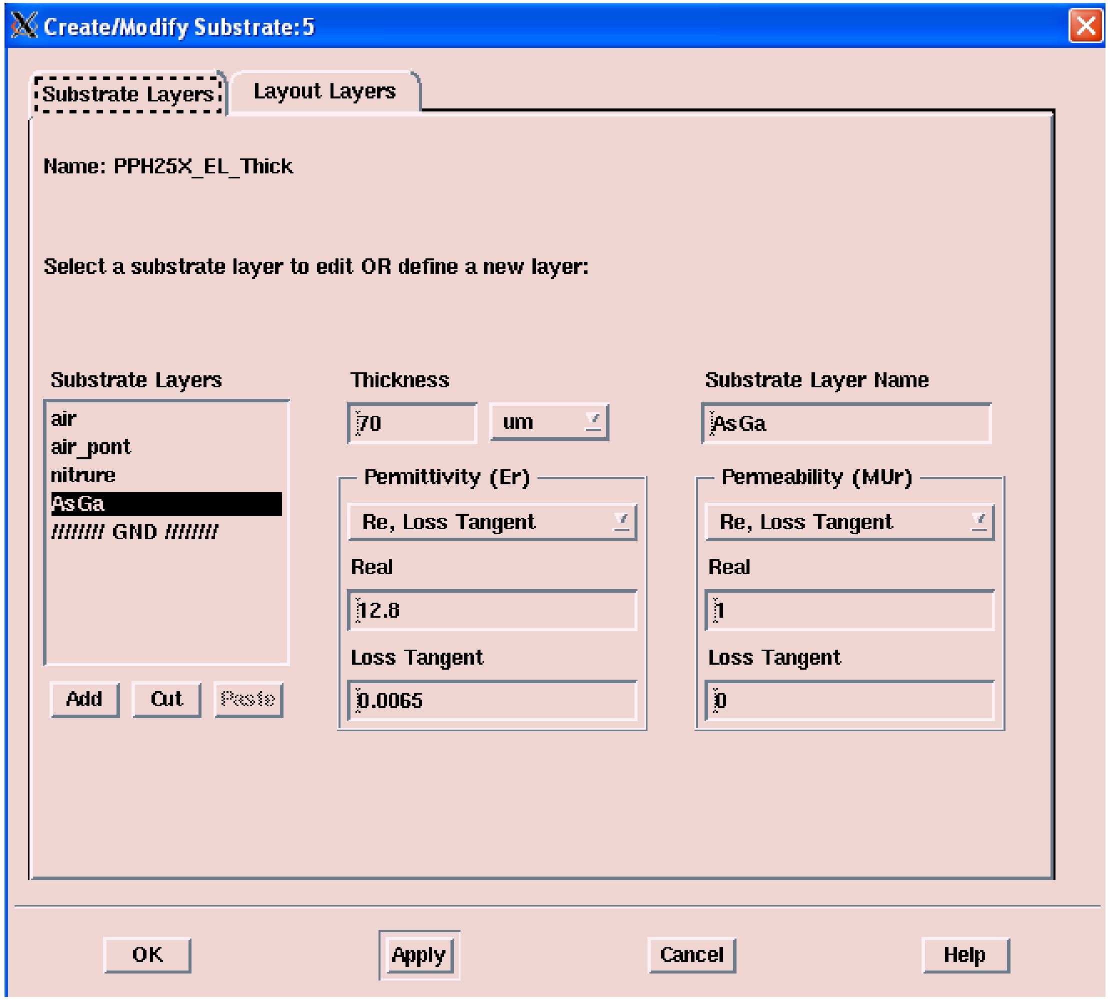


ADS components from UMS PPH25X design Kit and ADS libraries + 3D planar momentum Simulation

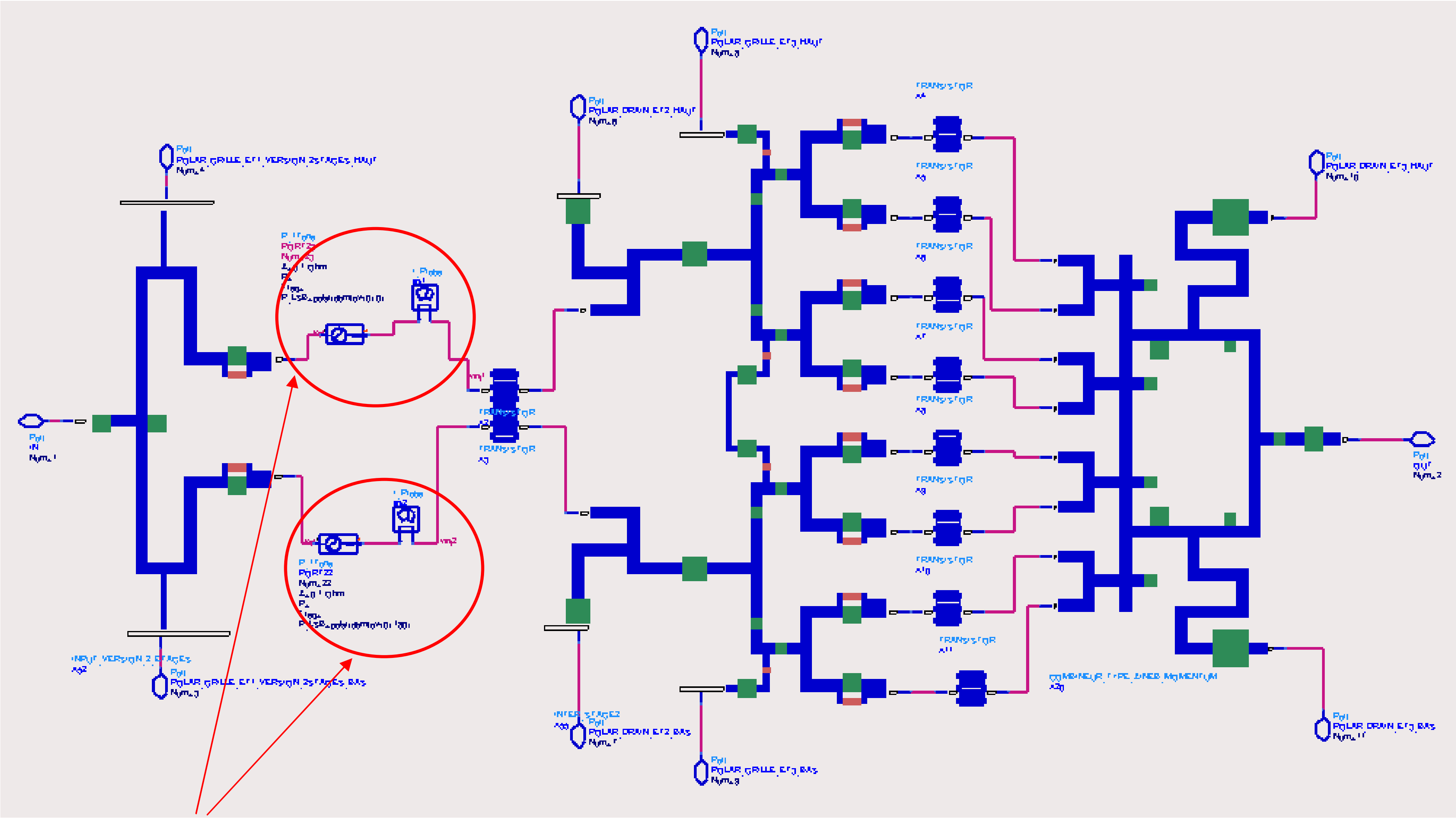
2-stage HPA: simulation with ADS software



3D planar momentum Simulation for Passive Networks:
SUBSTRATE DEFINITION FOR PPH25X TECHNOLOGY



2-stage HPA: Stability analysis



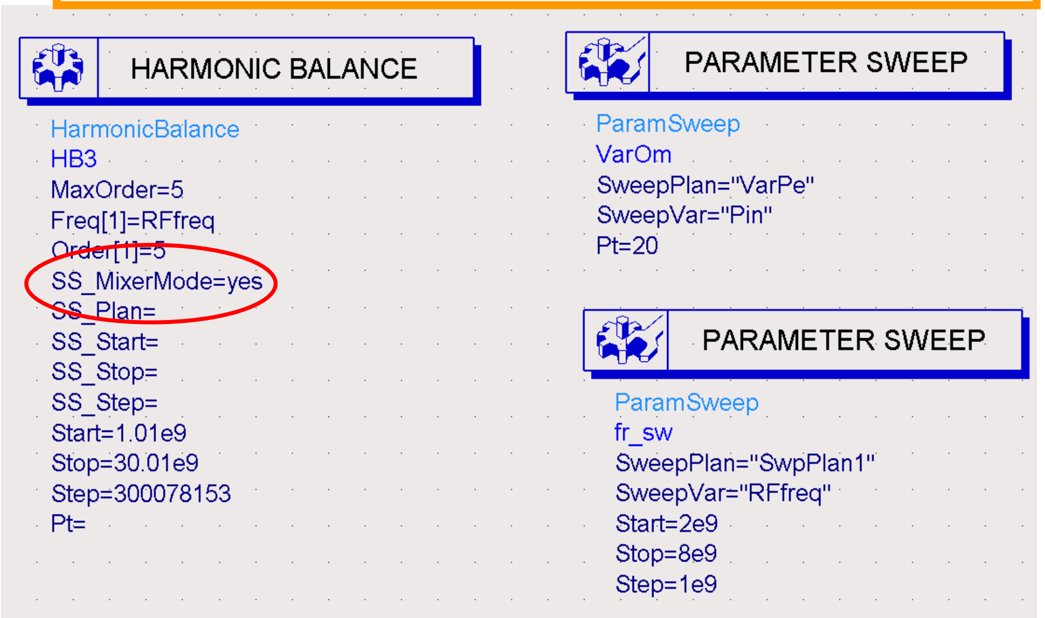
Components used for non linear stability analysis

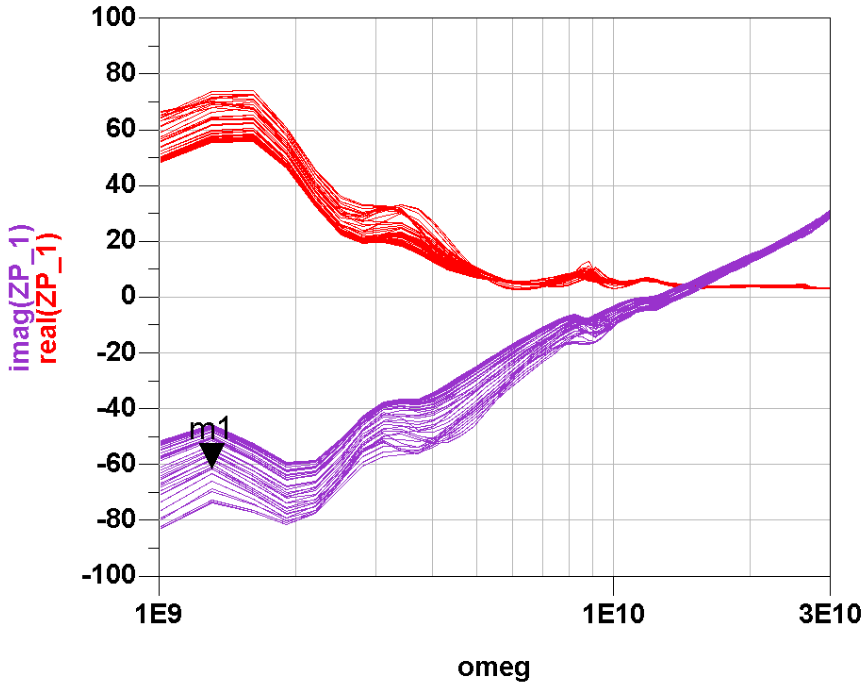
2-stage HPA: Stability analysis

Stability

Wide band stability checking

vs Frequency band & Input power

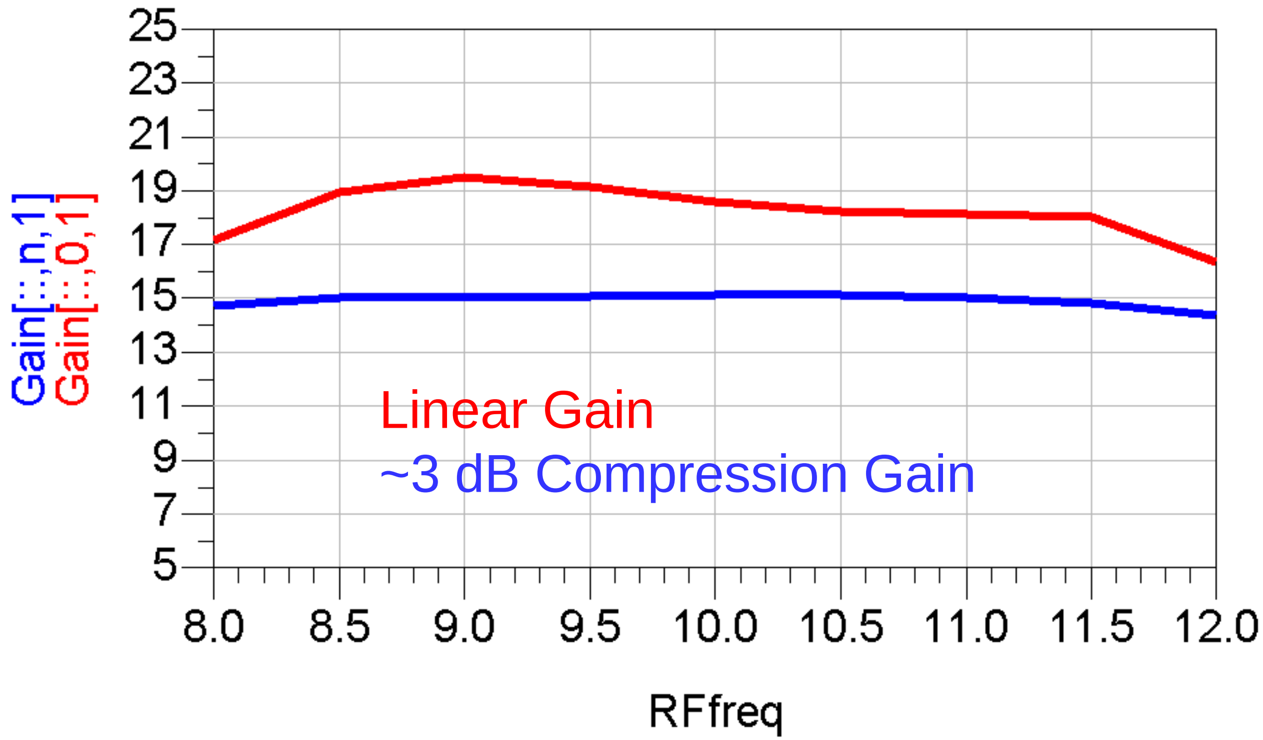




2-stage HPA: simulation with ADS software

Linear Gain and compressed gain @3dB compression vs frequency @20°C

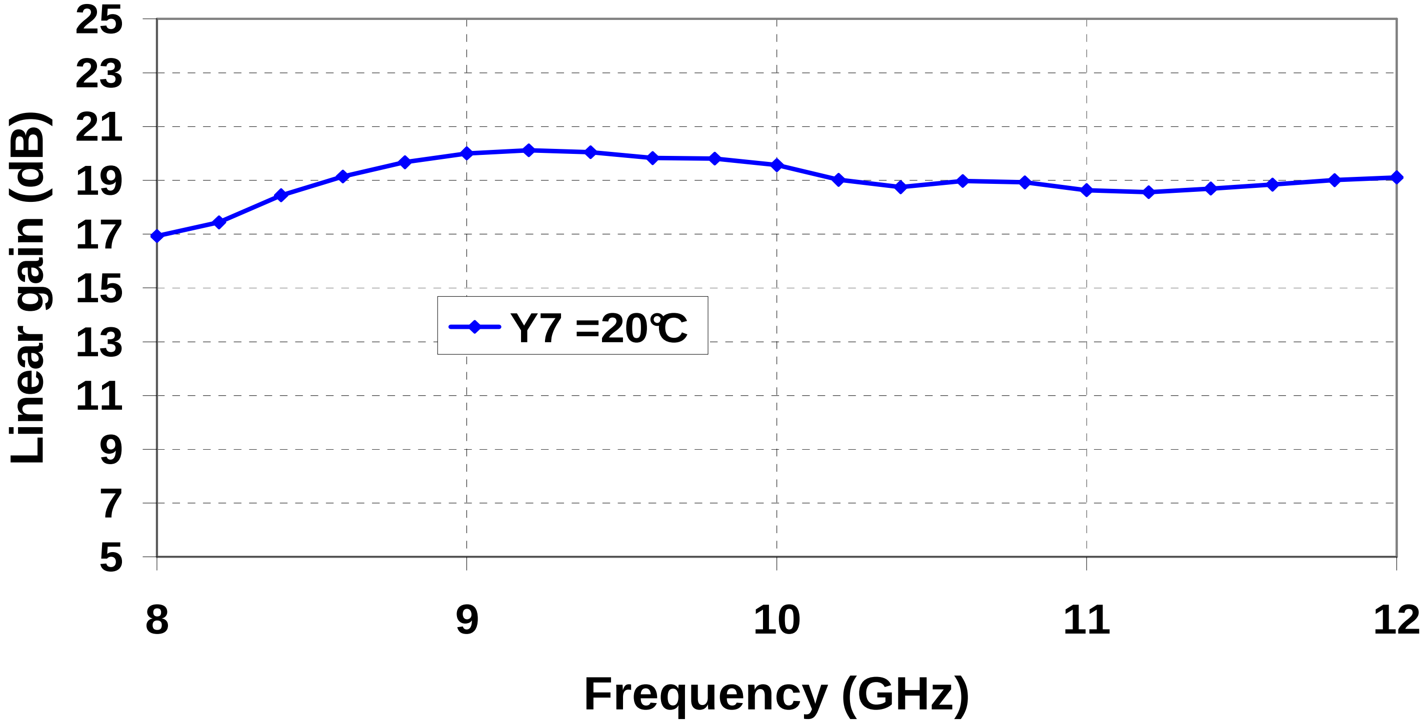
Drain voltage= 8V
Quiescent current= 2A



2-stage HPA: measurements

Linear Gain vs Temperature

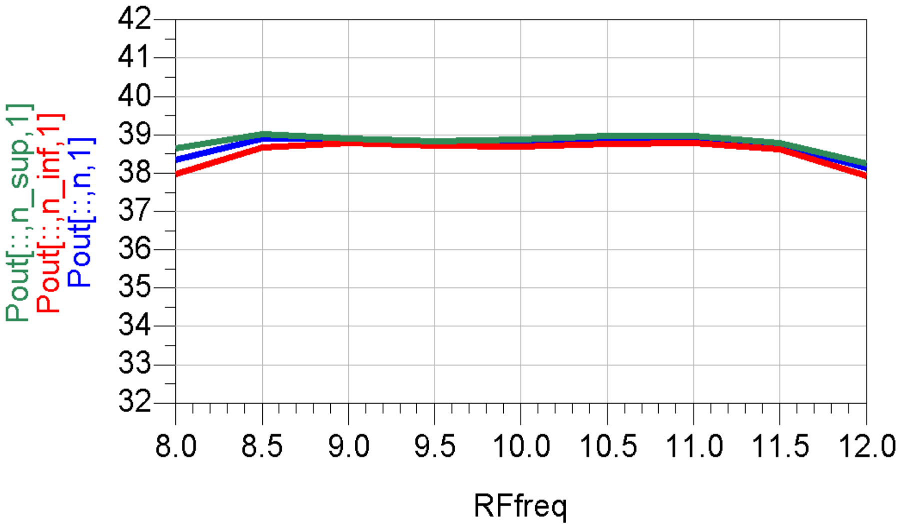
Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 100µs
Duty cycle= 30%

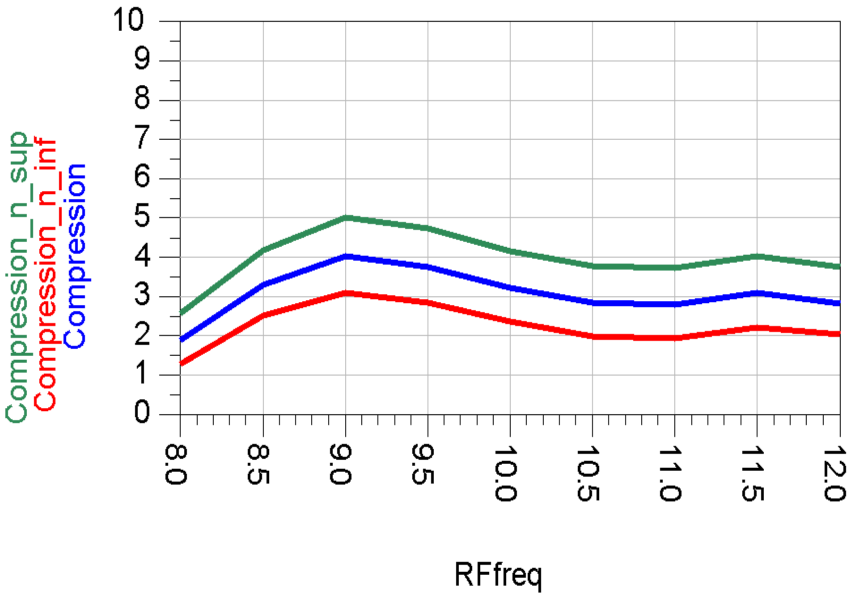


2-stage HPA: simulation with ADS software

Output Power for 3dB comp. vs Pin

Drain measurements: 8V
Quiescent current= 2A





2-stage HPA: measurements

Output Power for 3dB comp. vs Pin

Pulsed drain measurements: 8V
Quiescent current= 2A
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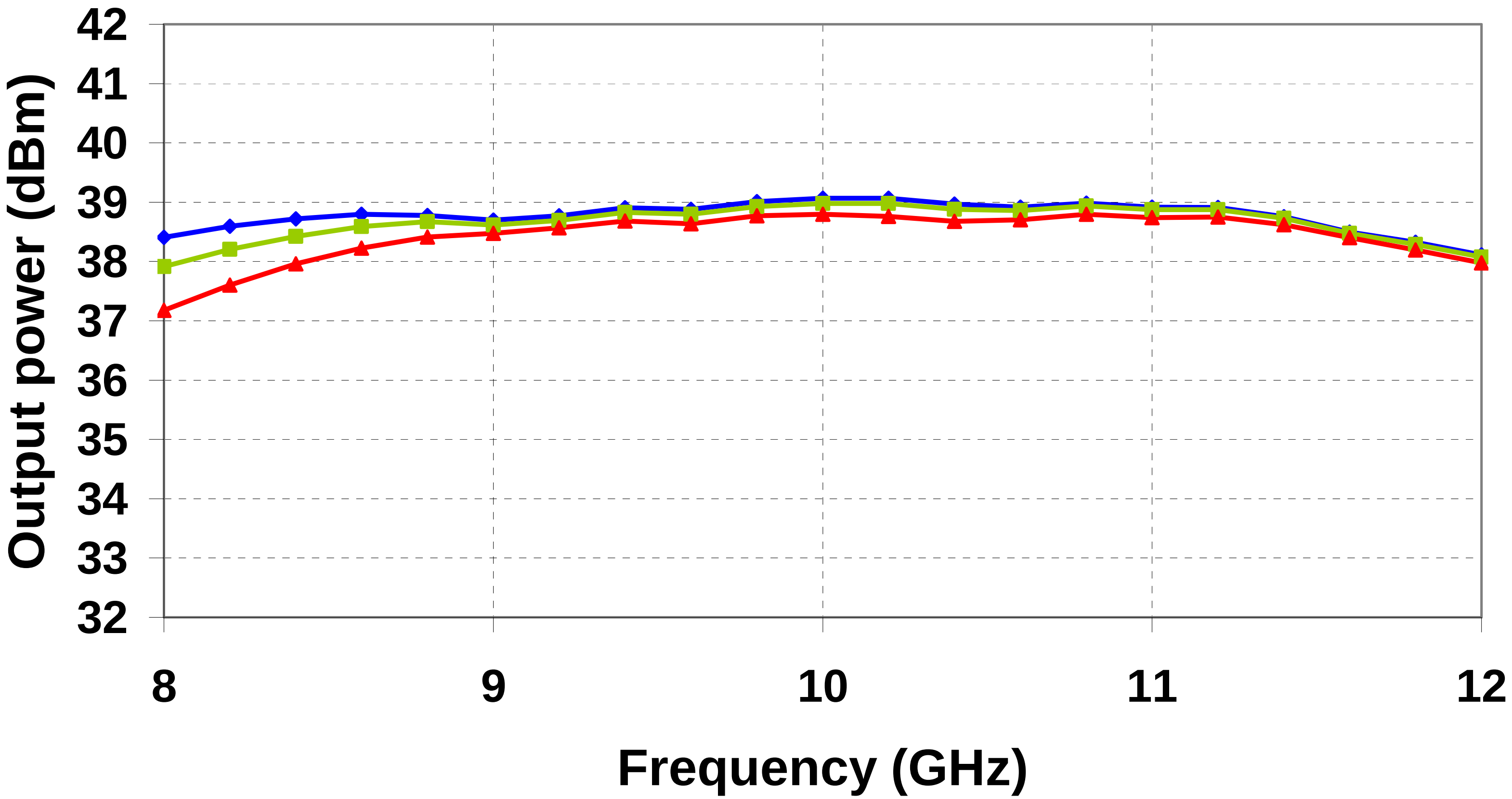
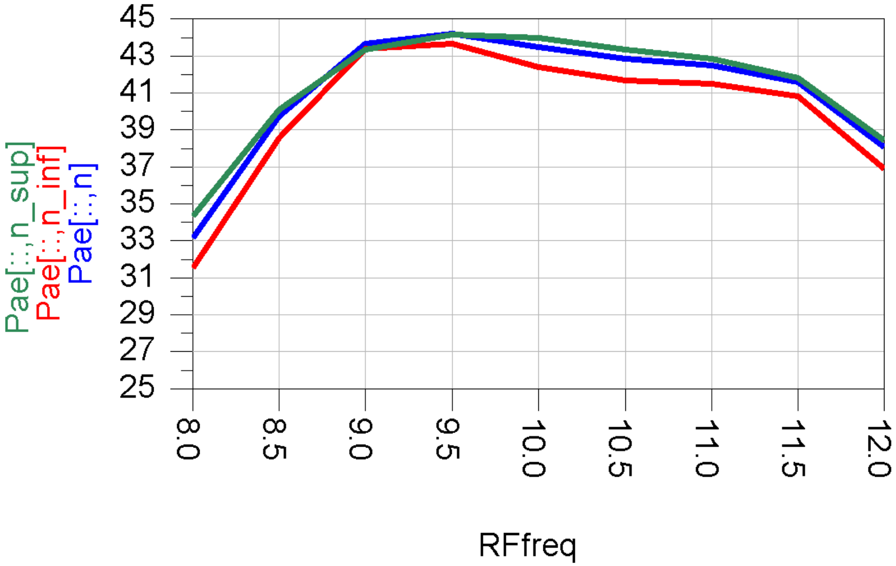


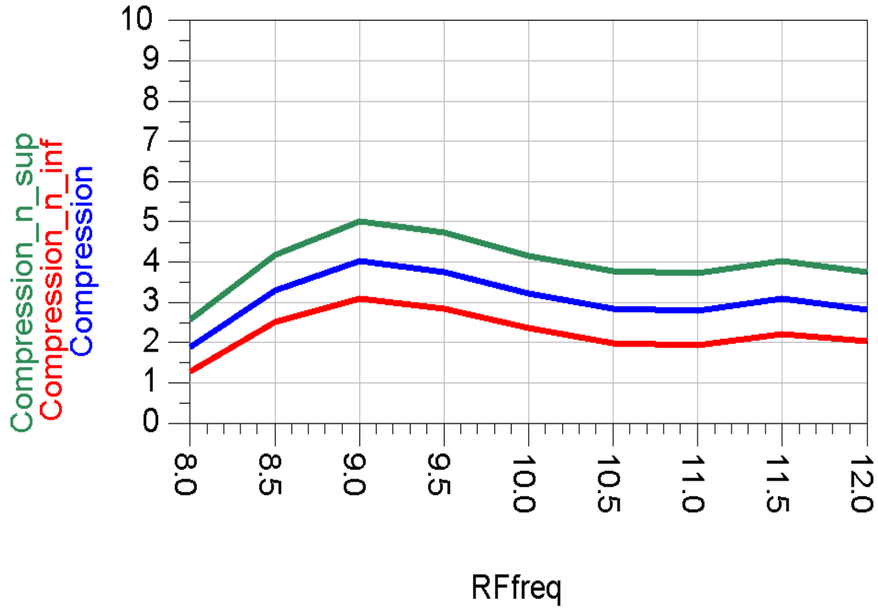
2-stage HPA: simulation with ADS software

PAE for 3dB comp. vs frequency

@+20°C

Drain voltage= 8V
Quiescent current= 2A

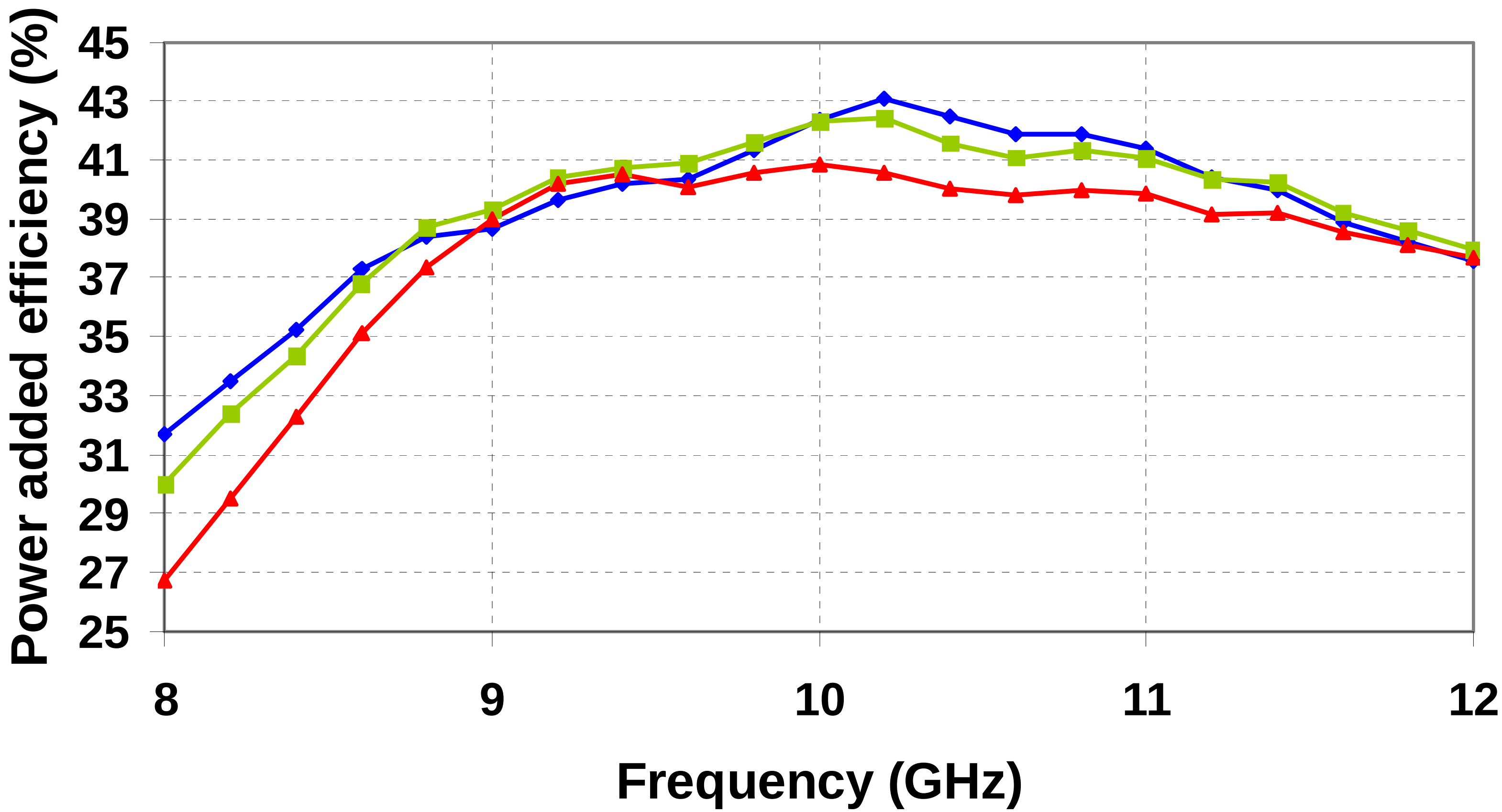




2-stage HPA: measurements

PAE for 3dB comp. vs Pin

Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 100µs
Duty cycle= 30%

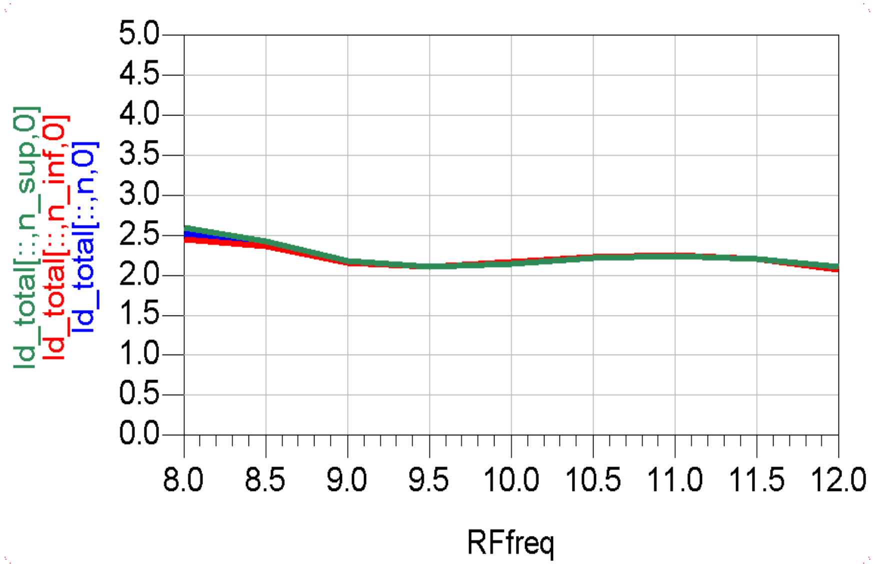


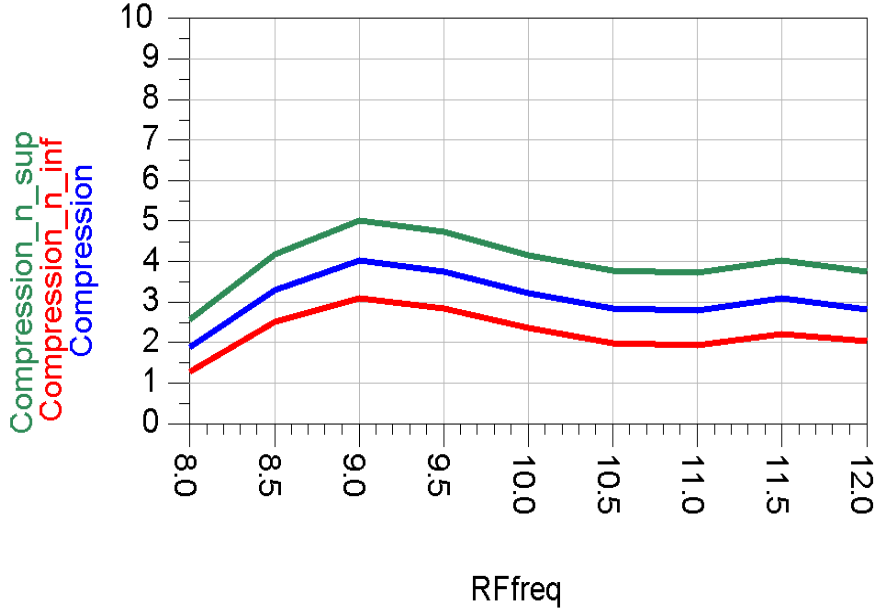
2-stage HPA: simulation with ADS software

Id for 3dB comp. vs frequency

@+20°C

Drain voltage= 8V
Quiescent current= 2A

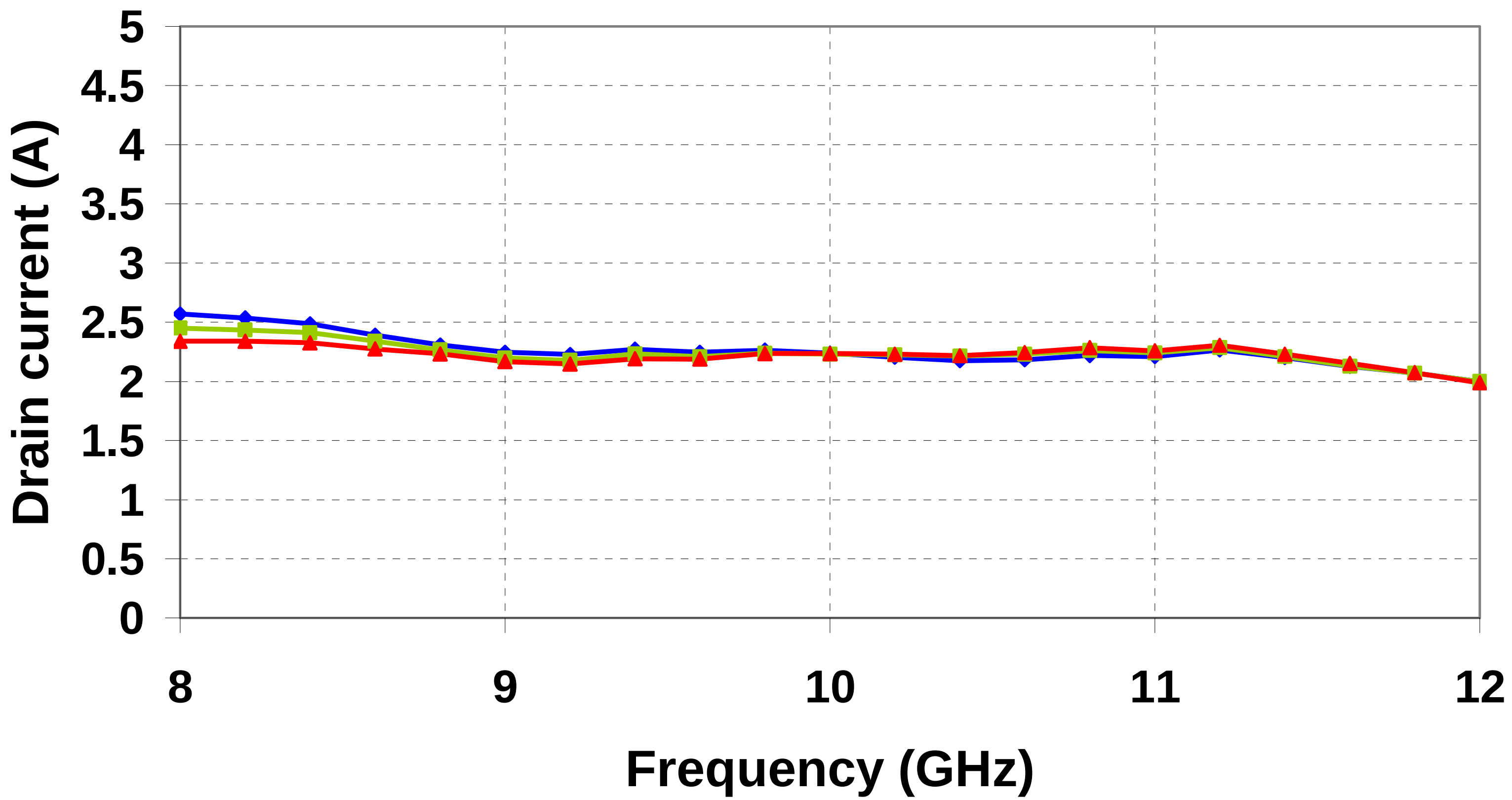




2-stage HPA: measurements

Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 100µs
Duty cycle= 30%

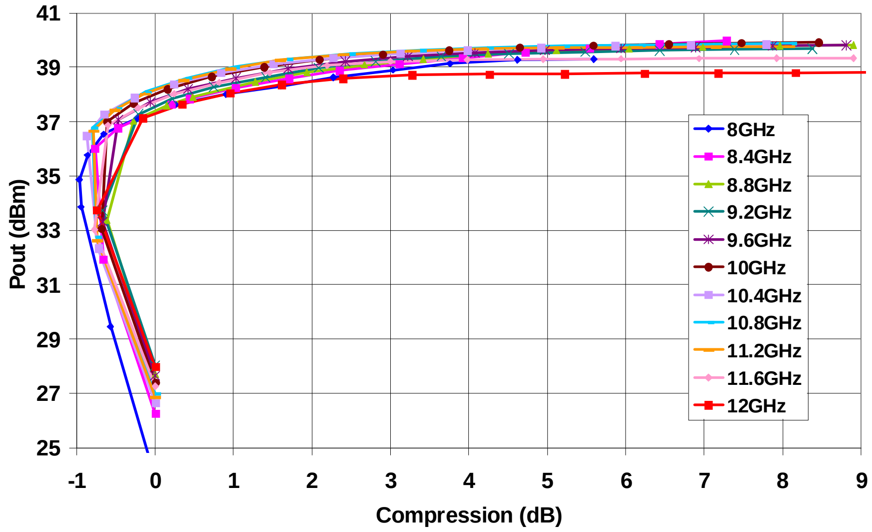
Id for 3dB comp. vs Pin



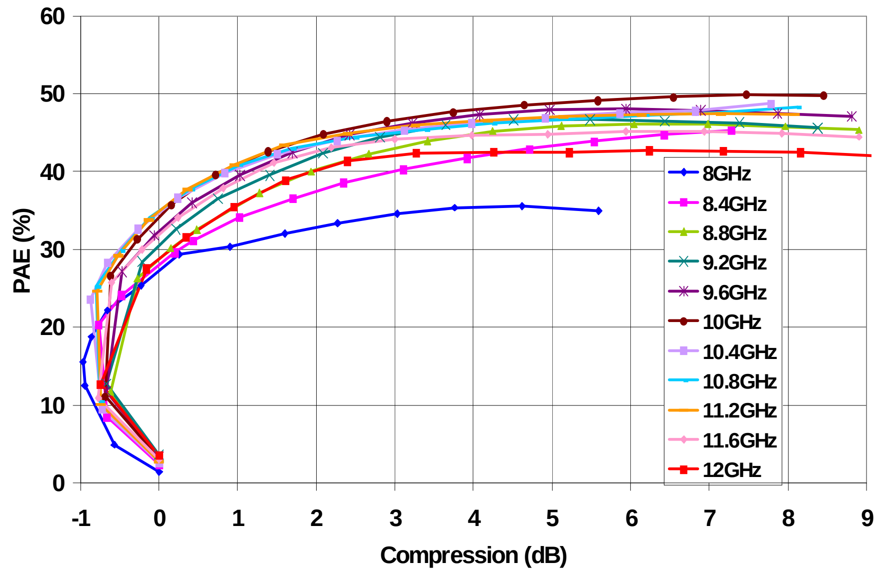
2-stage HPA: measurements

Pulsed drain measurements: 8V
Quiescent current= 2A
Pulse width= 25µs
Duty cycle= 10%

Output power @20°C vs compression



PAE @20°C vs compression



Robustness test vs overdrive

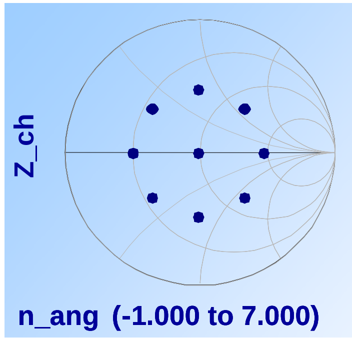
2-stage HPA: measurements

Robustness test in worst cases

Conditions:

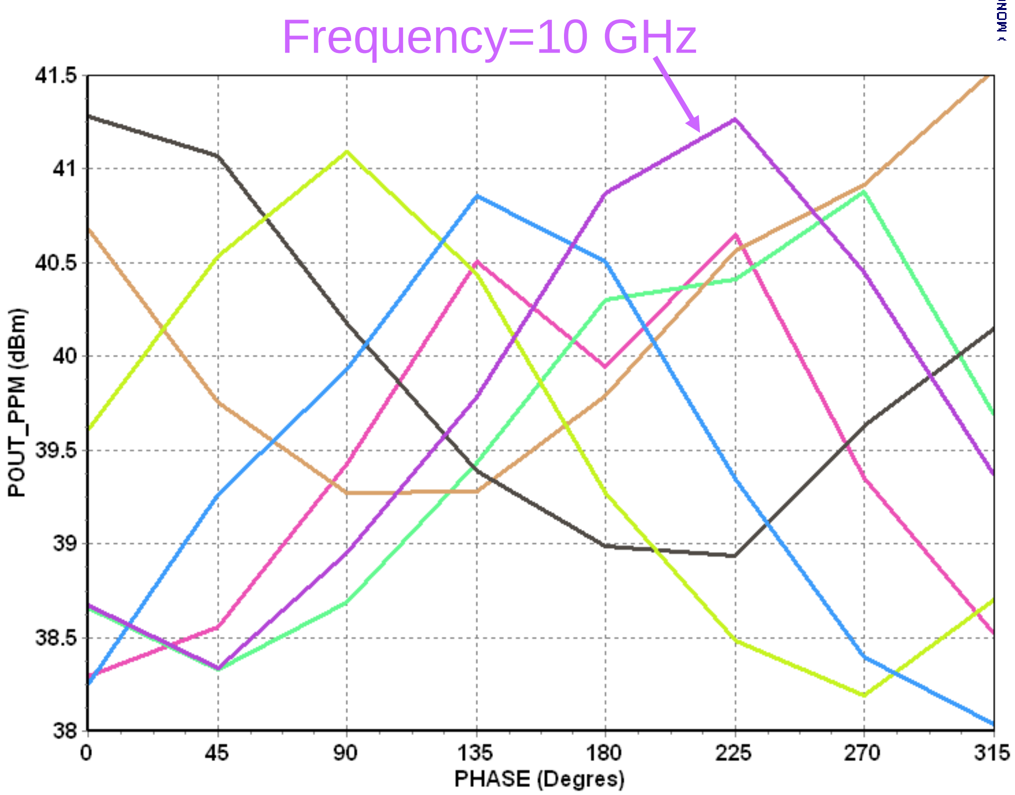
Bandwidth: 8.5-11.5 GHz

- ➔ Drain voltage 8V
- ➔ VSWR 2:1
- ➔ 8 Phase states
- ➔ Short Pulses
- ➔ - 40°C
- ➔ 6dB gain compression



No degradation after stress test

Output power vs phase state



› MONOLITHIC SEMICONDUCTORS

2-stage HPA: main performances and layout

Performances

8.5-11.5 GHz

Small signal gain 19-20dB

Sat. output power: >8W

Sat. PAE: > 40%

Features

DC Power consumption: 18.4W

Chip size : 4.41x 3.31x 0.07mm

Chip area: 14.6 mm^2

Conclusion

- The development of robust HPAs with high level of PAE and high output power has been presented on about 30% of frequency Band thanks to “Advanced Design System” from AGILENT.
- Based on this good accuracy between simulation and measurements, a new portfolio of HPA is under development
  - C Band , Pout >10 W , PAE=40%
  - X Band, Pout >10 W, PAE=40%

Thanks

Thank you for your attention

Any question ?