What’s New In ADS 2017: 3D Design, 3D Simulation & 3D Data Visualization

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ADS 2017: 3D Layout Design

- 3D Layout Viewing directly from the Layout Window
- 3D Editing & Routing
  - PCB & IC/Module Design
  - Dramatically Improved Visual Inspection
  - Simplified Via stitching in multi-layered design
  - Dense area routing
  - Selecting & grouping structures for EM
  - Including DRC Avoidance-routing (Beta)
  - Swap components
- Selection improvements
  - Cycle Selection w/ spacebar
  - Pin Selection
3D EM Performance & High Performance Computing

FEM 1.4X – 6.8X FASTER SIMULATION PERFORMANCE

• Significant improvements in several areas:
  • Initial mesh creation
  • Adaptive mesh refinement
  • Mixed-order basis functions

• HPC Parallel Simulation Licenses
  • Parallel solve of frequency points
  • Multiple W2342 FEM licenses, or
  • W2344 FEM Distributed Computing 8-pack (Turbo)

<table>
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ADS 2017: 3D Electro-Thermal Simulation

MULTI-TECHNOLOGY MMIC/MODULE APPLICATIONS

• Single IC/Single Technology
  • ADS 2016 and earlier releases

• Multi-Technology/Module Applications
  • In ADS 2017

• More ADS 2017 ETH enhancements
  • Thermal Reuse
  • Thermal Substrate Editor
  • Logarithmic Time-step
  • … and much more
ADS 2017: 3D Data Visualization (native install ADS 2017 Update 1.0 Feb/Mar)
ADS 2017 General Schematic & Data Display
New Capabilities
Simplified “Get Started” Screen

ADS 2016

Workspaces
Create a new workspace
Open an existing workspace
Open an example workspace
Convert a project to a workspace
Open recently used workspace
SIPr_FIPr_DDR4_wrk
RFIC_IndCondTemp_wrk
IBIS_PowerBird_9598s_Support_wrk
MyWorkspace2_wrk

Help Center
Current Users
New Capabilities in ADS 2016
Upgrading from ADS 2016 Update 1
New Users
ADS Overview
Create and Simulate a Circuit: Try It!
Register an Knowledge Center
Resources
Documentation (Manuals)
Training Courses and e-Learning
Contact Technical Support
Keysight E-Shop Website
Knowledge Center (Online)
Videos: ADS YouTube Videos

Don’t display this dialog box automatically
Close

ADS 2017

Advanced Design System 2017

Recent Workspaces
SIPr_FIPr_DDR4_wrk
RFIC_IndCondTemp_wrk
IBIS_PowerBird_9598s_Support_wrk
MyWorkspace2_wrk

Commands
New...
Open...
Open Example...
Unarchive...

Has pins

Close
Start Designing Faster

FEWER CLICKS TO A NEW WORKSPACE/SCHEMATIC

ADS 2016

ADS 2017
“Parts” docking window replaces palette window

COMBINES PALETTES, SEARCH, AND HISTORY

Type here to search libraries

Show Recent Parts

Launch Library Browser

Select libraries to search

Auto Completion of Part Names. History still available by clicking on the chevron

ADS 2017
Data Visualization

• 3D Plotting and 3D Smith Chart with the ADS Python Data Link
• Plot load pull contours from measured Maury/Focus data with the ADS Python Data Link
• Limit lines in Data Display
Demo: Limit Lines in Data Display
Data Display Limit Lines & Masks

QUICKLY SEE SIMULATION RESULTS VS. DESIGN GOALS, SPECTRAL MASKS
ADS 2017 Layout & Verification
Layout & Verification

- Layout
  - Complete 3D Layout Capability
  - Trace routing:
    - 45 auto-snap
    - Layer snap for traces
  - Swap components
  - Auto-select based on shape fill
  - DRC Avoidance-routing (Beta)
  - PCB creation wizard
  - 3D VIA Designer

- Verification
  - LVS: “check net names” option for synchronized design modes
  - DRC: New Dialog, Better Performance, Callback capability, Batch mode
DRC and LVS Improvements

**SPEED, CAPACITY, USABILITY & FUNCTIONALITY**

- **ADS DRC**
  - Higher Capacity: ADS DRC produces accurate results for very large ICs
  - Rule Categories: Designers can run a sub-set of the rules during design creation (spacing, width), and the full set of foundry signoff rules when the design is in the final stages (density checks).
  - Usability
    - One mouse click to run DRC.
    - Run DRC without locking up the ADS session.
    - No need to re-configure DRC with a new ADS session. DRC dialog auto detects rules in a PDK and saves the user-configuration (rule categories).
  - Batch DRC: Run DRC on all the cells in a library, or on a cell imported from GDSII, using the DRC configuration specified in a PDK.
  - PDK Configuration: Configure DRC at the library level using standard AEL functions.

- **ADS LVS**
  - Performance and reliability improvements for unsynchronized designs
  - Improved use model for specifying named nets (do not require Terms)
  - Assura DRC: Secure data file transfer protocol & Improved reporting of errors
  - ADS 2017 Licensing: ADS DRC, ADS LVS, and all 3rd party links require the W2320 Advanced Layout License
ADS 2017 EM Simulation: Usability, Performance, Automation & Silicon RFIC EM enhancements
Improved EM Usability

• Create and modify substrates
  • Table based substrate definition and support for non-EM layers

• Select a structure to EM model:
  • Grouping capability plus new cycle/3D/shape/reverse select modes

• Place multiple ports and pins
  • New pin dialog for shape, edge and delta-gap pins
  • Auto layer snap and same shape multiple port placement

• Assemble and Define Ports
  • Negative Pin Ground and Auto Delta Gap Port

• Set up EM simulation options
  • Save and load EM simulation options templates
  • Port “auto” calibration (now called feed types)
**EM Usability**

**PIN AND EM PORT SETUP**

- **Pin and EM Port Setup**
  - New shape support for “Insert>Pin” operation…edge or circle or rectangle or polygon, snapping options for area pins.
  - New easy placement & association of pins for differential port in 2 clicks...
  - New Delta-gap port, creation is now a single action
  - New Auto-Gnd on layer, the need to insert explicit reference pins has been lifted.

- ‘Calibration’ was renamed to ‘Feed Type’
  - “Auto” is new default. You let the decision to the EM simulator.
  - Anything else is a deliberated choice about what feed effect you want to account for
  - “Direct” is new name for “None”
EM Usability

**SETTING EM OPTIONS**

- **EM Setup Templates**
  - EM Setup Templates can be created within a library, a workspace, for a specific user or for all users of the ADS installation (site)
  - A list of templates is presented when you create a new EM Setup
  - You can (re)load a template in an existing EM Setup

- **Simulation Options**
  - Can be saved as Presets
  - Any edit moves you away from the Preset (Preset : <none>). Selecting the named Preset will restore all settings from that Preset.
ADS FEM 1.4x – 6.8x Faster Simulation Performance

- Significant improvements in several areas:
  - Initial mesh creation
  - Adaptive mesh refinement
  - Mixed-order basis functions
  - Parallel solve of frequency points

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FEM in ADS and EMPro 2017

Mesh and Solve Improvements for Accuracy and Performance

- **Initial Meshing**
  - better port mesh
  - merging of objects with same material *properties*
  - minimal memory strategy enforces lambda/3 to prevent false convergence

- **Refine Mesh**
  - full rewrite, more efficient
  - more stable results from mesh N to mesh N+1
  - can refine mesh or increase order

- **Solve**
  - (mutual) port calibration
  - support for mixed order basis functions

- **Frequency Sweep**
  - adaptive frequency sweep (AFS) improved with less zoom-in and can now efficiently work together with distributed simulations

- **Output**
  - smaller footprint: reduced mesh output, more compact field solutions
  - rational model output through .SIO instead of sampled files
**ADS Integrated 3D EM:** Eliminates 2 hrs. manual data transfer per simulation

**SAVE $50,000/YR. IN ENGINEERING TIME, FOR EACH SIMULATION/DAY**

- **START**
  - ADS Layout
  - Export GDS file
  - Import GDS file into other 3rd party EM tools
    - Duplicate layer information
  - Re-Assign material information
  - Set up geometry & ports for simulation
  - Auto-generate Ports
    - (For complex designs)
  - Run EM simulation for S-parameters
  - Import S-parameters from EM tool into ADS
  - Reconnect Ports from EM with other passives and actives for co-simulation and verification

- **END**
  - 10 min.
  - 20 min.
  - 20 min.
  - 10 min.
  - 30 min.
  - 30 min.
  - Hours of Simulation

**Process Breakdown:****
- ADS Layout
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**Time Breakdown:**
- 10 min.
- 20 min.
- 20 min.
- 30 min.
- 30 min.
- Hours of Simulation
EM Enhancements

- ITF and ICT Import
  - LTD substrate generation from Synopsys ITF and Cadence ICT files

- Enhanced EM co-simulation flow with CDF-based cells
  - Interconnect extraction, PyCell support, symbol/layout pin count mismatch, config view, netset properties

- Metal bias Add-on (metal line width and spacing dependent physical line width)
  - Under/over etch effect whereby actual conductor width depends on drawn width and space to other conductors

- Conductor temperature dependency in Momentum
  - Conductor resistance adjusts for temperature

- CoilSys Add-on
  - Add-On to create DRC clean inductor (single-ended or differential), balun, or transformer Pcells for any IC foundry technology. The layouts are parameterized and ready for EM simulation
CoilSys for Silicon RFIC Design

ADD-ON LIBRARY PACKAGE FOR ADS AND VIRTUOSO FLOWS

- Create a DRC clean inductors (single-ended/differential) and Balun/Transformer, Solenoid layout w/ layers mapped to Momentum sub
- Supports creation of Transmission Lines (Microstrip, StripLine, CPW, CPWG)
- Generates scalable EM model through Advanced Model Composer
- Creates PCells (ItemDef based and CDF based) in PDK
Foundries provide substrate data in Synopsys ITF format

AUTOMATIC SUBSTRATE GENERATION FOR EM

- Similar solution for TSMC iRCX format and Cadence ICT format
- Invoked from the Momentum Virtuoso Substrate Editor
- Converts multiple (corner case) ITF files in one go. Optionally generates a Momentum Module
iRCX and ITF files provide “metal bias” tables

ACCOUNTS FOR UNDER/OVER ETCHING EFFECTS

Metal bias table specifies the actual line width in function of the drawn width and spacing to other lines

Without metal bias
With metal bias
Momentum Accounts for Temperature

CONDUCTOR RESISTIVITY TEMPERATURE DEPENDENCY

Material Editor

Effective Inductance

Quality Factor

Layout Simulation

Circuit/EM Cosimulation

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ADS 2017
Silicon RFIC Interoperability w/Virtuoso

- Virtuoso layout opened in ADS to run EM simulation and to create an interoperable EM view usable in Virtuoso
- No more need to run a script for non interoperable PDKs when creating an interoperable EM view
- Interoperable Technology
  - Layer display properties in Virtuoso are now matched in ADS
• Connectivity is established on a physical basis. Instances with pins are no longer required to have instance pins associated with them.

• Inherited connections in a circuit component symbol are matched with bulk node connections in its layout.

• Bulk nodes that are present in a circuit component symbol but lacking from the layout are connected to a global net that can be reassigned in the emExtracted view.

• The restriction where all Pcell submasters of the same cell are required to have the same number of pins and instances has been lifted.

• It is now possible to edit the emExtracted view and still use if for simulation provided that you run EM > Tools > Update Connectivity Extraction Timestamp prior to saving.

• Support for arrays of components

• Support for Pycells

• Support for multi-technology and bondwires

• Transfer of non-substrate layers to emExtracted view for LVS compatibility
ADS 2017 New Electro-Thermal Simulation Capabilities
ADS Electro-Thermal Enhancements

- Multi/Nested Technology Support (Feature)
- Thermal Reuse (DC and HB) : 10X faster (Performance)
- Thermal technology generation using Substrate editor (Usability)
- Logarithmic time step (Envelope and Transient) : (Performance)
- Mask-specific HTCs (heat transfer coefficient) at Horizontal Domain Boundaries (Feature)
- Support splitting power arbitrarily between same named heat sources (Feature)
- Visualization of material data on a thermal layer (Usability)
  - Graceful force exiting of ETH envelope/transient simulation (Reliability)
  - Support Orthotropic Thermal Conductivity in ETH Simulation – No GUI (Beta Feature)
- Several Other Improvements/Fixes delivering. E.g. Auto correction of ETH controller parameter when cell, workspace, test bench copied over to new name/location.
ADS 2017 New Circuit Simulation Capabilities
Interoperable Config Views

• Virtuoso-like hierarchy management
• Create/change/control the hierarchy without modifying the design
• Single GUI to control the complete hierarchy
• Can read Virtuoso hierarchy information in interoperable designs
Simulation Performance Improvements

- New fast envelope options for better accuracy
- Unterminated ports are automatically handled within ADS (large port-count circuits and sweeps experience a large speed improvement)
- AC/SP linear simulation is multi-threaded
- Support for SOA (safe operating area) via assert functionality (for DC and Tran)
- Oscillator Phase Noise 4-10x faster and more accurate
- Simulation Manager runs on Windows
- New & Updated Models
ADS 2017

3D DESIGN, 3D SIMULATION, 3D VISUALIZATION

- ADS 3D Features
  - 3D Layout Design
    - 3D viewing, routing & editing
  - 3D FEM Sim Perf & HPC
  - 3D Data Visualization
  - 3D Electro-Thermal Simulation
- General
  - “Quick Start” & New “Get Started”
  - New Component Library Search
  - Ultra High Resolution Screen
  - Data Display Limit Lines & Masks
  - Improved EM Usability
- Silicon RFIC
  - Interop config views
  - Silicon RFIC Interop Enh
  - Encrypted iRCX support
  - CoilSys & SOA support
- RF/MW
  - Layout Performance
  - DRC & LVS Enhancements
  - FEM Performance & Parallel Sim
  - Electro-Thermal
    - Technology Editor
    - Multi-Technology Support
    - Thermal Reuse
  - Circuit Sim Performance