Hi, Welcome to the session USB 3.0: Facing the challenges of SuperSpeed Product Development

My name is Jim Choate, product manager for measurement technologies in high performance scopes division at Agilent.

First a little background on myself. I joined Agilent a little over a year and half ago following 10 years working for Intel where I focused on high speed serial communications technologies. In this capacity I worked on specifications, validation and compliance programs for high speed serial communications links starting with USB 2.0, then WUSB, PCI express both gen1 and gen2 and lastly the initial investigation into USB 3.0. I am now leveraging that experience by applying it directly to Agilent measurement science in the areas of general purpose debug, validation and compliance testing applications.
To start out I’d like to prepare you with what I hope to accomplish during this presentation.

Because the USB3 specification is still under development the content of this presentation is intentionally limited to information that has previously been disclosed or relates generically to high speed communications or related technology like PCI Express gen2.

Disclaimer: The material and content that describes specific details of the USB 3.0 specification belongs to the USB 3.0 Promoters. Agilent is not speaking or presenting on behalf of the USB 3.0 Promoters.
I will start with discussion of the USB market opportunities and explain why the Promoter group came together to start development of USB 3.0 late last year.

Then I will provide an overview of the PHY layer with a description of what is new for USB 3, what is the same and what has been improved.

Then I will address the challenges of creating a superspeed, backward compatible USB connector and cable assembly.

This will be followed by a description of Link and Protocol changes to address optimization of bus utilization, backward compatibility and improvements for power management.

Then I'll talk briefly about hubs which will serve the same purpose as USB2 hubs, fan out of existing ports.

Follow this with a discussion of power management. At the outset, making USB3 more power friendly is a key goal of the specification work. Last topic will be to address some frequently asked questions followed by a summary.
USB has been a wildly successful interconnect and widely claimed to be the most successful PC interconnect in the history of computing.

As such, following up such a success is a challenge in itself but one that will leverage almost 10 years of development and industry enabling experience.
Due to protocol overhead and bus Link limitations the real throughput of a high speed USB link is much less than 480Mbps. Typical throughput is less than 240Mbps with IO limitations bringing it to 10-20MB/s in many cases. Best case throughput will get us about 35MB/s with optimized drivers and IO speeds/

Clearly something faster is needed with growing sizes of multimedia files. The table shown here lists file size vs speed transfer time.

Under 1G transfer rates are something most people can live with but when you get multi Gig files the transfer rates of Fs are totally unusable with high speed getting beyond our technical patience limits.

Speaker: as you build the slide with the 6G – 16G and 25G numbers discuss the fact that USB2 performance numbers shown will even be slower on systems with other processes running in the back ground.

Also note that the performance improvements to be had with SS are due to both increased data rate (5Gbps) and improvements in link/protocol to get better BW utilization – to be discussed in following slides in more detail.
Ok, so USB 3 will fix the performance issues of USB but what USB products really need this type of performance.

The pie chart shown shows the biggest market opportunity for USB3 performance. A significant number of products are integrating much more memory as people begin to carry their content with them in an increasingly mobile world. This data was provided to the USBIF by iSuppli Corp: 2006.

The biggest piece of the storage market, at roughly 44%, consists of cameras, phones and PDAs which encompass embedded and removable flash used to store content. Getting this content on/off of these devices quickly will feed the need for speed.

External flash drives and mp3 players are another large category at almost 30% that needs high data rate transfers. As flash gets faster the bus needs to get faster to keep pace.

The last category is a rapidly growing category of solid state disk technologies for the mobile and external storage markets. These products already push the limits of USB 2.
Here is a summary list of the market requirements that are driving technical requirements for the USB 3 specification.

Must have 10x the performance of USB2, this means real system throughput – not just signal rate.

Must be capable of very low power states and have more flexibility for active management of power states

Must be backward compatible. USB2 products must work with USB3 hosts and USB3 devices must work with USB2 hosts.

Protocol needs to scale to provide room to grow

Must minimize sw impact to ensure investment in drivers and programming models is retained.

### Market Requirements Summary

- **Performance 10X USB2 - PHY signal rate of 5 Gbps**
  - data throughput > 200 MB/s
- **Optimize for power efficiency**
- **Connector & Cable backward compatible with USB 2.0**
- **Protocol scalable to provide extension beyond 5Gbps**
- **Minimize SW impact**
  - Same Programming and Device models as USB 2.0
- **Support Virtualization for Devices**
Here is the latest information on current USB3 schedule.

The specification is at Rev 0.85 today. Some significant changes have been made to the previous version so please be sure to review the latest draft for information. Currently only promoters and contributors have access to the specification and any specification details not already publically disclosed are USB3 promoter confidential.

The goal is to have the specification at rev 1.0 by the end of this year at which time it will be provided to the Adopters via signing the Adopters agreement so they can begin designing products to the specification.

Compliance program work and review will/has begun with a working face to face meeting in July in Oregon.

It is expected that initial USB3 silicon will be available at the end of 2009, beginning of 2010 with full scale deployment of commercial product starting in the second half of 2010.
This slide summarizes some of the industry events that have occurred and some upcoming working meetings.

The promoters and contributor groups were formed in 2007 and specification work commenced. Intel and the promoters held an Industry review and updates at spring IDF on status of specification and marketing requirements.

After compliance work is nearing completion, with work session planned in July, the USBIF will take on management of compliance test events and marketing/promotion of USB3.
This slide shows a comparison of USB2 vs 3.0 for most of the biggest differences.

Obviously the speed change is the biggest difference.

USB2 is half duplex (since twisted pair, bi directional) and 3.0 will be 8b/10 full simplex.

The block diagrams as the bottom of the slide show this difference.

USB2 has 4 signals, usb3 includes those 4 plus 4 additional signals.

For USB3 cable length details are “spec detail” because they haven’t been publically discussed yet so you should only verbally mention that the requirements don’t list a specific length yet, only performance requirements.

I config limits will change by increasing approximately 50% to 150mA for low power devices and 750mA for high power devices. Again, this detail is not something you should give in text in the slides as it may change.

SSC is not supported in USB2, SSC is required for USB3.
- Compliance testing will be very similar to PCI express gen2.
- Testing is defined at the connect
- The scope will terminate the link with the TX detection of 50 ohms the condition to go into compliance pattern mode just like PCIE
- Will analyze 1M UI and compute eye diagram, Rj, Dj, Tj, etc.
Due to the increased BW and longer channel lengths more testing requirements for cables, connectors and channel validation

TDR testing will be required for verifying cables, connectors and trace impedance meet new more stringent requirements, 90 ohms +/- 7 ohms differential impedance.

TDT measurements for cable skew will be required for cable qualification testing.
VNA measurement of Sparameters will also be necessary to accurately characterize return loss, insertion loss and near/far end cross talk.
The sparams can then be used to de-embed the channel to characterize the transmitter to the pins.
Some of the greatest challenges for SuperSpeed USB will be in creating robust and easy to use cables and connectors for USB 3 5Gbps data rates. EMI/ESD and backward compatibility are significant challenges for this technology. Not least is the goal of minimizing user confusion by minimizing the cable/connector combinations available for products.
Maintaining basic USB transfer types is critical to keeping the software architecture consistent with USB2.

One big problem with USB2 is the relative lack of power management capabilities and the power unfriendly nature of polling architecture.
Link/Protocol enhancements

Link Layer

- Dedicated IN and OUT lanes, not multiplexed
- Aggressive power management; Links go to low power states when idle

Protocol Layer

- Host schedules all transactions
  - There is no polling for SuperSpeed USB
- Devices transmit only when they have data
- Hosts transmit only when they have data
- Unlimited bursting

Important power and performance changes
USB2 transaction model as shown. From left to right you can see the basic IN and OUT transaction consisting of host token, data packet and handshake. Because the bus is bi-directional 100s of bit times are consumed during bus turn around phases resulting in wasted BW

For usb3 transactions the IN and OUT transactions incur no BW penalty
Flows

A new concept to give more flexibility to devices

An endpoint can have multiple flows, that are unique and handled separately by H/W

• Very close to being just another endpoint

Usage case: USB Mass Storage

• Driver can make multiple requests, with each request being a separate flow
• Drive prioritizes requests and returns data in appropriate flow
• Host HW deposits data in appropriate buffer
Hubs are the only type of device that can simultaneously transmit on USB2 and USB3 connections at the same time

Hubs serve the same role as they did for usb2 – fan out for usb3 and usb2 connectivity

Hub port routing logic is responsible for establishing the logical connection to either the usb2 or usb3 communication path depending on device capability.
LFPS is specified to provide a lower power state (lower frequency) communication mechanism without using super speed protocol
Frequently Asked Questions

1. Does USB 3.0 define or require an optical connection?
   • NO, this was discussed during the initial phases of the investigation but was ruled out due to cost. USB 3.0 will be wired only.

2. Is USB 3.0 going to be backward compatible with USB 2.0?
   • Yes, USB 3.0 requires that the host port is compatible with all USB 2.0 supported speeds: Low speed, Full speed and High speed.

3. Why does SuperSpeed require 4 new signals, SSTXP, SSTXN, SSRXP, SSRXN?
   • Backwards compatibility requires support for Low and Full-Speed USB. These run at 3.3V signal levels which is not compatible with IO buffers designed to run at 5Gbps

4. How will users know that a USB port supports SuperSpeed?
   • USB 3.0 ports will be color-coded Blue to make them recognizable.
Summary

SuperSpeed USB addresses USB 2.0 performance bottleneck and retains attributes that made USB so successful

• Maintains backward compatibility
• 10x performance
• Same programming and device models as USB 2.0
• Optimized for power efficiency
• Protocol scalable to 20Gb/s

USB 3.0 will deliver Performance and Power Efficiency
Agilent has the tools and expertise to help you validate your designs