Agenda

• Introduction

• Compliance Testing
  – Physical Layer Compliance Testing
  – Protocol Layer Compliance Testing: Agilent PTC 2.0

• Advanced Protocol Test Topics
  – LTSSM Validation
  – Link & Transaction Layer Advanced Testing
  – Power Management Testing
  – IO Virtualization
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- **Introduction**

- **Compliance Testing**
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  - Power Management Testing
  - IO Virtualization
Testing and Validation

When using a standard technology such as PCI Express, detailed testing and validation is critical to ensure devices will interoperate with each other.

Implementation of a proper test plan can significantly reduce cost later.

For example: How much does an ASIC spin cost when a bug is found after a device is in the field?
Basic vs Advanced Testing

Basic Testing

• PCI-SIG Compliance

Advanced Testing

• From the Link Layer Test Specification
  – “At this point this specification does not describe the full set of PCI Express tests for all link layer requirements. Going forward, as the testing gets mature, it is expected that more tests may be added as deemed necessary.”

• Ensuring your device is fully validated against the specifications
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PCI-SIG Compliance Testing

• Physical Layer
  – Validate Signal Quality of TX, Ref Clock and PLL Loop Bandwidth

• Configuration Space
  – Verify required fields and values behave as specified

• Link Layer & Transaction Layer
  – Exercise protocol, error and boundary layer conditions

• Platform Configuration
  – Validate BIOS correctly handles different topologies of PCI Express Devices

• Demonstrated Interoperability
  – Show that device drives load and device operates in actual PCI Express System
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Physical Layer Testing Goals for PCIe 2.0

Goals for PHY testing are unchanged from PCI Express 1.0
Achieving those goals is more challenging
Additional requirements added to increase confidence that designs are robust
Verify designs achieve critical specification targets
  - Jitter
  - Eye mask
  - Reference Clock
  - Voltage and Jitter margining
  - Receiver Margining
Changes Implemented under the 2.0 Specs
- Physical Layer

Changes to the PCIe Base Specification

- 5GT/s
- Different de-emphasis levels
- PLL bandwidth testing
- Backward compatibility with PCIe 1.1

PCle Card Electromechanical (CEM) Specification Changes

- Rj / Dj tables and new jitter budgets
- Changes to Reference clock phase jitter specification
- 2 port measurement method for systems
Signal Level and BW

2.5G de-emphasis = -3.5 +/- 0.5

5G de-emphasis = -3.5 +/- 0.5 OR -6.0 +/- 0.5

Low swing voltage levels = no de-emphasis

BW dependant peaking requirements

- 3dB for 8 to 16MHz
- 1dB for 5 to 8MHz
- 2.5G same as 1.1
PCIe 2.0 PLL Loop Bandwidth Testing

**Equipment Required:**
- Sine Wave Source (1GHz min)
- Modulated Pulse Generator (100MHz)
- Spectrum Analyzer (3 GHz min)
- Modified CBB2

**Steps:**
- Sweep source 100-125Mhz (-20dBm)
- SA: 35KHz Res BW, 40MHz Span, 2.5 GHz center
- Set display to peak hold
- Normalize response to note 3dB point
CEM Spec targets connector

System Board TX

Add-in Card

Clarification of measurement location
Compared to 1.1
Chip + Interconnect
5GT/s jitter challenges

Jitter measurement more complex!
Jitter decomposition required

\[ System \ Tj = \sum Dj + 2Q_{BER} \sqrt{\sum Rj^2} \leq 1.0 \ UI \]

Speed dependant phase jitter filters

- 2.5G = 1 pole HPF
- 5G = step band pass filter

Error correction needed to measure TX at pins

\[ +/- 7.03 \]
For 10-12 BER
New Transmitter base specification requirement
- “Measurements at 5.0 GT/s must de-embed the test fixture
- “It is also acceptable to use a common test fixture and de-embed it for measurements at both 2.5 and 5.0 GT/s.”

What does it mean to de-embed?
- “Measurement at 5.0 GT/s must de-convolve effects of compliance test board to yield an effective measurement at Tx pins.”
Source of Measurement Inaccuracies

- impedance mismatches
- probing effects
- smaller geometries
- test cables and adapters
- fixturing
- device packaging, etc.
- SCOPE NOISE FLOOR!

There are multiple ways to offset these measurement impairments.

- calibration methods
- mathematical signal processing
- de-embedding/embedding techniques

Why is error correction needed to measure at TX pins?

Measurement system noise will be amplified by de-embedding techniques
Error Correction Techniques

Pre-measurement operations

- Skew Calibration
- Probe Attenuation/offset
- Channel Vertical Cal
- Channel Trigger Cal

Calibrating the Scope

DSO91304A 13GHz Oscilloscope

Post-measurement operations

- De-embedding the CLB/CBB

N5230A PNA-L Network Analyzer

S-parameters

Fixture effects

Removed
De-embedding – Loss Compensation or Gain Function

- Compensate for Probing and Fixture Loss – Add Margin to Transmitter Characterization
- Allows more accurate measurement of de-emphasis levels at transmitter
- Compliance Requirement for Gen 2
SQ Test Tool Requirements – System Board

Use of CLB 2.0

SMP to SMA adapter, phase matched SMA cables

Terminate all lanes except the lane under test

Measure transmitted clock and data waveforms simultaneously with high speed oscilloscope

Use compliance pattern

1M UI of data

Sample rate of 40GS/s (25ps)

Compute:

– eye diagram,
– $R_j$, $D_j$, $T_j@10^{-12}$ BER,
– average data rate,
– rise/fall time,
– mode toggle

Measure all lanes of all 5GT/s capable slots
Test Tool Requirements - AIC

Use of CBB 2.0

SMP for all lanes, phase matched SMA cables
Terminate all lanes except the lane under test
Measure transmitted waveform with high speed oscilloscope
Use compliance pattern
1M UI of data
Sample rate of no more than 25 ps
Compute:
  - eye diagram,
  - $R_j, D_j, T_j@10^{-12}$ BER,
  - average data rate,
  - rise/fall time,
  - mode toggle
Measure all lanes
Key Requirements:

- 1M UI automated data acquisition
- Batch run capability for greater testing coverage or quick spot checking
- Implement measurements that respect the PCIe Specification
- Automated tools should self-scale to ensure top accuracy for each measurement performed
- Results must be consistent with PCI-SIG tools used at Compliance Workshops
Test Results with the Agilent N5393B

HTML based automatic report generator allows you to easily share test results.

Select the version to test
Select the test point
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Logical Physical Layer testing

Link Training issues –

“I start link training but I cannot establish a link”

“I plugged my 1.1 card into a 2.0 system and it does not work, why?”

“I plugged my 2.0 card into a 1.1 system and it does not work”

“I pass electrical compliance but I still cannot link”

Although a card may successfully pass the electrical requirements, it may not be possible to link for other reasons.

This is critical for interoperability!
Logical Physical Layer testing

Some suggested reasons why a link may not successfully train –

Presence Detect:
- Are the PRSNT1# and PRSNT2# pins wired correctly on both the system slot and the add-in card? Does the system support Hot-Plug?
- This is especially critical when the link width of the card and the mechanical and electrical link width of the slot do not match

Reference Clock:
- Are the reference clocks on both sides compatible?

Link Width:
- Does the link train to the desired width? Does it link in all required widths?

Reserved bits in Training Sequences:
- When the reserved bits are used in the TS1 and TS2 ordered sets (for example, Gen 2 uses some bits which were reserved in Gen 1), do the devices still train successfully?
Electrical testing forces the device into a special compliance mode designed to create the worst case scenario electrical characteristics. The device is connected to a piece of test equipment which measures the electrical characteristics.

Protocol Testing requires that the device link up with another device. Testing this requires 2 types of tester:
- Protocol Analyzer
- Stimulus tool, such as exerciser

The PCISIG has an extensive list of test assertions which can be used to verify that a device is compliant to the specification.
Goals for PCIe 2.0 Compliance Testing

Goals for Protocol testing are unchanged from PCI Express 1.0

Verify devices have met the critical specification targets for:

- Config space test specification
- Link layer test specifications
- Transaction layer test specifications
- Platform Bios test specifications

Additional testing regarding reserved bits usage
Test descriptions are not changed for Gen 2 Link and Transaction Layer tests with the exception of the Reserved bits test—

New for PCIe 2.0 devices

• All Gen 2 devices will be tested at 2.5GT/s AND 5GT/s where appropriate
• Gen 2, 2.5G only devices will be tested using the Gen 2 PTC
• Reserved bits test tries to link up with all reserved bits set in training sequences
Link and Transaction Layer Tests

Link Layer tests are a subset of the compliance checklist – a cross section of tests which if the device is compliant would indicate a reasonable chance of interoperability.

Includes Error checking, and dealing with Link stability problems

List of Link Layer and Transaction Layer Tests

- BadLCRC
- CorruptedDLLPs
- DuplicateTLPSeqNum
- LinkRetrainOnRetryFailNoAckNak
- LinkRetrainOnRetryFail
- ReXmitOnNak
- ReplayNumTest
- ReplayTLPOrder
- ReplayTimerTest
- RequestCompletion
- ReserverdFieldsDLLPReceive
- UndefinedDLLPEncoding
- WrongSeqNumInAckDLLP
### Flow Control Initialization Protocol

#### Data Link Layer Packet Rules

| DLL 5.2#1 | The link transmitter must start REPLAY of its RETRY_BUF as soon as (after finishing the current TLP in progress) a NAK is received | Test52-10 |
| DLL 5.2#1.1 | The link transmitter must start REPLAY of its RETRY_BUF upon its REPLAY_TIMER expiring when there are still some TLPs which have not received Ack or Nak DLLPs | Test52-11 |
| DLL 5.2#1.2 | A TLP must be retransmitted until a positive acknowledgement has been sent by the receiver and received by the transmitter and REPLAY_NUM doesn’t overflow while retransmitting (subject to the timeout values in Tables 3.4 and Table 3.5 to which Rx/Tx_L0e_Adjustment must be applied as appropriate) | Test52-12 |
| DLL 5.2#2 | If repeated retries fail and REPLAY_NUM overflows, the link transmitter must ask the Physical Layer to retrain the link. There must be a reported error to correspond to this as per Section 6.2 | Test52-20 |
Test Hardware Setup

Card being tested for compliance

Agilent PTC 2.0 approved by the PCI-SIG for Protocol Gold Suite testing.

Agilent protocol analyzer for troubleshooting any issues that come up
1. Matching test case names to easily identify which tests are being run

2. Matching test descriptions to the test spec.

3. Color coded to easily identify what the test results

4. Report tab, with detailed execution and reason for pass/fail

5. Message framing to allow the analyzer to easily capture the key parts of the test execution
Testing the reserved bits in Training Sequences

In the 1.1 base specification, there are several reserved bits in the TS1 ordered set. Some of these bits are now used in the 2.0 specification — mainly in relation to the speed change and capability, in the Data Rate Identifier field:

### 1.1 Specification

<table>
<thead>
<tr>
<th>Symbol Number</th>
<th>Allowed Values</th>
<th>Encoded Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>K28.5</td>
<td>COMMA code group for Symbol alignment</td>
</tr>
<tr>
<td>1</td>
<td>0 – 255</td>
<td>D0.0 - D31.7, K23.7</td>
<td>Link Number within component</td>
</tr>
<tr>
<td>2</td>
<td>0 – 31</td>
<td>D0.0 - D31.0, K23.7</td>
<td>Lane Number within Port</td>
</tr>
<tr>
<td>3</td>
<td>0 – 255</td>
<td>D0.0 - D31.7</td>
<td>N_FTS. This is the number of fast training ordered sets required by the Receiver to obtain reliable bit and Symbol lock</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol Number</th>
<th>Encoded Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>D2.0</td>
<td>Data Rate Identifier</td>
</tr>
<tr>
<td></td>
<td>Bit 0 – Reserved, set to 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 1 – 1, generation 1 (2.5 Gbps) data rate supported</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 2 – Reserved, set to 0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol Number</th>
<th>Encoded Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>D4.0, D10.2</td>
<td>TS1 Identifier</td>
</tr>
</tbody>
</table>

### 2.0 Specification

#### Table 4-2: TS1 Ordered Set

<table>
<thead>
<tr>
<th>Symbol Number</th>
<th>Allowed Values</th>
<th>Encoded Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>D2.0, D2.2, D2.4, D2.6, D6.0, D9.2, D6.4, D9.6</td>
<td>Data Rate Identifier</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 0 – Reserved, set to 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 1 – When set to 1b, indicates 2.5 Gbps data rate supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 2 – When set to 1b, indicates 5.0 Gbps data rate supported</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Devices that advertise the 5.0 Gbps data rate must also advertise support for the 2.5 Gbps data rate (i.e., set Bit 1 to 1b)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 3 – Reserved, must be set to 0b</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit 4 (Autonomous Change) – Downstream component. Autonomous Change/Reset Link De-emphasis: When set to 1b in Configuration state and Link/p = 1b, indicates that the speed or Link width change initiated by the Downstream component is not caused by a Link stability issue</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In Recovery state, this bit indicates the de-emphasis preference of the Downstream component. In Polling Active substate, this bit specifies the de-emphasis level the Upstream component must operate in if it enters Polling Compliance and operates in 5.0 Gbps data rate. In Configuration/LineWidth Start substate or poll back (Link/p = 1b) and in the Loopback Entry substate, this bit specifies the de-emphasis level the Upstream component must operate in if it enters Loopback state (from Configuration) and operates in 5.0 Gbps data rate. For de-emphasis, a value of 1b indicates -3.5 dB de-emphasis and a value of 0b indicates -6 dB de-emphasis. This bit is reserved in all other states for a Downstream component. Upstream component: In Polling Active, Configuration/LineWidth Start and Loopback Entry substates, this bit specifies the de-emphasis level the Downstream component must operate in if it enters Polling Compliance and Loopback states, respectively. A value of 1b indicates -3.5 dB de-emphasis and a value of 0b indicates -6 dB de-emphasis. This bit is reserved for all other states. Bit 7 (speed_change) – When set to 1b, indicates a request to change the speed of operation. This bit can be set to 1b only during Recovery/LineWidth state. All Layers under the control of a common TSGM must transmit the same value in the Symbol Transmitters must advertise all supported data rates in Polling Active and Configuration/LineWidth Start substates, including data rates they do not intend to operate on.
Testing the Reserved Bits in Training Sequences

– It has been observed that many cards built to the 1.1 specification do not in fact ignore the reserved bits when used by a 2.0 device.

– This can cause the link not to train and is a severe interoperability issue.

– The PCISIG has introduced an official test in the Link Layer test specification which ensures that devices can link when these reserved bits are used.

– This test can be done with the Agilent Gen 2 PTC card or any of the Agilent Gen 2 Exerciser products.

– Since official 1.1 testing will not change in the foreseeable future, this test can be run on 1.1 cards and is a very strong indicator whether the device will operate in a 2.0 system.
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Protocol Changes in the 2.0 Specs

Changes to the PCIe Base Specification

- Physical Layer : Logical Sub Block
  - 5GT/s Support
  - LTSSM use of Recovery state to Change to 5G speed
  - Link up/down configure – Dynamic Link Width change
- Data Link Layer
  - Replay timers for 5GT/s support
- Transaction Layer
  - Principally unchanged – the test specification is identical
- Configuration Space
  - Reserved bit usage, new registers to support different speed options
How does link training work?

Two PCI Express devices exchange Training Sequences to negotiate link parameters like

- lane polarity
- link number
- set of lanes that belong to the link
- lane numbers
- scrambler enabled or disabled
- link speed
- number of fast training sequences required
- ...

Training Sequences are also used to switch the link to low power states.
Example from the PCI Express 2.0 specification, Polling.Active state (p. 196):

- “Transmitter sends TS1 Ordered Sets with Lane and Link numbers set to PAD (K23.7) on all lanes ...”
- “Next state is Polling.Configuration after at least 1024 TS1 Ordered Sets were transmitted, and all Lanes ... receive eight consecutive TS1 or TS2 Ordered Sets ...”
- “Otherwise, after a 24 ms timeout the next state is:
  - Polling.Configuration if, ...
  - Polling.Compliance if ...
  - Else Detect if the conditions to transition to Polling.Configuration and Polling Compliance are not met.”
LTSSM Test Challenges

What are the LTSSM test challenges?

The LTSSM with all its states, substates, transitions and conditions is quite complex. The number of possible scenarios is immense.

Link training is a dynamic process.

The sequence and timing of state transitions is not fixed. The sequence differs with

– different lane ordering
– different timing behavior
– signal integrity (occasional bit errors)
– violations of the standard (error scenarios)
– implementation specific behavior
New Challenges for Gen 2 – Speed Change!

Key features:

• Recovery state used for speed change from Gen 1 to Gen 2

• Dynamic link width negotiation now possible, allowing the link to train up or down on the fly.

• Specific tests available for testing the LTSSM

• Gen 2 is backwards compatible with Gen 1

It is possible to plug a Gen 2 device into a Gen 1 slot and the link will negotiate to the highest common value.
LTSSM Test

Select Test Case

- Basic
  - Exerciser starts Link Training at 2.5 GT/s
  - Capture state transitions
- Recovery
  - Exerciser Initiates 5.0 GT/s Speed Change
  - DUT Initiates 5.0 GT/s Speed Change
  - Exerciser Initiates 2.5 GT/s Speed Change
  - DUT Initiates 2.5 GT/s Speed Change
  - Exerciser Initiates Transition to Recovery
  - Negotiated Data Rate Fails in Recovery.RcvrLock
  - Current Data Rate Fails in Recovery.RcvrLock
  - Exerciser Initiates Speed Change on Any Configured Lane
  - Force Transition from Recovery.RcvrLock to Configuratio
  - Negotiated Data Rate Failed in Recovery.RcvrCfg
  - Current Data Rate Failed in Recovery.RcvrCfg
  - Force Transition from Recovery.RcvrLock to Detect
  - Force Transition from Recovery.RcvrCfg to Detect
  - Force Transition from Recovery.Idle to Detect
  - Exerciser Initiates Upconfiguration
  - Exerciser Initiates Upconfiguration without being capab

Exerciser Initiates 5.0 GT/s Speed Change

**Purpose:** To test the link for a speed change from 2.5 GT/s to 5.0 GT/s data rate, initiated by the exerciser.

**Prerequisites:** Please ensure the following are satisfied before starting the test:
- Link is up.
- Link is in DL.ACTIVE state.
- Link speed is 2.5 GT/s.
- Data rate supported is 5.0 GT/s.

**Observation:** The following automatic checks are performed after execution:
- The link is up.
- Link speed is 5.0 GT/s.
- Link width is x1 <depends on user selected width>.
- Sequence of LTSSM states in transition:
  - Recovery.RcvrLock
  - Recovery.RcvrCfg
  - Recovery.Speed
  - Recovery.RcvrLock
  - Recovery.RcvrCfg
  - Recovery.Idle
  - L0, L0s
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Link & Transaction Layer Advanced Testing

- Large number of features/capabilities mandated by specification
- Each requirement has many branches and many actions
- Example: Advanced Error Reporting
- Time consuming to create these test cases, and also time consuming to troubleshoot and validate results
Advanced Error Reporting (AER)

Validation of all the different branches is required:

- Need to initialize the devices
- Need to create different types of errors, using exerciser test tool
- Need to check that the device under test (DUT) sets all the right bits in the right registers
- Need to make sure the right messages are sent with protocol analyzer
PTC II (E2969B)

• March 24, 2008 - Agilent Technologies Inc. today announced that its Protocol Test Card (PTC) 2.0 has been approved by the PCI-SIG(r) (PCI Special Interest Group) for PCI Express(r) (PCIe(r)) 2.0 protocol testing.

• Includes all add-in card tests from the Gen1 PTC (22 tests)

• The Agilent PTC II will enable device compliance with the PCI-SIG® by providing 13 mandatory test cases.

• Upgradable to X1 exerciser in the future

Compliance Assured Test Package (N5309A-COM)

• Compliance Assured Test Package (N5309A-COM), is available and adds an additional 180 recommended tests. The Compliance Assured Test Package includes transaction layer, link layer, electrical layer and configuration space tests.
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What is Power Management

Power savings by going into low power states

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
<th>Recovery Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>L0</td>
<td>Fully Active</td>
<td>N/A</td>
</tr>
<tr>
<td>L0s</td>
<td>Standby</td>
<td>ns</td>
</tr>
<tr>
<td>L1</td>
<td>Low Power Standby</td>
<td>us</td>
</tr>
<tr>
<td>L2</td>
<td>Low Power Sleep</td>
<td>ms</td>
</tr>
<tr>
<td>L3</td>
<td>Off (zero power)</td>
<td>ms</td>
</tr>
</tbody>
</table>
Power Management (ASPM) Testing

Drivers:

- Windows Vista supports the low power states for medium power saving and high power saving modes
- Cost savings in terms of power consumption, heating/cooling in datacenters
- Drive towards green devices

Challenges:

- Many devices have problems going in and out of the electrical idle states L0s and L1
- The link is technically still active in these cases even although it is in Electrical idle
- Getting devices into these low power states on demand, and waking them up on demand
Power Management Testing

**Exerciser**
- L0s support; ensure one direction only goes into L0s
- L1 support
  - Trigger other device to enter into L1 state

**Analyzer**
- PM packet decodes
- Fast sync times to track devices going into and out of PM states
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I/O Virtualization (IOV) – The capability for a single physical I/O unit [e.g. NIC card] to be shared by more than one system image (SI).

SR-IOV : Single Root IOV
MR-IOV : Multi Root IOV

Standards are an overlap, however, application drivers for SR-IOV and MR-IOV are very different.
Better server utilization through:

- Software virtual machines on one physical server; VMWare, Parallels, etc
- I/O end points do not need to know about virtualization

Challenges of current technology:

- Requires software/firmware intermediary
- The intermediary is involved in all transactions; configuration, I/O transfers, which lowers the performance
MR-IOV Drivers

Cost reduction

- I/O Purchase cost: each blade server goes from 28 NIC cards and 4 switches to 4 NIC cards and 2 switches
- Cost of power and cooling to the data center
- IO Consolidation: Moving from multiple technologies to single -> Ethernet & FC to FCoE
MR-IOV on Protocol Analyzer

<table>
<thead>
<tr>
<th>Record No</th>
<th>Timestamp</th>
<th>Rel. Ti.</th>
<th>101/1:Downstream</th>
<th>101/1:Upstream</th>
<th>Message</th>
<th>Len</th>
<th>RBus</th>
<th>RDev</th>
<th>CBus</th>
<th>CDev</th>
<th>C'In</th>
<th>Address, Register No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1008537</td>
<td>-4.286 us</td>
<td>376 ns</td>
<td>Ack</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1008539</td>
<td>-3.940 us</td>
<td>328 ns</td>
<td>MRUpdateFC Data</td>
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<tr>
<td>1008541</td>
<td>-2.980 us</td>
<td>960 ns</td>
<td>MRUpdateFC He...</td>
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MR-IOV fields decoded for easy analysis.
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Unique In The Industry

Agilent PCI Express® 1.0 & 2.0 Solution
The Digital Application

API – Automation
Exerciser
- LTSSM x16
- X16 Device Emulation & Error Insertion
- Compliance Testing

Probing
- Midbus 2.0 x16
- Interposer x16

One Analyzer – Two Use Models

Lane Analyzer
- Per-lane display
- 8B/10B decode
- Triggering on ordered set
- Power Management

Protocol Analyzer
- Packet, transaction and payload views
- Easy flow technology
- Advanced Triggering

One Analyzer – Two Use Models

Logic Analysis Solution
- FSB
- Memory Bus
- General Purpose

Extended P2L gateway

Probing
- Midbus 2.0 x16
- Interposer x16

Protocol Analysis Solution
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- PCI Express
- ASI

One Analyzer – Two Use Models

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The Digital Application

Agilent Tools
For further information

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<td><a href="www.agilent.com/find/pciexpress">www.agilent.com/find/pciexpress</a></td>
<td>Agilent tools to help you succeed with your PCI Express design such as the N5393A Compliance application.</td>
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<tr>
<td><a href="www.agilent.com/find/si">www.agilent.com/find/si</a></td>
<td>Agilent tools to help you master signal integrity challenges</td>
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