Welcome

Innovations in EDA Webcast Series

Accurate Modeling of GaAs & GaN HEMT’s for Nonlinear Applications

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Presented by:

Agilent Technologies

Free 1-hour Webcast

Dr. Ilcho Angelov
Associate Professor
Microwave Electronics Lab
Department of Microtechnology and Nanoscience
Chalmers University Goteborg Sweden

Roberto Tinti
Device Modeling Product Planner
Agilent EEsof EDA
Accurate Modeling of GaAs & GaN HEMT's for Nonlinear Applications

Innovations on EDA Webcast, May 7 2013

Agenda

• Part I: Non linear, self-heating and dispersion modeling in the Angelov-GaN model
  
  Dr. Il'tcho Angelov, Associate Professor, Chalmers University

• Part II: Overview of the Angelov-GaN model parameter extraction

  Dr. Roberto Tinti, Agilent Technologies
Outline:

1 Empirical Nonlinear IV and Capacitance LS Models
2 Self-heating and Dispersion modeling

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GHZ Centre Chalmers, Goteborg, Sweden, SSF.

Presenter Part1: Iltcho Angelov  MEL, Chalmers Univ. Goteborg, Sweden
iltcho.angelov@chalmers.se

Additional info on FET Modeling on Chalmers Web page:
FET model extraction: iltcho.angelov@chalmers.se
Model Types

1. Physical Models - *very important in the device design stage.*
2. Table Based Models - *accurate in the Measurement range!*
   Typ. 1000 measurement points! X-parameters, Neural Models - *now!*
Problems: Outside Measured Frequency Range? Harmonics? Change of working conditions: Temp, Rtherm, Ctherm etc.? Manufacturing tolerances?
Scaling to High Power Devices (it is easier with smaller devices and scale later).
Do not provide feedback for the device quality, change of parameters-> this is important issue for foundries! Data set is large >20 mB->slow.
3. Empirical Equivalent Circuit Models. 100-200 measurements points
   Accurate enough for many applications-1-10%.
   Comparably easy to understand and extract, compact form- parameter list.
   *Extendable out of the Measurement Range* > from 65GHz to 230GHz [Ref:46-48].
   Possibility to tune & change model parameters, production tolerances, Rtherm...
   Provide feedback for device parameters change, quality of processing.
   All model types have their place. We should use the right type for the specific application. We can mix & integrate different type models- example:
   Empirical & Physical[49]; Empirical & Table Based (ETB[44,45]) etc.
1. **Physical** !!!

2. Single definition $-\infty + \infty$; Infinite & correct derivatives.

3. Flags, conditions should be avoided (device don’t have flag)!

4. The best solution is to split (if possible) the model $F$ on independent parts:
   \[ F = f_1[\Psi_1(V_{gs})] \times f_2[\Psi_2(V_{ds})] \]

5. The model parameters should be responsible for specific things:
   - Current, Voltage, Cap, Slope, etc.

6. **When possible, use the inflection points to construct the model.**
   This reduce model parameters, simplifies the extraction.

7. **Directly extractable!** Available in CAD tools!
   If the guess for modeling function $F$ is good, extracted argument is linear function:
   \[ f_{1a}(V_{gs}) = 1 + \tanh(P_1 \cdot V_{gs}) \]
   \[ \Psi_{1a}(V_{gs}) = \arctanh(f_{1a}) = P_1 \cdot V_{gs} \]
   A pocket calculator can be used for extraction.
FET Ids-> solution of Schrodinger equation:

Error type functions

Typical for FET: \( f_1(V_{gs}) = 1 + \text{erf}(V_{gs}) \)

The error function is not always available in CAD tools and simple & direct reverse extraction is not possible.

Replacement of error functions for FET modeling:

a) GaAs: \( f_{1a}(V_{gs}) = 1 + \text{Tanh}[P_1.V_{gs}] \)
   extraction: \( \Psi_{1a}(V_{gs}) = \text{ArcTanh}[(\text{Ids}/I_{pk0}) - 1] \)

b) GaN and SiC: \( f_{1b}(V_{gs}) = 1 + \text{Tanh}[\text{Sinh}(P_1.V_{gs})] \)
   extraction: \( \Psi_{1b}(V_{gs}) = \text{ArcSinh} [\text{ArcTanh}[(\text{Ids}/I_{pk0}) - 1]] \)

c) We need to fit different profiles i.e. Adjustment possibilities!

d) Using inflection point( I_{pk0}, G_{max} ) will make model compact and exact at important, critical point - G_{max} with predefined G_{m} shape.
Ids Model Function Selection - direct
Direct Extraction $\Psi$  Examples GaN, SiC

a) GaAs: $f_{1a}(V_{gs}) = 1 + \text{Tanh}[P1 \cdot V_{gs}]$
$\Psi_{1a}(V_{gs}) = \text{ArcTanh}[(I_{ds}/I_{pk0})-1]$

b) GaN and SiC: $f_{1b}(V_{gs}) = 1 + \text{Tanh}[	ext{Sinh}(P1 \cdot V_{gs})]$
$\Psi_{1b}(V_{gs}) = \text{ArcSinh}[\text{ArcTanh}[(I_{ds}/I_{pk0})-1]]$

c) Directly extractable; d) Using $\text{Tanh}[\text{Sinh}]$ improves the harmonics fit for low $P1<1$

H. Rohdin ED-33, N5, May 1986 pp. 664

ns($V_g$) = $n_{s0}(\alpha + (1-\alpha)\text{tanh}[(V'_g - V_{gm})/V_1])$
Ids Model  Function Selection 4
Spectral content( derivatives)

\[
\text{erf}(x) = \frac{2}{\sqrt{\pi}} \sum_{n=0}^{\infty} \left( -1 \right)^n \frac{x^{2n+1}}{n!(2n+1)} = \frac{2}{\sqrt{\pi}} \left( x - \frac{x^3}{3} + \frac{x^5}{10} - \frac{x^7}{42} + \frac{x^9}{216} - \ldots \right)
\]

\[I_{ds} = I_{pk} \left( 1 + \tanh(\Psi) \right); \Psi = P_1(V_{gs} - V_{pks}); \text{GaAs}\]

\[I_{ds} = I_{pk} + I_{pk} \ast P_1 \ast V_{gs} - \frac{1}{3} (I_{pk} \ast P_1^3) V_{gs}^3 + \frac{1}{10} (I_{pk} \ast P_1^5) V_{gs}^5\]

\[I_{ds} = I_{pk} \left( 1 + \tanh(\Psi_1) \right); \Psi_1 = P_1(\sinh(V_{gs} - V_{pks})); \text{GaN}\]

\[I_{ds1} = I_{pk} + I_{pk} \ast P_1 \ast V_{gs} - \frac{1}{3} (I_{pk} \ast P_1^3) V_{gs}^3 + \frac{2}{15} (I_{pk} \ast P_1^5) V_{gs}^5\]

\[I_{ds1} = I_{pk} + I_{pk} \ast P_1 \ast V_{gs} - \frac{1}{6} (I_{pk} \ast P_1^3) V_{gs}^3 + \frac{1}{40} (I_{pk} \ast P_1^5) V_{gs}^5\]

You get Rectangular Gm shape directly

DC, 1-st equal

5-th different

3-rd different
High Power, High Frequency FET EC

Parasitic elements: $R_g, R_{gd}, R_d, R_s, R_{i}$, $C_{ds}, L_g, L_d, L_s$, layout elements etc.

**New:** $R_{del}, C_{del}$ shunting the gate control node $V_{gsc}$

- Frequency dependent gate control and delay.
- Frequency dependent $R_s$ for SiC

1. **Nonlinear:** $I_{ds}, I_{gs}, I_{gd}, C_{gs}, C_{gd}$ -> we need models.

Models are controlled by intrinsic voltages!

FET model extraction: iltcho.angelov@chalmers.se

I. Angelov
FET Measurements for Modeling, Screening for tolerance extraction:

1 Preliminary screening for device selection for modeling!
2 Measurements. The general rule is that the device should be measured sweeping Vgs from Pinch-off to the full channel current (typically Vgs=+0.8 GaAs), stepping Vds. To get the important points, matrix of 10Vgs and 10 Vds is typical. 

Screening, device selection for modeling, tolerance evaluations:

a) Resistances Ron and Rof (FET Transistor functionality): Vds in the linear region, below the knee, sweeping Vgs from pinch-off to full channel current. Vds=0.1 to 0.2V is good choice for GaAs FET, Vds=1 to 2V for GaN, SiC FET.
b) Full saturation current Isat for Vds at the knee. for GaAs FET Vds=0.8V, Vgs=+0.8; for GaN FET; Vds= 6 to 8V, Vgs= +0.8 to+1V

c) transconductance gm for Isat/2 ; gm for Isat, Vds at the knee.
d) Pinch-off current at Maximum operating Vds- important for high voltage, high power FET applications. Device biased at Class C (or AB)
e) S-parameter Measurement for Capacitive and parasitic parts extraction.
f) Screening Optional: Ft, Fmax at Isat/2 Vknee

g) Screening Optional: Pout for Zl= 50 ohm; low RF (0.5 to 1 GHz) Pin = 0 dBm GaAs, Pin= 14 dBm (GaN) for Isat/2; Vds=Vknee; Pin depends on the device size.

This logical flow is implemented in ICCAP
1 FET Transistor functionality evaluation: $R_{ds}(Ron)=R_d+R_s+R_{ch}(f(V_{gs}))$.

**Meas. 1** We need $R_s,R_d$ to account for the intrinsic voltage drop. Nonlinear Models for currents & capacitances are controlled by intrinsic voltages.

*Ids vs. Vgs for low Vds in the knee region* in the linear part of the IV: sweeping $V_{gs}$, fixed low $V_{ds}$. Cold extraction, $V_{ds}=0$, from S-par is not good for GaN! -> safe measurement, GaN -> $V_{ds}=1V$, GaAs -> $V_{ds}=0.1V$.

$R_{ds}(Ron)=V_{ds}/I_{ds}$: For gate in the middle S-D we can consider:

$Rs=R_d=R_{ch}=R_{ds}/3$ *Very good staring values for optimization.*

Good device: $Ron=3 \, \Omega$m, $Roff>3\, \Omega$Ohm

Working device: $Ron=6 \, \Omega$m, $Roff=10 \, \Omega$kOhm

FET model extraction: iltcho.angelov@chalmers.se
Measurements $I_{ds}$ vs. $V_{gs}$

Part of $\Delta V_{pk}$ is due to voltage drop on $R_s \times I_{ds}$

$\Delta V_{pk} \approx 0.2V$ (GaAs, CMOS)
$\Delta V_{pk} \approx 0.6-1V$ (GaN).

This should be considered as the device is controlled from intrinsic voltages.

**Meas 3. IV - $I_{ds}=f(V_{gs}, V_{ds})$**

$\rightarrow$ at $V_{pk}$ & and corresponding $I_{pk}$ $G_{mm}$ for $V_{ds}>V_{knee}$

$P_{1s}= G_{ms}/I_{pk}$

$\rightarrow$ $V_{pk}$ voltage & $I_{pk}$ current at $G_{m} (=G_{m0})$ for $V_{ds}<V_{knee}$

$G_{m}$ for GaAs, GaN, SiC, FET & CMOS are usually bell shaped.

FET model extraction: iltcho.angelov@chalmers.se
Measurements: $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ param.

\[
\begin{align*}
I_{ds}(mA) @ V_{gs} & = 0.6V \\
I_{ds}(mA) @ V_{gs} & = 0.4V \\
I_{ds}(mA) @ V_{gs} & = 0.2V \\
I_{ds}(mA) @ V_{gs} & = 0V \\
I_{ds}(mA) @ V_{gs} & = -0.2V \\
I_{ds}(mA) @ V_{gs} & = -0.4V
\end{align*}
\]

- $\alpha_r$: slope at Small currents, Low $V_{ds}$
- $\alpha_s$: slope High Saturated currents, Low $V_{ds}$
- $\lambda$: slope at high $V_{ds}$ & small currents.
- I.e. we need 3 parameters to model the slope $I_{ds}$ vs. $V_{ds}$(min.)

The **negative slope** at high dissipated power is due to selfheating, it is not observed in pulse IV! The effect should be modeled with a thermal network!

FET model extraction: iltcho.angelov@chalmers.se
Self-heating effects are due to:

1 **Change of mobility**: Reduced mobility at higher temperature ->smaller Gm:
   \[ P1T = \frac{gm/Ipk}{1 + TcP1 \cdot \Delta Tj} \]
   Linear function + -100C  (\( TcP1 = -0.003 \))-negative

2 **Change of carrier concentration**: This will reduce the channel current:
   \[ Ipk0T = Ipk0(1 + TcIpk0 \cdot \Delta Tj) \]
   \( TcIpk0 = -0.003 \)-negative

3 **Device speed**: mobility change will influence capacitances, tau:
   \[ Cgs0T = Cgs0(1 + TcCgs0 \cdot \Delta Tj); \]
   \[ Cgd0T = Cgd0(1 + TcCgd0 \cdot DTj) \]
   \( TcCgs0 = +0.003 \)

4 **RF and dispersion characteristics**: influenced by traps (at higher temperature things worsen)
   \[ R_c = f(T) \]
   \( TcRc = -0.002 \); \[ C_{rf} = f(T) \]
   \( TcC_{rf} = +0.002 \)

5 **For all FET, important temperature coefficients are similar**:
   \( TcIpk0 = -0.0025 \) to \(-0.0035\); & **negative**:
   \( TcP1 = -0.0020 \) to \(-0.0035\); & **negative**:
   \( TcCgs0 = 0.002 \) to \(0.0035\); & **positive**

6 **Temperature coefficients** can be found making CW measurements at 3 temperature( 25,75,125C).

7 **Rtherm is not constant with temperature**. For high dissipated power \( >10W \)
   should be considered:
   \[ R_{therm}(T) = R_{therm}(1 + TcR_{therm} \cdot DTj) \].
Ids model 1: Simple 5 Parameters, Vds>Vknee: Ipks, Vpks, P1, αs, λ

\[ I_{ds} = I_{pks} (1 + \tanh(\Psi_p)) \cdot \tanh(\alpha_s V_{ds})(1 + \lambda V_{ds}) \]

\[ \Psi_p = P_{1m} ((V_{gs} - V_{pks})) \]

\[ P_{1m} = g_{mpk} / I_{pk} \]

Ids, gm are exact (defined) at Vpks

With 5 parameters, typical global error <10%.
The model give directly correct shape of the IV and transconductance Gm.

Single definition \(-\infty+\infty\); Infinite & correct derivatives.
Ids model 2: 11 Parameters Model:
Ipks, Vpks, P1, αs, λ + ΔVpk, αr, P2, P3, B1, B2

\[ I_{ds} = I_{pks} (1 + \tanh(\Psi_p)).\tanh(\alpha.V_{ds})(1 + \lambda V_{ds}) \]

\[ \psi_p = P_m ((V_{gs} - V_{pks}) + P_2 (V_{gs} - V_{pks})^2 + P_3 (V_{gs} - V_{pkm})^3) \]

\[ V_{pk}(V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks} \tanh(\alpha_s V_{ds}) \]

\[ P_m = P_1(f(T))[(1 + \Delta P_1)(1 + \tanh(\alpha_s V_{ds}))] \]

\[ \alpha = \alpha_r + \alpha_s \times (1 + \tanh(\psi_p)) \]

11 parameters model: 5par. + ΔVpks, P2, P3, ar, B1, B2

P1 for Low Vds is higher than P1s for High Vds

DP1 - is reduction of P1 = Gm/Ipk for high Vds

B1, B2: track the change DP1 vs. Vds
Ids Equations – Extended: 
**Breakdown & Dispersion**

\[
I_{ds} = I_{pk}(T)(1 + \tanh(\Psi_p))\tanh(\alpha V_{ds})(1 + \lambda V_{ds}) + \lambda_{sb} e^{kb(V_{dg} - V_{tr})}
\]

\[
\Psi_p = P_{1m}(T)((V_{gs} - V_{pk0}) + P_2(V_{gs} - V_{pks})^2 + P_3(V_{gs} - V_{pkm})^3)
\]

\[
P_{1m} = \frac{g_{mpk}}{I_{pk}}; I_{pk} = f(T); P_{1m} = f(T)\text{self-heating}
\]

\[
V_{pks} (V_{ds}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks} \tanh(\alpha_s V_{ds} + K_{BGate} V_{BGate} - V_{sb2} (V_{dg} - V_{tr})^2)
\]

\[
\alpha_p = \alpha_R + \alpha_S \ast (1 + \tanh(\psi_p)); \alpha_n = \alpha_R + \alpha_S \ast (1 + \tanh(\psi_n))
\]

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**Ids Breakdown very Important for High Power designs**

**Back-gate-Dispersion parameter**

**Ids parameters=14** (Ids-10, Breakdown param.=4)

7 important Ids parameters: \(I_{pk}, P_1, V_{pk}, \Delta V_{pk}, \alpha_r, \alpha_s, \lambda\) are found directly from measurements and provide accuracy \(<5\%

CAD tool is used for the extraction and optimization.
Variety of \textbf{Gm shape, P1s= Gms/Ipks: GaN ,SiC, GaAs FET.} Models should be able to handle this.
It is important to find the reason for the specific effect, Gm dependence etc. to model and implement this properly.

Example 1; Gm shape- doping profile (Ids dependence vs. Vgs) - \( \text{Ids}=f(\Psi(\text{Vgs})), P2, P3 \)

Example 2; GaN FET – Rs, Rd are bias dependent, \( \text{Rs}=f(\text{Ids}), \text{Rd}=f(\text{Ids}) \),

Example 3; Rs, Rd temperature dependent - self-heating. \( \text{Rs}=f(T) \)

Usually we have several physical effects on the top of each other. I.e. we need several, properly designed measurements to distinguish between effects like specific Ids measurements, Measurements at 3 equally spaced temperatures, pulsed IV etc...

Example 1:
Parameters of the \( F=f(\Psi(\text{Vgs})) \) function changed

Example 2: Rs Bias dependent

Example 3: Rs, Rd temperature dependent
Ids Model  Function Selection

We can add part of $\Psi_2$ working at other voltage $V_{pk2}$, and combine. We can create large variety of Gm shapes with only 2 extra parameters $V_{pk2}$, $AA$. Example: $V_{pk}=-0.3$; $V_{pk2}=-2$; $AA=0$ to 1

$$\Psi = P_1p ((AA (Vgs - Vpk) + (1 - AA) (Vgs - V_{pk2}) + P_2p (Vgs - Vpk)^2 + P_3p (Vgs - Vpk)^3))$$

At some moment we should stop to increase parameters-> we can switch to Table Based Model or ETB !!!
ETB: Modeling Complicated IV & Cap shapes.

Combine the best of Empirical and Table Based Models

**Empirical model serves as spline function**

Complicated data (parts of the model) loaded using data set

High accuracy and good description of harmonics and good convergence. Significant reduction of required measured points (100-200 OK).

**Easy to extrapolate out of the measured IV and frequency range.**

**ETB LSM FET**

\[ I = I_{pk0} \cdot \tanh(\alpha_{\text{table}}) \left( 1 + \tanh(P1 \cdot \psi_{\text{table}}) \right) \left( 1 + \lambda \cdot \lambda_{\text{table}} \right) \]

1. Difficult to model parameters replaced with table data.
2. Good convergence and infinite number of derivatives.
3. User access to technologically \& mounting dependent parameters: Ipko, Vpk, P1, Ron, Rtherm, Ctherm etc.

Complicated Ids(Vgs)  Complicated Ids(Vds)

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FET model extraction: iltcho.angelov@chalmers.se

I. Angelov
FET Igs Equations –
These devices have Gates!

Gate parameters:
\[ V_{jg}, I_j, P_g \]

In ADS is implemented diode equation, shifting the coordinate system at \( V_{jg} \), at which we operate the device

Simple: 3 parameters Igs model - \( V_{jg}, I_j, P_g \); slope \( P_g = 1/(V_t \eta) \):

\[
I_{gs} = I_j (\exp(P_g \cdot \tanh((V_{gs} - V_{jg}))) - \exp(-P_g \cdot V_{jg})) ; GaAs, V_{jg} = 0.8
\]

\[
I_{gd} = I_j (\exp(P_g \cdot \tanh((V_{gd} - V_{jg}))) - \exp(-P_g \cdot V_{jgs})) ; GaN, V_{jg} = 1.2
\]

Igs Breakdown model: 3 parameters 6 tot

3-simple Igs model + \( 3K_{bdgate}, E_{bdgate}, V_{bdgate} \)

\[
I_{gsbd} = I_{gs} \left(1 + K_{bdgate} \cdot \exp(E_{bdgate}((V_{gs} - V_{bdgate})))\right)
\]

\[
I_{gdbd} = I_{gd} \left(1 + K_{bdgate} \cdot \exp(E_{bdgate}((V_{gd} - V_{bdgate})))\right)
\]
Important for Large&High Power devices:

1. The Gate Control is delayed and reduced at high frequency:
   Large&High Power Devices do not respond immediately at RF!
   
   $C_{del} = 2-3 \text{fF}$ is the capacitance of the gate footprint, $R_{del} = 2 \text{kOhm}$ (channel resistance)

2. Current slump - In some cases at RF we do not reach the DC $I_{ds}$ values.

3. (Back-gate) voltage will change the effective $V_{gs}$ at RF $\rightarrow$ dispersion

4. Higher $R_s$ and $R_d/\text{mm}$ for SiC and GaN FET in comparison with GaAs FET

5. $R_d$, $R_s$ bias and temperature dependent! (A. Inoe et al., IMS2006 WE2F2, M. Thorsel)

6. Self-heating model - must! Mounting quality is critical.

7. Breakdown important for high power devices!

8. Keep device safe $<P_{max}$!

Organize measurements properly. For GaN Dual region measurements & simulations:

A) High $I_{ds}$, Low $V_{ds}$;

B) Low $I_{ds}$, High $V_{ds}$ - Cover the load line!!!

FET model extraction: iltcho.angelov@chalmers.se
The main difference in the GaN FET model in comparison with the default GaAs model in Verilog implementation are:

1. Modified psi function: \( \tanh(\sinh(\psi)) \) – \( Ids \) model 3.
2. Capacitance model which can provide peaking for \( Cgs \), Capmodel 3,4. The capacitances are implemented as charge-Capmodel4 and as capacitance: Cap model3 – This keep the model compatible with simulators with capacitive implementation.
3. Temperature and bias dependent \( Rd, Rs \) – this is important when device is pushed hard.
4. Enhanced dispersion modeling, back gate approach \( Vbg \), delay circuit to model the knee walkout.
5. The \( Ids \) breakdown exponent can be adjusted with parameter \( Ebd \).
6. GS and GD junction breakdown is also included we push device to the limits. Setting \( Kbdgate=0 \) will switch-off the junction breakdown (default=0)
7. Many functional changes made by Tiburon to improve the stability.
8. **Verilog model can be used as mainframe.** When device has some specifics features the model equations can be easily changed.
Model Parameters GaN tot. 69

GaN
Ids parameters: 12
Cap parameters: 15
Thermal parameters: 8
Igs: 3

GaN model implemented in VerilogA => ADS 2009:
1 \( f_1(\Psi) = 1 + \text{Tanh}[\text{Sinh}(P1.Vgs)] \)
2 \( R_d \) and \( R_s \) are bias ( \( R_d^2 \) ) and temperature dependent ( \( T_cR_s \)),
\( R_{s\text{bdep}} = R_s \times (1 + \text{Tanh}(\Psi)) \); \( R_{d\text{bdep}} = R_d \times (1 + \text{Tanh}(\Psi)) \);
\( R_{s\text{bdepT}} = R_{s\text{bdep}} \times (1 + T_cR_s \times DT_j) \); \( R_{d\text{bdepT}} = R_{d\text{bdep}} \times (1 + T_cR_s \times DT_j) \);
3 Dispersion (\( R_c, R_{c\text{min}}, C_r, R_{\text{cin}}, C_{r\text{fin}} \)) + Backgate \( K_{\text{bgate}} + R_{\text{del}}, C_{\text{del}} \)
4 Breakdown for GS, GD Junctions: \( K_{\text{bdgate}}, V_{bdgs}, V_{bdgd}, P_{bdg} \)
5 GaN + Noise: RF and LF; Tiburon DA: ADS 2010; MO-implementatio

Parasitics & package

Breakdown: 7
Dispersion: 8

FET model extraction: iltcho.angelov@chalmers.se
SS Equivalent Circuit Extraction for GAN FET

1 Small Signal extraction from multibias S-parameter measurements Capacitances are extracted from S-par measurements in 3-10 GHz range, depending on the device size.

2 Measured & Extracted SS capacitances should be verified for Charge Conservation:

$$\frac{\partial C_{gs}}{\partial V_{gd}} = \frac{\partial C_{gd}}{\partial V_{gs}}$$

3 Cappy; Berroth - Cold FET method (VDS=0) for extraction will not give correct results for GaN! The reason for this: Rs and Rd are bias and temperature dependent. GaN Resistances Rd,Rs depend strongly on the dissipated power. For constant power they are quite constant with Vds. When cold values for Rs and Rd are used, unrealistically high Output Power and PAE will be predicted! Cold values should be used only as a start and limit the optimization values.

Bias dependence Rd,Pdc vs. Vgs(Ids)
Cap Models FET GaN

- Cgdpi-minimum cap; Cgs0, Cgd0: capacitances at the inflection point; P11, P21: slope vs. Vgs, Vds, Cgs, Cgd vs. Vds

Some GaN devices show peaking modeled with the term \( m \) when terminal voltage is 0 for charge conservation.

The charge Qgs or Qgd is 0 when terminal voltage is 0 for charge conservation.
Cap 1 vs. Charge2 Implementation

ADS (Cap and Charge implemented)

1 Cap implementation: DC current can be observed in HB for capacitor
2 Charge implementation, will not produce DC Current via cap.

I\text{cap}=0; \text{Use the charge implementation!!!}

- Cgs:Cap&Charge

  DCgs is small < 3%

- Cgd:Charge&Cap

  DCgd < 1%

\text{Igs with Cap Implementation}

Waveforms for Charge&Cap similar, but not equal.

Cap current is the same order as diode current. Harmonics are correct from the charge implementation!

1-st harmonic, Charge&cap, 2-nd harmonic Charge&Cap, 3-rd Charge&Cap
Small Signal GaN Dispersion Problems
GaN HEMTs are dispersive.

Example: GaAs Model used to model GaN

DC Gm; GaAs Model

;Simulated Mag S21: 3 dB higher with GaAs model

Gm Dispersion GaAs

GdsDispersion GaAs

GdsDispersion GaN

FET model extraction: iltcho.angelov@chalmers.se
Large Signal GaN Dispersion Problems

Red measured, Blue : Model without Knee walkout modeling facilities
GaAsModel used to model GaN

DC Ids vs Vds fit is good using GaAs model

But at RF: **Knee is different!**

1. Solution: using GaAs model: sacrifice the fit at CW to get the RF fit
2. Use the GaN VA model with Bias dependent Rd, Rs, Rdel, Cdel, Kbgate
3. In severe cases, further increase of complexity of the GaN model making additional, RF controlled part of Ids.
4. Improve the passivation and fix the problem, instead spending time to model the problem. It is more important, practical to fix the problem, instead modeling problem.
Dispersion Modeling Implementation

1. Simple approach: $R_c, C_{rf}$ at the output, usually implemented in CAD tools.
   $R_c$ is bias dependent! $R_{c1} = R_{c\min} + \frac{R_c}{1 + \tan p}$


3. Physical Approach: (K. Kunihiro, Y. Ohno, ED, Vol. 43, No. 9)

4. Device is symmetric: output and input dispersion: $R_{cin}, C_{fin}$

From ADS2009; GaN Extended dispersion Modeling
- combined $R_c$, back-gate $R_{del}, C_{del}$: 8 parameters

Severe knee walkout:
$$I_{ds} = (I_{ds_{DCRf}} + K_{RFDC} \cdot I_{dsRF})$$
Sweeping real Zload
50-280 Ohm

Univ. Cardiff, UK first used LSVNA and this approach.

Sweeping real Zload
RF=4 GHz; Pin=14 dBm
GaN DC Ids (red) and dynamic Ids (blue) sweeping real Zload

Sweeping real Zload Pin=14 dBm
Output Power for different impedances

Knee walkout:
2GHz Vmin=0.8V (DCKnee GaAs) 12GHz Vmin=4.5V
18GHz Vmin=6.3V
The high frequency IV slump is accurately modeled with the gate control network Rdel,Cdel

1LSNA & Load-Pull Measurements for Knee walkout problems: GAN FET: Real Load Evaluation!

FET model extraction: iltcho.angelov@chalmers.se

I. Angelov
1. Measured (points) and modeled RF and DC Power Load Pull C-band.

2. Measured and simulated Load Impedances C-band.

3. Measured and modeled Waveforms $V_{ds}=15V$; C-band Harmonic Load pull evaluation.

FET model extraction: iltcho.angelov@chalmers.se
A general purpose large-signal modeling approach for GaAs,GaN FET was proposed, implemented in CAD tools and experimentally evaluated. Thank you for your attention! S.D.GL.

Meyer’s Law, part of Murphy’s Law: 
**It is a simple task to make things complex, but a complex task to make them simple**
Dispersion Treatment Summary

Output Dispersion
Rc, Crf
Rc1 = Rcmin + Rc/(1 + tanp)
Back-gate node

1) In not very severe cases modify only the output conductance Rcmin Rc
2) More advanced (difficult) SS cases when you treat both Gds, Gm - use backgate Kbg - i.e you insert the back gate feedback to the gate voltage control.
3) High frequency delay, mild knee walkout: Rdel Cdel
4) In severe knee walkout cases you need to modify the Ids current - the knee current is dependent on drain and gate at RF. This modification can be done by users, both in the VA implementation or SDD:

\[ \text{Ids} = (\text{Ids}_{\text{DCRF}} + \text{KRFDC} \times \text{Ids}_{\text{RF}}) \]

\[ \text{Ids}_{\text{DCRF}} = \text{IPK0} \times (1 + \tanh(x1p)) \times \tanh(\text{Alpha}p \times \text{Vds}) \times (1 + \text{LAMBDA} \times \text{Vds} + \text{LSB0} \times \exp(\text{Vdg} - \text{VTR})) \]

\[ \text{Ids}_{\text{RF}} = \text{IPK0} \times (1 + \tanh(x1p)) \times \tanh(\text{Alpha}p \times \text{Vrf}) \times (1 + \text{LAMBDA} \times \text{Vrf}) \]

\[ \text{Vpkm} = \text{Vpkm} - D_{VKS} + D_{VPKS} \times \tanh(\text{ALPHA} \times \text{Vds}) - V_{SB2} \times (\text{Vdg} - V_{TR})^2 - V_{bg} \]
Common mistakes

1. Too much input power when doing S-parameters, S21 is compressed. The input power should be small (typ-40dBm), should not change DC current. Take a look in the ICCAP modeling book (Franz Sischka) for the golden rules.

2. Resistances in the bias lines not measured.

3. Gate current Igs not monitored or Igs compliance too low.

4. When working with dispersive devices like GaN a separate
   a) Ids vs Vgs, (Vds parameter)
   b) Ids vs Vds (Vgs parameter) measurements should be made.

Measured Ids vs. Vds, Vgs parameter
   a) stepping up with Vds - triangles,
   b) stepping Vds down - cross.

For GaN devices, depending on the starting point, direction (up or down) Ids can differ >10%
We can use resistors to limit & define safe currents levels. The same resistors used in the CAD tool to extract models for breakdown.

1 Common Gate Device: we split the GS, GD Junctions:

- Gate -Drain breakdown measurement setup

\[ \text{Rmeas} = 1 \, \text{kOhm} \text{ defines the current in the measurement path} \]
\[ \text{Rcon} = 1 \, \text{MOhm} \text{ defines the current in the connected path.} \]

**Injected current <0.1mA/mm for safety!!!**

- Gate -Source breakdown measurement setup.

2 For Common Source Device:

Source without via, using needles.

FET model extraction: iltcho.angelov@chalmers.se
1 Capacitance implementation: we don’t need transcapacitances! Cap directly from SS extraction!

2 The Cap. Functions should be well defined: \(-\infty < x < \infty\).

\[
\psi_1 = P_1 + \frac{1}{11} V_{x_1} + \frac{1}{111} V_{x_2} \quad \psi_2 = P_2 + \frac{1}{21} V_{x_2}
\]

\[
C_{gd} = C_{gdp} + C_{gdo} (1 + \tanh[\psi_3]) (1 + \tanh[\psi_4] + 2P_{111})
\]

High voltage effects for \(C_{gs} & C_{gd}\) cross-coupling from \(V_{ds}\) - \(P_{111}\)

\[
HB: \frac{\partial V_{gs}}{\partial t}; \frac{\partial V_{gd}}{\partial t}; 2I_{gsc} = \frac{\partial V_{gs}}{\partial t} C_{gs}; I_{gdc} = \frac{\partial V_{gd}}{\partial t} C_{gd}
\]

2 Charge Implementation:

\[
Q_{gs} = \int C_{gs}(V_{gs}, V_{ds}) dV_{gs} = C_{gsp} V_{gs} + C_{gs0} (V_{gs} + Lc_1) Th_2
\]

\[
Q_{gd} = \int C_{gd}(V_{gs}, V_{gd}) dV_{gd} = C_{gdp} V_{gd} + C_{gdo} (V_{gd} + Lc_4) Th_3
\]

\[
Lc_1 = \frac{\log[\cosh[\psi_1]]}{P_{11}}; \quad Th_2 = \tanh[\psi_2]; \quad Lc_4 = \frac{\log[\cosh[\psi_4]]}{P_{41}}; \quad Th_3 = \tanh[\psi_3]
\]

Total Charge Implementation \(Q_g = Q_{gs} + Q_{gd}\)

Integration vs. terminal voltage! Remote voltage parameter!

We will always have some difference in the simulated S-parameters using capacitance or charge implementation, using the same coefficients!

> S. Maas Nonlinear Microwave Circuits
Extraction & Fit IV parameters flow

Summary:

1. **On** resistance Ron Extraction. Ron = Rs + Rs + Rch
2. **Igs** parameter extraction and fit.
3. Extraction of **lambda** (slope Ids vs. Vds at high Vds, above the knee.
4. Extraction, fit Iknee with **Ipk0** (Isat/2), **P1** = Gm/IPks, Vpks
6. Thermal resistance fit **R_{therm}**.
7. Fit Gm with **P1**
8. Extraction of second **P2** and third derivative **P3** parameters.
   Repeat the procedure 4-8, because parameters are interdependent
9. Global IV optimization. Typical, at this point fit <2-5%.
10. Breakdown parameter for Ids, Igs (optional) followed by Global IV optimization

Implemented in ICCAP2013
Cap Direct extraction using the CAD tool.

Cgs, Cgd extracted directly using the CAD tool.

Small Signal extraction good papers: Dambrine, Berroth, Manohar, Sommer, Shirakawa, Campbell

FET model extraction: iltcho.angelov@chalmers.se
The active, injection based harmonic load-pull measurement setup.

It is very fast & accurate!
The amplifier at the output should provide enough power to compensate circulator & cable losses (2-3 dB).

$$P_{IN} = \frac{|a_1|^2}{2Z_c}; \quad P_{OUT} = \frac{|b_2|^2 - |a_2|^2}{2Z_c}; \quad \Gamma = \frac{a_2}{b_2};$$

where $Z_c$ is the system impedance.

The circulator separates the injected and outgoing wave, terminating $b_2$ in a 50 Ω load. This gives full control of $\Gamma_L$ seen by the DUT at $f_0$, according to:

$$\Gamma(f_0) = \frac{a_2(f_0)}{b_2(f_0)} = \frac{A(V_I, V_Q)e^{j(\omega_0 + \theta(V_I, V_Q))}}{b_2(f_0)}$$
Self-heating is usually modelled with a single thermo-electrical circuit $R_{therm} \cdot C_{therm}$.

With temperature coefficients $Tc_{Ipk}, Tc_{P1}$ known, there is only one thermal parameter to find $> R_{therm}$. This is done in the CAD, at high $P_{dc}$:

1. Fit accurately $I_{ds}$ at the knee (current parameters), 2. Adjust $R_{therm}$ to fit the slope $I_{ds}$ vs. $V_{ds}$.

Accurately, thermal resistance can be found measuring junction temperature $T_j$ with infrared microscope. $T_j = R_{therm} \cdot P_d + T_{amb}$

**$R_{therm}$ is not constant with temperature.** For high dissipated power $> 10 \text{W}$ should be considered: $R_{therm}(T) = R_{therm}(1 + TcR_{therm} \cdot DT_j)$.

The thermal capacitance $C_{therm}$ model the thermal storage capacity of the structure. We can have different $R_{therm}$ and $C_{therm}$ for the chip $R_{thermchip}, C_{thermchip}$ and for package $R_{thermpackage}, C_{thermpackage}$ for high power devices.

FET model extraction: iltcho.angelov@chalmers.se
For LS & Harmonics modeling we need correct derivatives. Self-Heating, Dispersion, Memory effects, complicate the picture.

**DC data for I_ids derivatives are noisy! Solution:**

1. Power Spectrum Evaluation (PS) using Spectrum Analyzer, or LSVNA;
2. Load Pull, Waveforms LSNA or
3. Combined Load Pull & LSNA Waveform Evaluation!!

**Pin, RF freq, Vds Constant.**

1. **Low RF** - evaluation of I_ds current source
2. **High RF** - capacitances

**Procedure for PS:**

1. Calibrate input power at DUT (Pin=0 dBm GaAs, 10-14 dBm for GaN SiC) at the device terminal for fund. and harmonics.
2. Calibrate losses of output cables, diplexer, etc. **Keep attenuators directly at the bias tees, close to DUT!!**
3. Measure 1,2,3 harmonics sweeping Vgs(10pts), Vds (14V, 28V..for GaN, SiC; Vds=0.1;3V, GaAs)

---

**PS: GaN C-band and X-band Measured and modeled**
Accurate Modeling of GaAs & GaN HEMT's for Nonlinear Applications

Part II: A quick overview of the Angelov-GaN model parameter extraction

Innovations on EDA Webcasts

Agilent EEsot EDA

Dr. Roberto Tinti, Ph.D.
Product Manager, Device Modeling
May 7, 2013
Angelov-GaN Extraction with IC-CAP

**Measure**
- DC Measurements
- SP Measurements
- (Large Signal Measurements)

**Extract**
- Parasitic Extraction
- DC Extraction
- AC (CV and SP) Extraction
- (LS Extraction / Verification)
Recommended Extraction Flow

- Reset / Initialize Parameters
- De-embed Data
  - Update Measured Data (inc. de-embedding)
  - Extract System Series Resistance
- Extract Rx_Lx with Cold FET
- Extract/Tune Gate Current
- Extract/Tune DC idvg
- Extract/Tune DC idvd
- Tune DC idvg/idvd
  - Repeat until getting medium level fit
- Extract/Tune SP
  - Extract CV parameters
- Tune SP
  - Repeat until getting medium level fit
- Tune Temp DC/SP

- Large Signal Verification

- Extraction Flow
  - Reset Parameters to Defaults (defined in Circuit)
  - Initialize Parameters and Boundaries for Extraction
  - Update All Measured Data for Extraction (It will take time)
  - PreDC Port1
  - PreDC Port2
  - SP Cold FET
  - DC gate diode forward
  - DC gate diode reverse
  - DC idvg
  - DC idvd
  - DC idvg
  - DC idvd
  - DC idvg
  - SP vg at vd0 A1
  - SP vd at vg0
  - SP vg at vd0 A1
  - SP vd at vg0
  - SP vd at vgm2
  - Save Parameters
DC Extraction (Forward Gate current)

Tips:
✓ Measure Gate Forward Diode characteristics.
✓ Sweep Vg up to the level where enough current flows to get Gate resistance.
✓ Measure 3 Vds points around Vd=0 to check the device behavior.
DC Extraction (Drain current, Id-Vgs)

Tips:
✓ Measure Drain current with Gate Voltage sweep.
✓ Include negative Vg region where Gate leak current is observed.
✓ Include Gmmax point and falling down region.
Self Heating Effect Modeling

Use RTH (and CTH) to model the dynamic thermal effect.

Slope at low power is positive: $\Rightarrow \text{Lambda}$

Slope at high power is negative: $\Rightarrow \text{RTH (Rtherm)}$

Pulsed IV measurements, when available, can give isothermal results, avoiding the self heating effect. (Pulse width < 100-200 nsec) However, dispersion problems may be observed.

Negative slope at high dissipated power is due to self heating of the device. This effect is modeled with a thermal network.

Reference:
I.Angelov “Compact Equivalent Circuit Models for GaN, SiC, GaAs and CMOS FET”, MOS-AK Baltimore Dec9
SP Tuning Example

**capacitances**

S-parameters Tips:
- Make sure the signal input level is not too high
- Account for series resistance due to bias tees and cables
SP Tuning Example

gate and collector resistances
SP Tuning Example
Parameter Extraction and Validation with Agilent NVNA Data

**Benefits:**
- Best set of model parameters for a fixed empirical model
- Data under realistic conditions of use
- Validation for free!

**NVNA-based device characterization**

**Dynamic Load-line Waveform meas.**

DC-IV, S-pars

**Parameter extraction for std. compact model using NVNA data as target**

See [1]
Validation with NVNA Data with IC-CAP and ADS

- Trade-off LS vs SS fits
- Tune parameters for specific applications
- Extract breakdown and other parameters at operating extremes
- Explore model limits

See [2,3]
Summary

• Complete Angelov-GaN extraction flow

• As a optional step, the Agilent NVNA can be used in conjunction with IC-CAP and ADS to verify and improve the accuracy of compact models, such as Angelov-GaN, extracted using traditional linear techniques (DC and S-parameters). The exclusive Harmonic Balance simulation link between IC-CAP and ADS enables model parameters optimization to match large signal data.

Acknowledgements

• Takashi Eguchi, Tanigawa Hirohaki, Agilent Technologies
• David Root and Franz Sischka, Agilent Technologies

References:


2. F. Sischka, "Improved compact models based on NVNA measurements", European Microwave Week 2010, Paris, Workshop WFS06 (EuMC/EuMIC) 'Silicon Characterization from MHz to THz'.

Where to find more information about today’s content:

Angelov-GaN paper library at Chalmers University:
- Angelov-Model-Library-at-Chalmers

IC-CAP and Angelov-GaN extraction package:
- www.agilent.com/find/eesof-iccap

ADS and supported foundry libraries:
- www.agilent.com/find/eesof-ads
- www.agilent.com/find/eesof-foundries

Non-linear verification with Agilent NVNA
- Future Device Modeling Trends by David Root
- See also reference papers on slide 12
Appendix
The Agilent IC-CAP W8533EP Angelov-GaN Extraction Package
Choose VerilogA directory and Working directory.
VerilogA Model for Simulation

File Location: **(ADS Install Dir)/veriloga**

File Name: **angelov_gan.va**

angelov_gan.va in ADS2009U1 **(not supported)**
in ADS2011.10 **(supported)**
in ADS2012.08 **(supported)**
Pad Open/Short Measurement

OPEN measurement settings

SHORT measurement settings

De-embed data manage

De-embed
De-embedding Set

Open S-parameters

Short S-parameters

If you don't use the de-embedding function in the toolkit, set **Ideal Open and Short** for the De-embedding Set.
RF S-Parameter Measurement

- Parameter Measurement
- May 7, 2013

- RF measurement settings
- De-embedding
- .mdm Data import and export
Extraction Flow / Function Editor

Customize Extraction Procedure
- Modify Extraction Flow
- Modify Function Flow
- Add New Function (Function Editor)
Tuner Function

Measurement v.s Simulation

Slider

Parameter | Tuner
--- | ---
amplov:VFKS | 
-0.000 | -1.964 | 0.000

amplov:P2 | 
-10.00 | -267.1m | 0.000

amplov:PS | 
0.000 | 50.27m | 10.00
IC-CAP

• Open and flexible modeling platform
• Turn-key model extraction kits for a broad range of models
• Allow customization to standard extraction routines with Python
• Control your entire modeling process
  – Instrument control for efficient data collection
  – Seamless data transfer
  – Extraction
  – Link to design tools
You are invited

You can find more webcasts
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