Interfacing with HP E 4889A

- what to consider first, how to prepare interconnection
- HP E 4821A #501 Connectivity Kit
- how to get material: Connectors, Cable,...
- Layout Hints & mechanical details
- Electrical characteristics, Transmission Line issues, Grounding
- Signal View
- 3.3 V issues
- HP E 4821A #510 Cable extension
- How to test a Level 2 Device
- Monitoring

Parallel Cell & Traffic Generator and Analyzer  E 4829B
The HP E4889A can run as TX or RX, the assignment is done when system boots.

- Signals are provided on upper and lower connector, the lower connector carries the most important ones.
- Depending on ATM-8 or ATM-16, the data pin assignment changes slightly.
what to consider first, how to prepare interconnection?

- there are two ways to interface to DUT:
  - direct plug-in of POD to DUT evaluation board
  - interface by cable between POD and board
- direct plug in:
  - + rugged, reliable connection
  - - needs room on board, plan before board design
  - see "Layout rules"
- interface by cable
  - provide connector on testboard, less room needed than for direct plug-in
  - use of flexible single wire cable together with probes to adapt to testpads and device pins
The kit contains 4 pieces of each cable shown here.

There are several choices when using cables:

1. using 50 to 50 pin cable for upper and lower connector provides any signal. Requires up to 2x 50 pin header in test board layout.

2. using a 50 to 34 pin cable provides all basic ATM-8 signals (data, SOC, handshakes, clock). So only one small header (34pin) in test board layout is needed.

3. if no header is provided in the testboard layout, the flexible cable ending with 'single wire' can be used. This allows to individually connect into the board or to use the grabbers known from logic analyzer.

Grounding: for best performance all ground wires (black insulation) have to be connected to the test board!

cable length is 20 cm or 8 inch, keep PC board traces to DUT short!
Use of the flexible cable together with grabbers

- The 200 mm long ribbon cable is spliced into single wires after 100 mm with single sockets at the end.
- Single sockets fit to round pins with diameter of .9 to 1.1 mm or square pins 0.6 to 0.8 mm.
- Grabbers are not included in the set.
- The HP through hole grabber tips (P/N 5959-0288, 20 pieces) or surface-mount tips (P/N 5090-4356, 20 pieces) are recommended.
if you want to do cabling yourself, you need:

- 50 pin cable connector:
  - 3M 3425-6650
  - AMP 1- 746286-0 (with strain relief 499252-4)
  - Robinson Nugent IDS-C50PK-TG
  - Thomas & Betts 609-5041
- 34 pin cable connector:
  - 3M 3414-6634
  - AMP 1- 746286-8 (with strain relief 499252-6)
  - Robinson Nugent IDS-C340PK-TG
  - Thomas & Betts 609-3441
- 50 wire cable:
  - 3M 3365/50
- 34 wire cable:
  - 3M 3365/34
Layout Hints (1)

- There are two ways to include connection of Pods to a board:
  - a) Edge wise, position connectors on the tip of a tongue
  - b) Place it inside a board, but provide cut-throughs for Pod connectors. The cut-throughs can be omitted, when the ejectors are removed from Pod connector.

P/N of mating part: 3M: 8550-4500, SJ 50 pin

Application Note: Interfacing, Slide 7
Layout Hints (2)

upper con.
pin 1 to pin 50:

lower con.
pin 51 to pin 100:

top view
(component side)
to connection area
on test board

Application Note: Interfacing, Slide 8
HP E4889A Mechanical Details

Application Note: Interfacing, Slide 9

All Dimensions in mm
Signals at connector of HP E4889A

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
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<td>100</td>
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- Note: the pins HS_in and HS_out change definition depending on operating mode:

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<tr>
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<th>TX ATM</th>
<th>RX ATM</th>
<th>TX PHY</th>
<th>RX PHY</th>
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<td>HS_in</td>
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<td>RXClav</td>
<td>TXEnb</td>
<td>RXEnb</td>
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<td>HS_out</td>
<td>TXEnb</td>
<td>RXEnb</td>
<td>TXClav</td>
<td>RXClav</td>
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</tbody>
</table>

Application Note: Interfacing, Slide 10
All Pod signals in and out are driven from ABT technology (74ABT16601). All signals have serial resistor of 21.5 Ohm for ESD and short protection.

- Bus transceiver DC parameters:
  - $V_{oh} = 2V$ @ $I_{oh} = 32 mA$
  - $V_{ol} = 0.55V$ @ $I_{ol} = 64 mA$
  - $V_{ih} = 2V$ @ $I_{i} = 20 uA$
  - $V_{il} = 0.8V$ @ $I_{i} = 20 uA$

- Capacitive budget:
  - 9pF bus transceiver pin + 10 pF Pod layout + 10 pF cable (.5pF/cm)
  - TX: test device input capacity up to 30 pF possible
  - RX: test device will be loaded with 30 pF/(20pF) when connecting with 20cm cable/ (direct plug-in)

- AC Characteristics:
  - TX: together with the serial resistor the source impedance is 50hm typically.
  - RX: the input is high impedance
Transmission Line?

- 20cm cable length, do you have to worry about transmission line effects? **The answer is YES:**
  - transceiver's $tr, tf = 1.5$ to $3\text{ns typ}$
    - signals can get excessive overshoot and ringing if there is no proper grounding and isolation
  - $tr,tf > tpd \rightarrow$ neglect reflections by TML effects
  - signal speed: $30\text{cm/ns in air}, 15\text{cm/microstrip (Er=4.5,)},$ ribbon cable $\sim 20\text{cm/ns (Ereff=2.5), tpd(cable) = 1ns}$
  - due to AC impedance (typically $50\text{Ohm}$), any signals reflected back to output will be terminated
Transmission Line & Wiring Techniques

- Any test board layout should make use of stripline or microstrip design. This means that the signal traces run over a ground plane or between planes, while the geometry (line width and height over ground) and the material define the impedance.
  - for the line impedance chose any value from 50 to 100 Ohm, all lines should have same impedance
  - the lines should be short but have similar length
  - for reasonable decoupling between lines ensure a separation of at least 2x line width between lines
- When hand wiring:
  - use a pc board with a copper plane, wire all ground pins to this plane as short as possible, keep the individual wires for each signal routing close above the board's surface
  - when using a board without copper plane, use coaxial or twisted pair cable for wiring. Connect all ground pins of the test device together like a mesh. Connect all ground pins of test connector together like a rail. Connect coax shield/2nd wire of twisted pair on both ends to the ground mesh/rail as short as possible.

Another issue to take care is device supply pins: ensure sufficient decoupling capacitors to provide energy needed in simultaneous switching outputs. For best decoupling provide always a set of capacitors (100pF, 1nF, 100nF) due to frequency dependent impedance.
The following pictures show data signal at Pod output with load 15pf: 30pF:

The left picture is similar also for Receiver's internal signal, when connected directly.
Signals at 20cm Cable End

- The following pictures show data signal at Cable End with add. load 15pf: 30pF:
- The left picture is similar also for Receiver's internal signal when connected via 20cm cable.
How to connect on my board, if there's no room for a connector?

- hp offers a family of PQFP Probes, together with Adapters for signal connection:

<table>
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<tr>
<th>Pin Count</th>
<th>Probe</th>
<th>Adapter, rigid</th>
<th>Adapter, flexible</th>
</tr>
</thead>
<tbody>
<tr>
<td>160 pin</td>
<td>E5319A</td>
<td>E5330A</td>
<td>E5316A</td>
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<tr>
<td>184 pin</td>
<td>E5343A</td>
<td>E5330A</td>
<td>E5316A</td>
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<td>208 pin</td>
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<td>240 pin</td>
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<tr>
<td>304 pin</td>
<td>E5331A</td>
<td>E5333A</td>
<td></td>
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</tbody>
</table>

- other vendors of Probes for various IC packages:
  - ITT Pomona
  - ET (Emulation Technology)
How to interface to 3.3V

- The diagram is taken from TI's data book on ABT
  - There are two ways to protect 3.3V logic:
    1. by clamping with a Schottkey diode to 3.0V
    2. by an additional 55 Ohm Resistor to Gnd

- Calculation of resulting Hi-Level:
  - Pod internal 21.5 Ohm
    - dc: 55/(55+21.5) x 3.0V = 2.15V
    - ac: 55/(55+21.5) x 5.0V = 3.6V
  - so this should provide proper hi-level as well as sufficient protection

![ABT output circuitry](image)

DC: RL = 76 Ohm
The HP E4821A #510 is a cable extension to the connection between module (HP E4821A) and Pod (HP E4889A).

- It increases the length from 1 to 2m.
- Included are: 2x cable and 2 x adapter for connecting two cables together.
- It is not recommended to use more than one extension to maintain maximum operating frequency.
How to test a Level 2 Device with Level 1 solution

- IUT is ATM Layer device:
  - Transmitter: The test-system will supply all cells deterministically dedicated from any port. So as long as the IUT is able to receive cells, a loading with 100% traffic is possible.
  - Receiver: So the test-system does not participate in polling and selecting, it receives cells dedicated for any port maintaining all features for cell and traffic analysis.
  - The analysis of IUT's proper polling and selection handling is not possible.
Monitoring means to listen to a connection between ATM Layer device and Physical Layer device.

HP E4889A Pod can be used for monitoring as Receiver in Custom Mode:
- at TX while TXenb* = Data Valid (active low) @ HS input pin, without any add. circuitry.
- at RX while (RXempty and RXenb*-1) = Data Valid @ HS input pin, but this needs add. circuitry.

Principle:

- RxEmpty
- RxEnb
- Clock
- Data Valid @ HSin