Test Signals for Multi-Input Digital Devices

| | | | | | | | Multi-phase clocks
| | | | | | | |
| | | | | | | |
| | | | | | | |

0010110011001010011011111111 Parallel data
0111111011001010011011111111
1100000001111000001111100100

| | | | | | | | 3- and 4-levels
| | | | | | | |
| | | | | | | |

| | | | | | | | Glitch simulation
| | | | | | | |

Foreword

Compact, convenient, flexible

Designed for characterizing digital circuits in the lab and in the automatic test environment, the Agilent 8110A pulse generator has extensive functionality and high parametric performance. Its small size and weight pair well with Agilent's oscilloscopes so that a powerful stimulus-response tool can be applied rapidly to new problems as they occur.

Through master-slaving, multi-input devices can be stimulated with signals that match the real environment. Low per-channel volume, easy hook-up to systems, and the ability to compensate for skews introduced by test heads and cables, are some of the attributes that make this approach practical and economic.

Applications

CAD emulation can only go so far; thorough characterization under realistic conditions is needed before you can proceed with confidence through the product cycle. For these measurements, repeatable signals are needed that are accurate models of the real ones. This means not only simulating the necessary clocks, control impulses and two- or multi-level data streams, but also the effects of crosstalk, ground-bounce and distortion.

The same Agilent 8110A master-slave setup will generate any of these signal types, even a mix of them. In the case of data, a few extra initialization steps are needed to ensure frame synchronization, but the hardware and connections remain the same. This document therefore focuses on multi-channel clock and pulse applications on the one hand, and multi-channel data applications on the other. It is hoped that this results in a good overview of the possibilities without going into detail of all possible signal mixes.
Part 4: Multi-phase clocks
-----------------------------------

An Agilent 8110A master-slave setup generates accurate clock signals and can also simulate "real life" clocks where phase and duty cycle have been corrupted through the clock distribution path.

The same setup can also generate parallel pulse sequences (and data, too, but this is described later). It's easy to set up phase, duty cycle and squareness of clock signals because these period-dependent parameters can be set up directly. On the other hand, when time intervals are required, a keystroke changes the display to delay and width (or leading edge and trailing edge delays, as required by the application).

In reality, the signals may well be subject to ground-bounce, ringing and crosstalk. To help understand these problems early in design, the Agilent8110A lets you simulate these effects before hardware is completed. This is possible because you can set up an interferance pulse in one channel and combine it internally with a clean waveform in the other. An application of this kind, with say 4 clock phases, two of which with simulated distortion, would be met by a setup with 2 slaves and just 12 inches height. With the appropriate number of Agilent 8110As connected as shown in Appendix B, set the instruments as follows:

Master
- Recall the default settings.
- Set a deskew delay of 26 ns in both channels (this is the typical value of slave propagation delay).

Slave(s)
- Recall the default settings.
- TRG-MODE page: set pulse period to "ext CLK-IN", "leading edge".
- TRG-LEV page: change default value of "CLK-IN: threshold" as follows:
  - One slave: 1.2 V.
  - Two slaves: 0.6 V.
  - Three slaves: 0.6 V for the slave via one splitter, 0.3 V when via two splitters.
  - Four slaves: 0.3 V.

If deskew at the device-under-test is an important consideration, connect the Agilent 8110A outputs to an oscilloscope with the cables you would normally use with the device. Use a slave trigger output to trigger the oscilloscope. Set the master to a fairly low frequency to avoid pulse-position ambiguity, and adjust master and slave delays to "tune out" the skews.

For continuous sequences of higher stability, you can use the master's internal PLL, or External Clock input, instead of the internal oscillator. All that now has to be done is to set the required parameters and enable the outputs. Frequency* (and any other parameters) can now be adjusted any time as needed.

* Frequency and other timing parameters: A glitch may occur when crossing a boundary from one range to another. Synchronization is not impaired. A list of ranges is given in Appendix C so that boundary glitches can be avoided.

Triggered signals, such as clock bursts can be generated by setting the master to one of the following:
- Gated pulses
  Pulse period: VCO or PLL.
  Gate source: Ext Input
- Triggered burst
Pulse period: VCO.
Trigger source: Ext Input or PLL
or:
Pulse period: PLL.
Trigger source: Ext Input.

In a triggered mode, the slave(s) must be switched to "Meas Once" to avoid a false measurement. Use this procedure to initialize:
- Master: set to Continuous mode.
- Slave: go to TIMING page and, with "Per" (or "Freq") value highlighted, select "Meas Once" in the MODIFY panel. Now press Enter to measure the frequency.
- Return the master to the required mode.

If the clock frequency of a triggered sequence is to be adjusted during a measurement, remember that the timing parameters (even if set in terms of phase or % of period) will NOT change with frequency because of the need to operate in "Meas Once" mode.

Part 5: Multi-channel digital signals
--------------------------------------
Digital devices all need "data" of some kind to be tested realistically. Requirements in practice will be manifold: chip control signals, device-triggered sequences, parallel data, RZ or NRZ formats, and 3- or 4-level codes.

The kind of measurement (for example: pattern compare, state or timing analysis, eye-pattern or BER) will also influence the stimulus requirements. These are addressed by the following Agilent 8110A capabilities:
- a pattern mode with an editor that includes prbs,
- internal or external starting and clocking,
- channel addition for multi-level communications codes, plus timing and level capabilities available in all modes.

As an example, consider an 8-bit MUX with chip select and reset inputs. An Agilent 8110A master with three slaves can stimulate not only the eight data lines but also -thanks to the strobe channels- the control lines as well.

With the appropriate number of Agilent 8110As connected as shown in Appendix B, set the instruments as follows:
Master
- Recall the default settings.
- Set a deskew delay of 26 ns in both channels (this is the typical value of slave propagation delay).
Slave(s)
- Recall the default settings.
- TRG-MODE page: set pulse period to "ext CLK-IN", "leading edge".
- TRG-LEV page: change default value of "CLK-IN: threshold" as follows:
  - One slave: 1.2 V.
  - Two slaves: 0.6 V.
  - Three slaves: 0.6 V via one splitter, 0.3 V via two splitters.
  - Four slaves: 0.3 V.

If deskew at the device-under-test is an important consideration, connect the Agilent 8110A outputs to an oscilloscope with the cables you would normally use with the device. Use a slave trigger output to trigger the oscilloscope. Set the master to a fairly low frequency to avoid pulse-position ambiguity, and adjust master and slave delays to "tune out" the skews.

Continuous Sequences
To set up the sequences, proceed as follows:
1. Set master and slaves to Continuous Pattern mode
2. Select the format (RZ or NRZ) needed in each channel.
3. Set all Agilent 8110As to the same pattern length.
4. Enter the data required.
5. Set timing and output values as required.
6. Synchronize as shown in Table 1.
Table 1: Data generator synchronization

| - Set master to "Triggered Pattern" and "Trg'd by: MAN key" (the object of this is to stop the master so that no clock pulses get to the slaves during this synchronization).  
| - Set the master to Burst mode, then back to Triggered Pattern mode.  
| - Set the slave(s) to Burst mode, then back to Pattern mode (this and the previous step clears all the address counters so that all channels will start at bit 1 on the first clock).  
| - Enable all outputs.  
| - Set the master to the required mode:  
|   - "Continuous Pattern"  
|   or "Triggered Pattern" / "Trg'd by: PLL"  
|   or "Triggered Pattern" / "Trg'd by: EXT-IN"  

For continuous sequences of higher stability, you can use the master's internal PLL, or External Clock input, instead of the internal oscillator.

Triggered Sequences

As implied by the last step of Table 1, externally or internally (PLL)-triggered patterns are also feasible. In the case of externally-triggered patterns, the PLL can be used as the period source for higher accuracy. Here, two important conditions must be observed:

a) The start is asynchronous, that is, after the external trigger, the master will wait until the next available clock edge (or next-but-one if the first edge happens to be masked by the trigger pulse). The advantage of this mode -apart from better frequency stability and accuracy- is that the period settling time is zero.

b) The slaves must operate in the "measure frequency once" mode because continuous measurement of a gated clock would lead to a false result.

To set up a triggered pattern:

1. Set master and slaves to Continuous Pattern mode.
2. Go to the Timing page of each slave and, with "Per" (or "Freq" highlighted, select "Meas Once" in the MODIFY panel. Now press the Enter key(s) so that each slave measures the incoming clock frequency from the master. Return the master to the required mode.
3. Select the format (RZ or NRZ) needed in each channel.
4. Set all Agilent 8110As to the same pattern length.
5. Enter the data required.
6. Set timing and output values as required.
7. Synchronize as shown in Table 1.

If the clock frequency of a triggered sequence is to be adjusted during a measurement, remember that the timing parameters -even if set in terms of phase or % of period- will NOT change with frequency because of the need for "Meas Once" mode.

Note also that triggered and continuous patterns lose synchronism when a boundary from one frequency or other timing range to another. A list of ranges is given in Appendix C so that loss of synchronism can be avoided. If a boundary is crossed, perform the synchronization procedure of Table 1. Any change of data in the programmed pattern will cause loss of synchronization, too. If data is changed, perform Table 1.

Part 6: Some application tips
Here are some examples showing how the Agilent 8110A's features in master-slave operation solve demanding stimulus requirements.

Double-frequency auxiliary clock

Generally, master and slaves will be operated in the same mode (examples: multi-phase clock, parallel data applications). However, there is nothing to prevent one or more of the slaves being operated in pulse mode when the master and other slaves are in data mode. An example is shown in Figure 2 where a double-pulse is generated on each bit of master data.

Master (data)

```
X X X X X X X X
```

Slave (double pulse)

```
| | | | | | | | | |
```

Figure 2: Generation of double-frequency square wave (for clarity, pulses are shown before width and spacing have been equalized).

Accurate downstream trailing edge placement

The above technique can also be used when trailing edges in one channel must be placed critically relative to the data in others. This overcomes the incremental nature of trailing-edge position in NRZ (non-return zero) data format, relative to the leading edge. Further, a slave may be clocked from a strobe output instead of the clock output when a single event is needed in the data cycle.

Master, pattern mode:

Output:

```
X X X X X X X X
```

Strobe out

```
| | | | | | | | |
```

Slave (pulse mode):

Output 1 (single pulse):

```
: Delay
:--------->:
: |
:---Width-->:
```

Output 2 (double pulse, complement)

```
:----Double -------->
:----Width----->:
```

Figure 3: Both edges of a pulse event have variable timing and hence can be placed with high resolution anywhere in the data frame.

The above example is taken from a flash-RAM test application and is given here to show some of the potential.

A "third channel" in each Agilent 8110A

Mention has already been made of the strobe output. This has the same data capability as a main output, has selectable TTL/ECL output level and fixed NRZ timing, so can be used to stimulate channels that do not require parametric adjustment. Thus each Agilent 8110A can be regarded as providing an extra channel.
Absolute and period-dependent parameters

Delay, width and transition-time can be entered in period-dependent terms (e.g., phase, duty cycle, % of period) in master and slave instruments as well as in stand-alones.

How does a slave "know" the period value? Simply that one of the functions of the PLL module is to measure the external clock frequency. However, take care if the external clock is not continuous (which is the case if the master is, for example, in burst or gate mode, or in triggered pattern mode) because the "missing" clock pulses will falsify the frequency measurement. To help solve this problem, there is a "count once" mode which can be implemented when the system is initialized.

APPENDIX A: Modules needed in the Agilent 8110As

Whether your application needs several pulse channels, multi-phase clocks or parallel data patterns, the same hardware setups apply. These consist of a master with up to four slaves. The instrument configurations are:

Master Agilent 8110A:
- An Agilent 8110A mainframe.
- Two Agilent 81103A channel modules.
- An Agilent 81107A deskew module. This module compensates for slave propagation time by delaying the two master channels by an appropriate amount (typically about 24 ns).
- Optional: an Agilent 81106A PLL module for enhanced master/slave clock accuracy. Also allows synchronization to an external clock.

Slave Agilent 8110As
- An Agilent 8110A mainframe.
- Two Agilent 81103A channel modules.
- An Agilent 81106A PLL module, essential for synchronizing to the master.
- Optional: an Agilent 81107A deskew module. This module is more essential the higher the frequency. It allows differences in set-up and test-head propagation times to be compensated at the device-under-test.

APPENDIX B: Connections and accessories needed

For all applications - that is, multi-channel clock, pulse and data requirements - a slave is synchronized to the master by connecting the master's Trigger output to the slave's Clock input.

For clean triggering, it is important to connect with 50-ohm components and to ensure that all slave Clock inputs are set to 50-ohm. Depending on the number of slaves, one or more power splitters are needed to preserve a 50-ohm match throughout the clock distribution. This number of splitters determine the threshold level to which the slave Clock inputs should be set. These details are shown below for setups consisting of 2, 3, 4 and 5 instruments.

Two Agilent 8110As: 4 full channels 2 strobes
---------------------------------------------
- one master and one slave,
- one 61 cm, 50-ohm coax cable (Agilent 8120-1839).

Master Agilent 8110A Slave Agilent 8110A
Trigger Out <--------------------------> Clock In (rear panel)
(TTL levels 61-cm BNC selected) (50 ohm, cable 1.2 V threshold)

Three Agilent 8110As: 6 full channels 3 strobes
-----------------------------------------------
- one master and two slaves,
- one 61 cm, 50-ohm BNC coax cable (Agilent 8120-1839),
- one BNC f-f adapter (Agilent 1250-0080),
- one adder/splitter (Agilent 15104A, passive 50-ohm delta network),
- two 30 cm, 50-ohm BNC coax cables (Agilent 8120-1838).

Four Agilent 8110As: 8 full channels 4 strobes
---------------------------------------------------------------------
- one master and three slaves,
- one 61 cm, 50-ohm BNC coax cable (Agilent 8120-1839),
- one BNC f-f adapter (Agilent 1250-0080),
- two adder/splitters (Agilent 15104A, passive 50-ohm delta network),
- three 30 cm, 50-ohm BNC coax cables (Agilent 8120-1838).

Five Agilent 8110As: 10 full channels 5 strobes:
---------------------------------------------------------------------
- one master and four slaves,
- one 61 cm, 50-ohm BNC coax cable (Agilent 8120-1839),
- one BNC f-f adapter (Agilent 1250-0080),
- three adder/splitters (Agilent 15104A, passive 50-ohm delta network),
- four 30 cm, 50-ohm BNC coax cables (Agilent 8120-1838).

APPENDIX C: Timing ranges
### Width ranges

<table>
<thead>
<tr>
<th>Width</th>
<th>2.4ns</th>
<th>9.99ns</th>
<th>10ns</th>
<th>99.9ns</th>
<th>100ns</th>
<th>999ns</th>
<th>1us</th>
<th>9.99us</th>
<th>10us</th>
<th>99.9us</th>
<th>100us</th>
<th>999us</th>
<th>1ms</th>
<th>9.99ms</th>
<th>10ms</th>
<th>99.9ms</th>
<th>100ms</th>
<th>999ms</th>
</tr>
</thead>
</table>

### Delay ranges

<table>
<thead>
<tr>
<th>Delay</th>
<th>0ns</th>
<th>9.99ns</th>
<th>10ns</th>
<th>99.9ns</th>
<th>100ns</th>
<th>999ns</th>
<th>1us</th>
<th>9.99us</th>
<th>10us</th>
<th>99.9us</th>
<th>100us</th>
<th>999us</th>
<th>1ms</th>
<th>9.99ms</th>
<th>10ms</th>
<th>99.9ms</th>
<th>100ms</th>
<th>999ms</th>
</tr>
</thead>
</table>

### Double pulse ranges

<table>
<thead>
<tr>
<th>Double pulse</th>
<th>4.3ns</th>
<th>9.99ns</th>
<th>10ns</th>
<th>99.9ns</th>
<th>100ns</th>
<th>999ns</th>
<th>1us</th>
<th>9.99us</th>
<th>10us</th>
<th>99.9us</th>
<th>100us</th>
<th>999us</th>
<th>1ms</th>
<th>9.99ms</th>
<th>10ms</th>
<th>99.9ms</th>
<th>100ms</th>
<th>999ms</th>
</tr>
</thead>
</table>

### PLL frequency ranges

<table>
<thead>
<tr>
<th>PLL frequency</th>
<th>160MHz</th>
<th>80MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>79.99MHz</td>
<td>40MHz</td>
<td></td>
</tr>
<tr>
<td>39.99MHz</td>
<td>20MHz</td>
<td></td>
</tr>
<tr>
<td>19.99MHz</td>
<td>10MHz</td>
<td></td>
</tr>
<tr>
<td>9.999MHz</td>
<td>5MHz</td>
<td></td>
</tr>
<tr>
<td>4.999MHz</td>
<td>4MHz</td>
<td></td>
</tr>
<tr>
<td>3.999MHz</td>
<td>2MHz</td>
<td></td>
</tr>
<tr>
<td>1.999MHz</td>
<td>1MHz</td>
<td></td>
</tr>
<tr>
<td>999.9kHz</td>
<td>800kHz</td>
<td></td>
</tr>
<tr>
<td>799.9kHz</td>
<td>400kHz</td>
<td></td>
</tr>
<tr>
<td>399.9kHz</td>
<td>200kHz</td>
<td></td>
</tr>
<tr>
<td>199.9kHz</td>
<td>100kHz</td>
<td></td>
</tr>
<tr>
<td>99.99kHz</td>
<td>80kHz</td>
<td></td>
</tr>
<tr>
<td>79.99kHz</td>
<td>40kHz</td>
<td></td>
</tr>
<tr>
<td>39.99kHz</td>
<td>20kHz</td>
<td></td>
</tr>
<tr>
<td>19.99kHz</td>
<td>10kHz</td>
<td></td>
</tr>
<tr>
<td>9.999kHz</td>
<td>8kHz</td>
<td></td>
</tr>
<tr>
<td>7.999kHz</td>
<td>4kHz</td>
<td></td>
</tr>
<tr>
<td>3.999kHz</td>
<td>2kHz</td>
<td></td>
</tr>
<tr>
<td>1.999kHz</td>
<td>1kHz</td>
<td></td>
</tr>
<tr>
<td>999.9Hz</td>
<td>800Hz</td>
<td></td>
</tr>
<tr>
<td>799.9Hz</td>
<td>400Hz</td>
<td></td>
</tr>
</tbody>
</table>
399.9Hz 200Hz
199.9Hz 100Hz
99.99Hz 80Hz
79.99Hz 40Hz
39.99Hz 20Hz
19.99Hz 10Hz
9.999Hz 8Hz
7.999Hz 4Hz
3.999Hz 2Hz
1.999Hz 1Hz
999.9mHz 800mHz
799.9mHz 400mHz
399.9mHz 200mHz
199.9mHz 100mHz
99.99mHz 80mHz
79.99mHz 40mHz
39.99mHz 20mHz
19.99mHz 10mHz
9.999mHz 8mHz
7.999mHz 4mHz
3.999mHz 2mHz
1.999mHz 1mHz

Part 1.10.

APPENDIX D: Automatic synchronization

The following program in HPBasic automates the procedure in Part 5 for synchronizing digital patterns. It also handles data loading.

```
10 !Master/slave: data loading and sync routine
20 CLEAR SCREEN
30 ASSIGN @Pm TO 711
40 ASSIGN @Ps TO 712
50 CLEAR @Pm
60 CLEAR @Ps
70 OUTPUT @Pm;"*RST"
80 OUTPUT @Ps;"*RST"
90 
100 ! Master settings:
110 OUTPUT @Pm;":TRIG:COUN 50;:DIG:PATT ON" ! 50-bit pattern, pattern mode.
120 OUTPUT @Pm;":ARM:SOUR IMM;:TRIG:SOUR INT2" ! Continuous cycle, PLL clock.
130 !OUTPUT @Pm;"ROSC:SOUR EXT;EXT:FREQ 10 MHZ" ! Activate if ext frequency ref needed.
140 OUTPUT @Pm;":FREQ 100 MHZ"
150 OUTPUT @Pm;":DIG:PATT:DATA #250400113333333333333331
20000000000000000000000000000"
160 !Data pattern: # =start of block
170 ! 2 = "next 2 characters define block length
180 ! 50 = "block has 50 characters"
190 ! Block characters set consecutive bits (from bit 0)
200 ! into channels 1, 2 or strobe as follows:
210 ! 1 sets a bit in ch1 to 1
220 ! 2 sets a bit in ch2 to 1
230 ! 3 sets same bit in ch1 and ch2
240 ! 4 sets a bit in strobe channel to 1
250 ! 5 sets same bit in ch1 and strobe to 1
260 ! 6 sets same bit in ch2 and strobe to 1
270 ! 7 sets same bit in all channels to 1
280 OUTPUT @Pm;":DIG:SIGN1:FORM NRZ;:DIG:SIGN2:FORM NRZ"
290 
300 ! Slave settings:
310 OUTPUT @Ps;":TRIG:COUN 50;:DIG:PATT ON" ! Pattern count same as master's.
320 OUTPUT @Ps;":PULS:WIDT1 2.4NS" ! Min pulse width....
330 OUTPUT @Ps;":PULS:WIDT2 2.4NS" !.to allow max frequency.
340 OUTPUT @Ps;":PULS:PER:AUTO ONCE" ! Measures master frequency M-Trig Out to S-Clock In.
350 OUTPUT @Ps;":ARM:SOUR IMM;:TRIG:SOUR EXT2" ! Cont cycle. Rear-panel Clock In is source.
360 OUTPUT @Ps;":DIG:PATT:DATA #250400011333333333333331
00000000000000000000000000000"* 
370 OUTPUT @Ps;":PULS:PER:AUTO ONCE"
```
380 OUTPUT @Ps;":DIG:SIGN1:FORM RZ"
390 OUTPUT @Ps;":PULS:DEL1 2NS"
400 OUTPUT @Ps;":PULS:WIDT1 5NS"
410 OUTPUT @Ps;":PULS:WIDT2 5NS"
420 WAIT 1
430 LOCAL @Pm
440 LOCAL @Ps
450 PRINT "Manual adjustments can now be made. When finished,"
460 PRINT "press CONT to synchronize master and slave"
470 PAUSE ! Synch routine. Implement whenever frequency or
pattern are changed.
480 CLEAR SCREEN
490 OUTPUT @Pm;":PULS:DEL1 22.3NS" !Compensates slave prop
500 OUTPUT @Pm;":PULS:DEL2 22.3NS" ! delay. Skip if 81107A
not fitted.
510 OUTPUT @Pm;":ARM:SOUR MAN" ! Stop master
520 OUTPUT @Pm;":DIG:PATT OFF" ! Set master to....
530 WAIT 1
540 OUTPUT @Pm;":DIG:PATT ON" ! ....start at bit 1.
550 ! Set slave to start at bit 1:
560 OUTPUT @Ps;":DIG:PATT OFF" ! Set slave to.....
570 WAIT 1
580 OUTPUT @Ps;":DIG:PATT ON" ! ....start at bit 1.
590 OUTPUT @Pm;":OUTP1 ON;:OUTP2 ON" ! Switch all...
600 OUTPUT @Ps;":OUTP1 ON;:OUTP2 ON" ! ...outputs on.
610 PRINT "Press CONT to start signals"
620 PAUSE
630 CLEAR SCREEN
640 OUTPUT @Pm;":ARM:SOUR IMM" ! Start master
650 PRINT "Master and slave synchronized and active"
660 WAIT 5
670 CLEAR SCREEN
680 PRINT "Re-run program if frequency or pattern are to be
changed."
690 LOCAL @Pm
700 LOCAL @Ps
710 END