Power integrity is more than decoupling capacitors…
The Power Integrity Ecosystem

Keysight HSD Seminar
Mastering SI & PI Design
Signal Integrity

Power Integrity

SI and PI Eco-System
What Does the Power Distribution Network Look Like?

The “Real World” PDN Network

Supply Noise

Ground Noise

Device Detail

Control Loop Feedback – Power Sense

Control Loop Feedback – Ground Sense

V_{ATE\_HCL}

Device

Supply

Cable

PCB Path

Bulk C

Ceramic C

Power Plane

Package

R_{DUT}

R_{cable}

L_{cable}

R_{PCB}

L_{PCB}

R_{bulk}

C_{bulk}

L_{bulk}

R_{ceramics}

C_{ceramics}

L_{ceramics}

R_{plane}

C_{plane}

L_{plane}
Is Target Impedance Really this Simple?

Target Impedance Calculation

\[ Z_{\text{Target}} = \frac{(\text{Power _ Supply _ Voltage}) \times (\text{Allowed _ Ripple})}{\text{Current}} \]

Example:

4 A → 3.3 V VRM → 2 A → 3.3 V Power Plane

\[ Z_{\text{Target}} = \frac{\Delta V}{\Delta I} \]

\[ Z_{\text{Target}(3.3V)} = \frac{(3.3V) \times (5\%) \times 2A}{2A} = 82.5m\Omega \]

“Target Impedance is the goal that designers should hit!!!”

At what frequency? Why is it a target? What is the minimum? Do I need capacitors?
L-C Series Resonance Problem with Capacitors

Impedance Curve

\[ Z = ESR_{cap} + \left( j\omega \times ESL_{cap} - j \frac{1}{\omega \times C} \right) \]

Voltage and current are in phase at \( f_{cap} \)

\[ f_{cap} = \frac{1}{2\pi \sqrt{ESL_{cap} \times C}} \]

Damping factor (D) expresses the sharpness of the transition from C to L. Higher D = slower phase change at \( f_0 \)

\[ D = \frac{1}{2Q} = \frac{ESR_{cap}}{2} \sqrt{\frac{C}{ESL_{cap}}} \]

Series C-R-L Impedance vs. Frequency

- Phase of \( V \) leads \( I \)
- Phase of \( I \) leads \( V \)

V in phase with I
(Pure resistance)
L/C Parallel Resonance Problem in the PDN Design

\[ Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{50\text{nH}}{100\text{uF}}} = 22.4\text{m}\Omega \]

\[ Q = \frac{Z_0}{R} = \frac{22.4\text{m}\Omega}{4\text{m}\Omega} = 5.6 \]

\[ f \approx \frac{1}{2\pi\sqrt{LC}} \approx \frac{1}{2\pi\sqrt{50\text{nH} \cdot 100\text{uF}}} \approx 71\text{kHz} \]

\[ Z_{\text{peak}} = Z_0 \cdot Q = 125\text{m}\Omega \]

\[ \Delta V = \Delta I \cdot Z_{\text{peak}} = 250\text{mV}_{\text{pp}} \]

\[ f_{\text{resonance}} = 70.79\text{kHz} \]

\[ 126\text{m}\Omega \]
Power Delivery Target Impedance

Flat Z at lower frequencies reduces the package/DUT anti-resonance at higher frequencies!

Reference Design does not fit an R/L Model!

R/L model assumes a flat PDN design!
Forced and Natural Response – Time Domain
Spectral Content of the Sink

Digital Switching Spectral Content

- Edge speeds determine the di/dt maximum for Ldi/dt ripple voltage.
- I(t) waveform determines the spectral content, digital patterns have a wide bandwidth (peaks are at odd harmonics of clock rate)
Z is below target, but not flat..... Is this a problem?
3rd resonant peak (52MHz)

2nd resonant peak (1MHz)

1st resonant peak (69kHz)

Several cycles are simulated at the 1st resonant frequency allowing the forced response to grow to maximum amplitude.

The resulting 369mVpk is approximately the sum of the three impedance peaks or 3X the target impedance value.

Steve Sandler – Picotest
Author of *Power Integrity*
Start at the Voltage Regulator Module to Design for Flat PDN

Minimizes the quantity of capacitors to reach target Z

\[ C = \frac{L_{slope}}{Z_{desired}^2} \]

No DeCaps vs. With DeCaps
How to get a flat VRM Impedance

STATE SPACE AVERAGED MODEL

\[ \text{Duty} = T_{on \_ SW1} \cdot F_{sw} \]

\[ V_{out} = V_{in} \cdot \text{Duty} \]

\[ V_{out} = V_{in} \cdot \frac{V_c}{V_{ramp}} \]

State 1: SW1 = On and SW2 = Off

State 2: SW1 = Off and SW2 = On
The PDN Seen as a Series of Networks

1. Passive Network
2. Passive Network
3. Active Network
4. Passive Network

Vref is a dominant noise source, though it is not generally accessible.

Low noise is obtained by:
- Minimizing interaction between network ports [2,3] and [4,5]
- Maximizing isolation between network ports [1,2], [3,4] and [5,6]
- Minimizing self generated noise within each network
All of the Noise Paths are Related

Reverse Transfer - (S12)

Output Impedance - (S22)

PSRR - (S21)

Power Supply Rejection Ratio

Input Impedance - (S11)

Input impedance can be NEGATIVE!
If All are Related, Why Choose Impedance?

Modern circuits are **DENSE...**

6 Output Power Supply

8.5mm

More Power Supplies

8.5mm

72mm²

..and continuously **shrinking**

2013 eGaN

2014 LDO

12mm²

The output capacitor is one place that is almost always available to measure (miniscule though it may be)

AND, as we said, all performance paths are related to impedance
Measuring Impedance

Method is chosen primarily by impedance magnitude

**APPROXIMATE Measurement Ranges**

- 1-port reflection 0.5Ω-2.5kΩ
- 2-port shunt thru 250uΩ-25Ω *
- 2-port series thru 25Ω-1MΩ
- 3-port voltage/current 1mΩ-2kΩ
- Impedance adapters 0.1 Ω-400kΩ

Most Power Integrity Measurements use the 2-port shunt thru method
1-Port Reflect vs 2-Port Shunt Through

2-Port Shunt is a 4-wire sensing method that increases sensitivity

Current Density at 1MHz

Port 1
Injects
Current

Port 2
Measures
Voltage

$Z_{shunt} = 25 \cdot \frac{S_{21}}{1 - S_{21}}$
2-Port Impedance Measurement

\[ Z_{DUT} = 25 \cdot \frac{S21}{1 - S21} \]

Connecting low frequency DC Blocks at the VNA input isolates the 50 Ohm instrument loading from the circuit.

2-Port Probe

J2130A or P2130A

DC Blockers

J2102A

Common Mode Coaxial Transformer -- Ground Loops

In some cases, a 2-port probe can be used, simplifying the connections and getting into small spaces.

1mΩ measurement with and without coaxial transformer
Separating PCB Mounting L from $C_{ESL}$

**MEASURED**

PCB EM MODEL + TUNED C-L-R MODEL

**IDEAL 2-PORT SHUNT THROUGH**

*Shorting the Capacitor Pads to Simulate/Measure the PCB Mounting Inductance*

**0805 Mounting Inductance**

$L_{PCB_{0805}} = 548 \text{ pH}$

$L_{Short} = 362 \text{ pH}$

**Current Density at 10 MHz**
Manufacturer’s Demo PCB – Not Flat, Hard to Measure
VRM Characterization Board for Flat Z Design

IMPROVED DESIGN

9mΩ + 4.2nH

FREQUENCY (Hz)

IMPEDEANCE (OHMS)

SIMULATED vs MEASUREMENT
Measurement Based VRM Modeling

Steve Sandler – PICOTEST

How to Video
http://tinyurl.com/vrm-video

State Space Hybrid Model – LM20143
Switching Transients & Small Signal Impedance

www.keysight.com/find/eesof-sipi-resources
Modern Day PCB's Have Increasing Data Speed and Complexity
– Xilinx KCU105 FPGA Kit

- HDMI: 2.0 = 6Gbps → 3.1 = 10Gbps
- FMC: 2Gbps ~ 10 Gbps
- SFP: 8Gbps → 16Gbps w 64b/66n encoding, QSFP 25 Gbps+
- USB3.0: 5Gbps → 3.1 = 10 Gbps
- DDR4: 3.2Gbps
- PCI-E: 3.0 = 8 Gbps → 4.0 = 16Gbps

9.27 x 5 inch, 16 layers PCB
Modern Applications with Multiple PDNs

Xilinx Kintex VCU105 Board:
Power Planes

15 Major Power Distribution Networks (PDN)

16 Layer PCB
PIPro – DC IR Drop

Voltage and current reported per Via, Sink, VRM and more!

Xilinx KCU105 – VCC1V2 PDN
EM Simulations for Multi-Port PDN PCB Models

64 Port PDN PCB EM Circuit Model
(S-parameter Behavioral Model)

No Capacitors

With Capacitors

ADS PIPro and SIPro

KEYSIGHT TECHNOLOGIES
PIPro – AC PDN Impedance Analysis

Component Model assignment:
- Lumped
- SnP
- Murata
- Samsung
- TDK
- Create custom parts from Schematic models

Easy setup: Filter, drag and Drop Components

+ Full scripting support for setup, simulation and post-processing
PIPro – AC PDN Impedance Analysis
– Decoupling Capacitor Selection in PIPro

Analyze effect of decap model changes without any need to re-simulate

Original PDN Impedance

New Model Selected
PIPro – AC PDN Impedance Analysis
– Decoupling capacitor tuning from schematic

Completely flexible PDN optimization strategy
SI and PI Co-EM Simulation

Power and Signal Nets in the same EM simulation
Vendor Specific IBIS Models to Improve Accuracy

– Xilinx Kintex FPGA and Micron DDR4 IBIS models
Simultaneous Switching Noise (SSN)

- Shows SSN noise voltage at VCCO pin, which is similar to the measured data
  - Both eye width and height are reduced by SSO noise, as expected.
  - \(387.5\text{p} \rightarrow 375\text{p}, \ 510\text{mV} \rightarrow 474\text{mV}\) respectively
SSO Noise Measured Example
– Simultaneous Switching Output Noise (SSON)
SI with PI, PI with SI, and SI PI Co-Simulation

EEsof ADS SIPro and PIPro Integrated EM Simulation

Loss, Delay, Crosstalk
S-Parameters

IR Drop, AC Impedance

EM Behavioral Model
S-Parameters

SI

PI

SI and PI
Want More Resources?

ADS Bundle Used for Power Integrity Analysis:

- **W2222BP Power Integrity Bundle: ADS Core, TransConv, Harmonic Balance, Layout, PIPro**

Signal Integrity & Power Integrity Resources

www.keysight.com/find/eesof-ads-sipi-resources

www.keysight.com/find/eesof-tutorials-signal-integrity

Try it for free for 30 days with absolutely no obligation.

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Thank You!