DRAM Memory
In High-Speed Digital Designs

Presented by:

Micron –
The Worlds Memory Expert & Agilent Partner
Agenda

- Introduction
- Micron overview
- Choosing a memory in high-speed designs
- Micron Memory portfolio and segments
- DRAM volume drivers
- Evolution of DDR, introducing DDR4
- General DRAM design considerations
  - General layout and termination
  - SSO – Simultaneous Switching outputs
  - RPD – Return Path Discontinuities
  - ISI – Intersymbol Interference
  - Crosstalk
  - Vref
  - Pathlength, Cin and Rtt
Micron is the world’s memory expert

Micron R&D, Design Center and Manufacturing Locations
Why is Memory important in High-Speed Digital designs?

• Applications demand specific memory features - Memory now plays a vital role in system performance
  

• Memory is no longer just commoditized & standardized - Making the right memory decisions is critical
  
  • SDR, DDR 1 / 2 / 3(3L) / 4, HMC?
  • Format (component or module type)?
  • Price, availability & quality?
Micron supplies the right Memory……

**DRAM Families**
- SDRAM
- DDR
- DDR2
- DDR3(3L)
- DDR4
- RLDRAM®
- Mobile LPDRAM
- PSRAM/
  - CellularRAM
- HMC

**Solid State Drives**
- Client SSD
- Enterprise SATA
- Enterprise SAS
- Enterprise PCIe

**DRAM Modules**
- FBDIMM
- RDIMM
- VLP RDIMM
- VLP UDIMM
- UDIMM
- SODIMM
- SORDIMM
- Mini-DIMM
- VLP Mini-DIMM
- LRDIMM
- NVDIMM

**NAND Flash**
- TLC, MLC, SLC
- Serial NAND
- Enterprise NAND

**Managed NAND**
- MCP
- eMMC™
- Embedded USB

**NOR Flash**
- Parallel NOR
- Serial NOR

**Phase Change Memory**
- Serial PCM
- Parallel PCM

**Bare Die**
- Multiple technologie

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June 6, 2013
...for every Application.
DDR2/3(3L)/4 SDRAM Volume Drivers

▶ Volume Drivers

- DDR2 – 800MT/s (400MHz CLK), 1Gb and 2Gb
  Backwards compatible with 400/533/667 speeds
- DDR3L – 1600MT/s (800MHz CLK), 2Gb and 4Gb
  Backwards compatible with 800/1066/1333 speeds
- DDR4 – 2133MT/s (1066MHz CLK), 4Gb
  Backwards compatible with 1600/1866 speeds

▶ Power (IDD7/IPP7)

- DDR2 – 396mW (50nm, 2Gb, 800MT/s)
- DDR3L – 339mW (30nm, 4Gb, 1866MT/s)
- DDR4 – 247mW (30nm, 4Gb, 1866MT/s)
## DDR2/DDR3(3L)/DDR4 Feature Highlight

*(see background for full summary)*

<table>
<thead>
<tr>
<th>Features/Options</th>
<th>DDR2</th>
<th>DDR3(3L)</th>
<th>DDR4</th>
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</thead>
<tbody>
<tr>
<td>Voltage (core, /IO)</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
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<td>Vref Inputs</td>
<td>1 - DQs/CMD/ADDR</td>
<td>2 - DQs and CMD/ADDR</td>
<td>1 -CMD/ADDR</td>
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<tr>
<td>VREFDQ Calibration</td>
<td>none</td>
<td>none</td>
<td>Supported/Required</td>
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<td>'tCK_{base} – DLL enabled</td>
<td>125MHz to 400MHz</td>
<td>300MHz to 800MHz</td>
<td>625MHz to 1.6GHz</td>
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<tr>
<td>Data Rate – Mb/s</td>
<td>400/533/667/800 plus1066</td>
<td>800 /1066/1333/1600 plus1866, 2133</td>
<td>1600/1866/2133 /2400/ 2667/3200</td>
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<tr>
<td>DQ Bus</td>
<td>SSTL18</td>
<td>SSTL15</td>
<td>POD12</td>
</tr>
<tr>
<td>ODT Modes</td>
<td>Nominal, Dynamic</td>
<td>Nominal, Dynamic</td>
<td>Nominal, Dynamic, Park</td>
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<tr>
<td>MultiPurpose Register</td>
<td>None</td>
<td>1 Defined, 3 RFU</td>
<td>3 Defined, 1 RFU</td>
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<tr>
<td>VPP Supply</td>
<td>none</td>
<td>none</td>
<td>2.5V</td>
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<td>Bank Group</td>
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<td>none</td>
<td>four</td>
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<td>Data Bus Write CRC</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Data Bus Inversion (DBI)</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Connectivity Test Mode</td>
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<td>none</td>
<td>supported</td>
</tr>
</tbody>
</table>
Self Refresh (IDD6 with ASR, LPASR)
Micron – Rs parts

- DDR2 Range of Commercial Operation
- DDR3, DDR4 Range of Commercial Operation
- DDR2 Self Refresh Range of Operation
- DDR3L Self Refresh Range of Operation
- DDR4 Self Refresh Range of Operation

Temperature Ranges:
- Room Temperature Range
- Reduced Temperature Range
- Normal Temperature Range
- Extended Temperature Range

Temperature Zones:
- 0°C to 25°C
- 25°C to 45°C
- 45°C to 85°C
- 85°C to 95°C

Refresh Rates:
- 1/4x Refresh Rate
- 1/2x Refresh Rate
- 1x Refresh Rate
- 2x Refresh Rate
DDR2/3(3L)/4 Implementation
## For DDR3 SDRAM (22)

<table>
<thead>
<tr>
<th>Title &amp; Description</th>
<th>Secure</th>
<th>ID#</th>
<th>Updated</th>
<th>Type</th>
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</thead>
<tbody>
<tr>
<td>![A Micron/Engicam Case Study: When Versatility and Durability Matter Most:](PDF 1.29 MB)</td>
<td></td>
<td>02/2013</td>
<td></td>
<td>Case Study</td>
</tr>
<tr>
<td>![Industrial and Multi-Market Applications Flyer](PDF 454.13 KB)Our extensive and stable portfolio of IMM-focused memory solutions empower technology developments in automotive, industrial, medical, manufacturing, and other multimarket segments.</td>
<td></td>
<td>02/2013</td>
<td></td>
<td>Product Flyer</td>
</tr>
<tr>
<td>![Why DRAM for Ultrathins](PDF 64.92 KB)Micron’s DRAM portfolio is the industry’s broadest and includes every type and form factor used in today’s ultrathin and Ultrabook designs.</td>
<td></td>
<td>02/2013</td>
<td></td>
<td>Product Flyer</td>
</tr>
<tr>
<td>![Micron Compatibility Guide for Xilinx FPGAs](PDF 119.3 KB)See which Micron memory comes validated on Xilinx platforms.</td>
<td></td>
<td>02/2013</td>
<td></td>
<td>Product Flyer</td>
</tr>
<tr>
<td>![DDR3 Point-to-Point Design Support](PDF 620.19 KB)DDR3 is an evolutionary transition from DDR2.</td>
<td></td>
<td>02/2013</td>
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</tr>
<tr>
<td>![Error Correction Code in SoC FPGA-Based Memory Systems](PDF 361.92 KB)This presentation will examine the potential sources and implications of soft errors and explain an error detection and correction method implemented in Altera and Micron to make embedded systems more resilient to these types of soft errors.</td>
<td></td>
<td>02/2013</td>
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<tr>
<td>![DDR3L SDRAM System-Power Calculator](XLSM 197.81 KB)</td>
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<td></td>
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</table>
General Layout Concerns

- DLL added
  - Clock jitter increasingly important as speeds go up
    Reduces data eye out by 2x the amount of jitter in
- Avoid crossing splits in the power plane
- Low pass VREF filtering on controller helps
- Minimize Vref Noise
- Minimize ISI
- Minimize Crosstalk
Layout and Termination

Guidelines
“Near Perfect” Data-Eye

Jitter=1ps
Unadjusted, Non-terminated Data-Eye

Jitter=129ps  MinSlew=4.1V/ ns

Overshoot

Undershoot

VDD

VSS

Jitter
Terminated Data-Eye

Jitter=32ps  AptACDC=1.11ns  MinSlew=2.1V/ns

- Overshoot
- VIHdc
- VILdc
- 0.75 Vref
- Undershoot
- VIHac
- Hi-Ringback
- Lo-Ringback
- VILac
Layout and Termination

- **Signal Integrity Review**
  - Importance of transmission line theory
    - Today’s clock rates are too fast to ignore
  - Matched impedance line is important for good signaling
    - Mismatched impedance lines result in reflections
    - Termination schemes are used to reduce / eliminate reflections
  - Good power bussing is paramount to reducing SSO
    - SSO reduce voltage and timing margins
  - Decoupling Capacitors need and requirements
Signal Integrity Analysis is paramount to developing cost-effective high-speed memory systems

- Develop timing budget for proof of concept
- Use models to simulate
- Board skews are important and should account for
- ISI, crosstalk, Vref noise, path length matching, Cin and R\textsubscript{TT} mismatch – employ industry practices and assumptions
- Model vias too
- Eliminate RPDs (return path discontinuities)
- Minimize SSO affects
  - Difficult to model
Simultaneous Switching Outputs (SSO)
- Timing and noise issues generated due to RAPID changes in voltage and current caused by MULTIPLE circuits switching simultaneously in the same direction

Problems caused by SSO:
- False triggers due to power/ground bounce
- Reduced timing margin due to SSO induced skew
- Reduced voltage margin due to power/ground noise
- Slew rate variation
Layout and Termination

- Good power bussing is paramount to reducing SSO
  \[ \Delta V = \left( L \cdot \frac{dI}{dt} \right) \]
- Reduce L (power delivery effective inductance)
  - Use planes for power and ground distribution
  - Proper routing of power and ground traces to devices
  - Proper use of decoupling capacitance
    Locate as close as possible to the component pins
- Reduce dI/dt (switching current slew rate)
  - Use the slowest drive edge that will work
  - Use reduced drive strength instead of full drive where possible
Layout and Termination

- RPDs induce board noise and are difficult to model
  - Splits/holes in reference planes
  - Connector discontinuities
  - Layer changes

- Avoid RPDs if at all possible
  - Avoid crossing holes/splits in reference plane
  - Route signals so they reference the proper domain
  - Add power/ground vias to board
    - Especially in dense layer-change areas
  - Place decoupling capacitors near connectors
Layout and Termination

- Intersymbol interference (ISI)
  - Occurs when data is random
    - Clocks do not have ISI
  - Multiple bits on the bus at the same time
    - Bus can’t settle from bit #1 before bit #2, etc.
  - Signal edges jitter due to previous bit’s energy still on the bus
  - Ringing due to impedance mismatches
  - Low pass structures can cause ISI
Layout and Termination

- Minimize ISI
  - Optimize layout
  - Keep board/DIMM impedances matched
    - Drive impedance should be same as Zo of transmission line
  - Terminate nets
    - Termination values should be the same as Zo of transmission line
  - Select high-quality connector
    - Matched to board/DIMM impedance
    - Low mutual coupling
Layout and Termination

- Crosstalk
  - Coupling on board, package, and connector from other signals, including RPDs
    Inductive coupling is typically stronger than capacitive coupling
  - When aggressors fire at same time as victim (e.g. data-to-data coupling):
    Victim edge speeds up or slows down, causing jitter
  - When aggressors do not fire at same time as victim (e.g. data-to-command/address coupling):
    Noise couples onto victim at time of aggressor switching
Layout and Termination

- Minimize Crosstalk
  - Keep bits that switch on same “clock” edge routed together
    Route data bits next to data bits; never next to CMD/ADDR bits
  - Isolate sensitive bits (strobes)
    If need be, route next to signals that rarely switch
  - Separate traces by at least two to three \{preferred\} conductor widths (more accurately, one would define by trace pitch and height above reference plane)
    Example: 5 mil trace located 5 mils from a reference plane should have a 15 mil gap to its nearest neighbors to minimize crosstalk
Layout and Termination

- Minimize Crosstalk (cont)
  - Choose a high-quality connector
  - Run traces as stripline (as oppose to microstrip)
    Not at the cost of additional vias
  - Maintain good references for signals and their return paths
  - Avoid return-path discontinuities (RPD’s)
  - Keep driver, BD Zo, and ODT selections well matched
Layout and Termination

- **Vref Noise**
  - Induces strobe to data skews and reduces voltage margins
  - Power/ground plane noise
  - Crosstalk

- **Minimize Vref Noise**
  - Use widest trace practical to route
    - From chip to decoupling capacitor
  - Use large spacing between Vref and neighboring traces
Layout and Termination

- DDR2 and DDR4 have single VREF input pin
- DDR3(3L) has 2 VREF pins - VREFCA and VREFDQ
  - When the DQs are driving data there is a lot of noise injection onto VREF
    - The DRAM DQ bus is not capturing data when the DQ pins are driving
  - However, the ADDR/CMD buses may latch inputs when the DRAM DQ outputs are driving
    - Noise by DQs driving could adversely affect the ADDR/CMD data
  - By separating these VREF busses, the VREF for ADDR/CMD can be kept quieter
DDR3(3L): VREFCA and VREFDQ can have a common source supply but should be separately routed and decoupled at the DRAM

- Place one decoupling capacitor per DRAM input
  - Use 0.1 uF and or 0.01 uF
- Keep length from decoupling capacitor to the DRAM ball short
  - Use a wide trace
- Use the same reference plane as the related signals
  - For VREFDQ use the DQ buss reference plane
  - For VREFCA use the command and address bus reference plane
Layout and Termination

• Path length Mismatch
  ▪ Path length differences between strobe and data bits
    Also between clock and command/address/control
  ▪ Any mismatch adds strobe-to-data skew
    Check controller, most have adjustment tools to mitigate mismatching

• Minimize Path length Mismatch
  ▪ Balance the mismatch allowed
    Large mismatches results in easier layout rules but reduce timing margin in timing budgets
    Minimal mismatches results in harder layout rules but have minimal impact on timing budgets
Layout and Termination

- **Cin Mismatch**
  - Differing input capacitances on receiver pins
  - Adds skew to input timings

- **R\text{TT} Mismatch**
  - Termination resistors not at nominal value
  - Internal ODT on Data pins have smaller variation than on DDR2
    - They are calibrated (so is DRAM’s Ron)
  - External termination resistor variation must be accounted for
    - Consider one-percent resistors
High-speed signals must maintain a solid reference plane

- Reference plane may be either VDD or ground
- For DDR3 UDIMM systems, the DQ busses are referenced to ground while the ADDR/CMD and clock are referenced to VDD
- All signals may be referenced to ground if the layout allows

Best signaling is obtained when a constant reference plane is maintained

- If this is not possible try to make the transitions near decoupling capacitors
QUESTIONS?
# Develop Timing Budgets

- **Example of a DDR3 Write Timing budget for 2 slots**

<table>
<thead>
<tr>
<th>Element</th>
<th>Skew Component</th>
<th>800</th>
<th>1066</th>
<th>1333</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock</td>
<td>Data/ strobe chip PLL jitter</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td>DRAM tJitter</td>
<td></td>
<td>50</td>
<td>50</td>
<td>45</td>
<td>45</td>
<td>40</td>
</tr>
<tr>
<td>Clock skew</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

| Transmitter              | Memory Controller Skew  | 267 | 267  | 209  | 209   | 177  | 177   | ps  | Assume similar to DRAM, used DRAM's         |

| Interconnect             |                         |     |      |      |       |      |       |     |                                           |
| Controller               |                         |     |      |      |       |      |       |     | Controller uses uncoupled package model, some increase can be expected pending Controller model used; probably in the 15ps to 30ps region |
| DQ Crosstalk and ISI*    |                         | 52  | 52   | 32   | 32    | 30   | 30    | ps  | 1 victim (1010...), 4 aggressors (PRBS); Different termination scheme for 800 other than that used for 1066 and 1333 should reduce xtlk to less than 25ps |
| DQS Crosstalk and ISI*   |                         | 23  | 23   | 23   | 23    | 10   | 10    | ps  | 1 shielded victim (1010...), 2 aggressors (PRBS) |
| Vref Reduction           |                         | 10  | 10   | 10   | 10    | 10   | 10    | ps  | +/- 30 mV included in DRAM skew; additional = ( +/- 10 mV) / (1 V/ns) |
| Ref Mismatch             |                         | 0   | 0    | 0    | 0     | 0    | 0     | ps  | +/-6% accounted for by DRAM spec |
| Path Matching (Board)    |                         | 10  | 10   | 10   | 10    | 10   | 10    | ps  | Within byte lane: 165 ps/m * 0.1 in; Impedance mismatch within DQS to DQ |
| Path Matching (Module)   |                         | 5   | 5    | 5    | 5     | 5    | 5     | ps  | Module routing skew (30% reduction with leveling) |
| Input Capacitance Matching |                         | 5   | 5    | 5    | 5     | 5    | 5     | ps  | Strobe & data shift differently |
| DDT Skew (1%)            |                         | 5   | 5    | 5    | 5     | 5    | 5     | ps  | Estimated |
| **Total Interconnect**   |                         | 110 | 110  | 90   | 90    | 75   | 75    | ps  | |

| Receiver                 | DRAM Skew               | 215 | 215  | 165  | 165   | 140  | 140   | ps  | tDS, tDH from DRAM spec, derated for faster skew rate and to Vref |

| Total Loss               |                         | 592 | 592  | 464  | 464   | 397  | 397   | ps  | Trans. + rec. + interconnect skew |

| Max Eye                  | Time Allowed            | 625 | 625  | 469  | 469   | 375  | 375   | ps  | |

| Budget 4L                | Timing Margin           | 33  | 33   | 5    | 5     | -22  | -22   | ps  | 4 layer board (micronstrip) 43-ohms, 0.135mm trace to trace spacing |

| 4 to 6 layer             | DQ Crosstalk and ISI    | 9   | 9    | 9    | 9     | 9    | 9     | ps  | decrease using stripline vs microstrip |
| DQS Crosstalk and ISI    |                         | 19  | 19   | 19   | 19    | 19   | 19    | ps  | decrease using stripline vs microstrip |

| Budget 6L                | Timing Margin           | 61  | 61   | 33   | 33    | 6    | 6     | ps  | 6 layer board (stripline), 40-ohms, 0.135mm trace to trace spacing |
PtP Termination
PtP Termination

- The best signaling is achieved when the driver impedance matches the trace impedance
  - Termination impedance matched as well

- For memory down applications, 50Ω to 60Ω may be adequate, but an ideal system would use a 40Ω impedance
  - DRAM has optional 40Ω or 48Ω driver (Ron$_{\text{base}}$ is 18Ω or 34Ω)
  - Larger ODT values are for generally used during Writes
  - Smaller ODT values are for generally used during standby
    - If single rank then ODT during standby is not needed
Source vs. Source and load termination

- **Source** - Driver’s impedance is termination
  - Lower power
  - Larger voltage margin
  - Overshoot / fast slew rates can be a problem in some case
  - Series R can improve results and save power over ODT

- **Source & load** - Driver’s impedance and ODT/VTT termination
  - Less sensitive to changes in the value of Ron
  - Less prone to overshooting the supply rails
  - Slower slew rates
Terminating PtP DQ Bus

- Generally use higher impedance DQ driver option
  - Usually slightly less than Zo
- DDR4 requires use of ODT termination due to POD
- DDR2 and DDR3(3L) do not mandate ODT usage, but should be used if possible in most cases
  - Series resistor likely should be added if ODT is not used
    - Line length < 2”, one series resistor in middle seems acceptable
    - Line length > 2”, one series resistor on each end might work
  - If ODT power is too much, disable ODT and use series resistor
    - Reduces I/O switching current by approx. 40%
    - Will slow down edge rate a little bit too
Terminating PtP DQ Bus

- **Source termination**
  - DDR2 has $R_{on}$ value of 18Ω; **Reduced $R_{on}$ value of approx 40Ω**
  - DDR3(3L) has $R_{on}$ value of 34Ω; **Reduced $R_{on}$ value of 40Ω**
  - DDR4 has $R_{on}$ value of 34Ω; **Reduced $R_{on}$ value of 48Ω**

- **ODT load termination**
  - DDR2 has ODT values of 50Ω, 75Ω and 150Ω
  - DDR3(3L) has ODT values of 20Ω, 30Ω, 40Ω, 60Ω, and 120Ω
  - DDR4 has ODT values of 34Ω, 40Ω, 48Ω, 60Ω, 80Ω, 120Ω, and 240Ω
  - Larger ODT provides voltage margin and uses less power
    - too large ODT then overshoot occurs and jitter increases
The CMD/ADDR bus is more sensitive than the DQ bus to input slew rate

- Faster slew rates introduce higher frequency harmonics onto the bus, degrading signal integrity
  - Faster is not always better when it comes to slew rate

Controller Ron, lead length, and board impedance determine termination requirements

- Series resistor probably ok at lower frequencies
- Series resistor with parallel termination to $V_{tt}$ should be used at higher frequencies
  - Larger $R = \text{more voltage margin but more jitter;} \text{ find best trade off via simulations}$
Command/Address Topologies

- Tree
  - Excellent performance - Until you run out of bandwidth
  - Hardest to route

- Hybrid tree
  - Good performance
  - Easier to route than tree

- Daisy chain
  - Good performance
  - Easiest to route
  - Best bandwidth – works at highest rates and largest loading
Pt4P CMD/ADDR Bus Termination

Tree

- Route + Skew Bandwidth + Performance

Hybrid tree

Route Skew Bandwidth Performance

Daisy-chain “fly-by”

+ Route - Skew + Bandwidth + Performance
Multiple Rank Termination
Multiple Rank Termination

- Design guides on web – WWW.Micron.com
- Systems are complex and require simulation
- DDR2 modules use Tree topology
- DDR3(3L) modules use Daisy Chain or “fly-by” topology
- DDR4 modules use Daisy Chain or “fly-by” topology
  - Daisy Chain reduces number of stubs and stub length
  - Address/Command/Control VTT termination at end of bus
  - More Address/Command/Control bandwidth
  - Has interconnect skew between clock and strobe at every DRAM on DIMM → must be de-skewed
Backup - Termination

DDR3 PtP Examples
PtP Layout and Termination Analysis

- The DQ bus is a single connection from the memory controller to a single DRAM
- DDR3 with Data rate = 1,333MT/s
- Zo for bus transmission lines is 50Ω
- What is the best way to terminate the DQ bus?
  - Consider three choices
    - Source termination
    - Source and load termination - on die termination (ODT)
    - Source and series termination
DDR3 PtP DQ Bus Termination

DRAM Read
TL0 = TL1 = ½”

Ron = 34Ω, ODT = 0Ω
Jitter=15ps  ApTACDC=0.87ns  MinSlew=4.2V/ns

Ron = 40Ω, ODT = 0Ω
Jitter=24ps  ApTACDC=0.66ns  MinSlew=4.0V/ns

Ron = 48Ω, ODT = 0Ω
Jitter=44ps  ApTACDC=0.64ns  MinSlew=3.7V/ns

Ron = 34Ω, ODT = 60Ω
Jitter=4ps   ApTACDC=0.65ns  MinSlew=2.7V/ns

Ron = 40Ω, ODT = 60Ω
Jitter=2ps   ApTACDC=0.64ns  MinSlew=2.5V/ns

Ron = 48Ω, ODT = 60Ω
Jitter=7ps   ApTACDC=0.62ns  MinSlew=2.3V/ns
DDR3 PtP DQ Bus Termination

DRAM Read
TL0 = TL1 = \( \frac{1}{2} \)"
DDR3 PtP DQ Bus Termination

DRAM Read
MB1 = MB2 = B2 = \( \frac{1}{2} \)"

Use DDR1, adjust settings and turn VTT off

Various Series R, with two driver impedances

Rs = 0Ω, Ron = 40Ω, ODT = off

Rs = 10Ω, Ron = 40Ω, ODT = off

Rs = 20Ω, Ron = 40Ω, ODT = off

Rs = 20Ω, Ron = 34Ω, ODT = off
DDR3 PtP DQ Bus Termination

- Source/series vs. Source/load termination
  - Source/series mitigates the overshoot and slew rate issues with source yet offers power savings
  - Source and load (ODT) still provides the largest data eye

Ron = 40Ω, ODT = off, Rs = 10Ω, Ron = 40Ω, ODT = 120Ω
Pt4P CMD/ADDR Bus Termination

- **Daisy chain** \((Ron=48\,\Omega, Rterm=40\,\Omega)\):
  - Jitter= 7ps, Eye= 1.36ns, Slew= 2V/ns
  - Easiest route
  - Timing skews between clock and data

- **Pt4P** \((Ron=34\,\Omega, Rs=0, Rterm=30\,\Omega)\):
  - Jitter= 8ps, Eye= 1.34ns, Slew= 1.7V/ns
  - Harder route
  - No overshoot or ringing

- **PRt4P** \((Ron=34\,\Omega, Rs=17\,\Omega, Rterm=0\,\Omega)\):
  - Jitter= 14ps, Eye= 1.26ns, Slew= 1.3V/ns
  - Lower power since no Vtt/Rterm

See backup for various termination comparisons
Backup – DDR4

Comparison to DDR2 and DDR3(3L)
# DDR2 to DDR3(3L) to DDR4 Comparison

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<tr>
<td><strong>Voltage (core, /IO)</strong></td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
</tr>
<tr>
<td><strong>Low Voltage Std.</strong></td>
<td>No</td>
<td>DDR3L at 1.35V</td>
<td>Probably 1.05V</td>
</tr>
<tr>
<td><strong>Vref Inputs</strong></td>
<td>1 – DQs/CMD/ADDR</td>
<td>2 – DQs and CMD/ADDR</td>
<td>1 – CMD/ADDR</td>
</tr>
<tr>
<td><strong>Densities Defined</strong></td>
<td>256Mb–4Gb</td>
<td>512Mb–8Gb</td>
<td>2Gb–16Gb</td>
</tr>
<tr>
<td><strong>Internal Banks</strong></td>
<td>4 → 8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>Bank Groups (BG)</strong></td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td><strong>Page Size – x4/x8/16</strong></td>
<td>1KB/1KB/2KB</td>
<td>1KB/1KB/2KB</td>
<td>512B/1KB/2KB</td>
</tr>
<tr>
<td><strong>tCK – DLL enabled</strong></td>
<td>125MHz to 400MHz</td>
<td>300MHz to 1066MHz</td>
<td>625MHz to 1.6GHz</td>
</tr>
<tr>
<td><strong>tCK – DLL disabled</strong></td>
<td>Optional, ≤125MHz</td>
<td>Optional, ≤125MHz</td>
<td>Feature, ≤125MHz</td>
</tr>
<tr>
<td><strong>Data Rate – Mb/s</strong></td>
<td>400/533/667/800 plus1066</td>
<td>800/1066/1333/1600 plus1866, 2133</td>
<td>1600/1866/2133/2400/2667/3200</td>
</tr>
<tr>
<td><strong>Prefetch</strong></td>
<td>4–bits (2 clocks)</td>
<td>8–bits (4 clocks)</td>
<td>8–bits (4 clocks)</td>
</tr>
<tr>
<td><strong>Burst length</strong></td>
<td>BL4, BL8</td>
<td>BC4, BL8</td>
<td>BC4, BL8</td>
</tr>
<tr>
<td><strong>Burst type</strong></td>
<td>(1) Fixed</td>
<td>(1) Fixed, (2) OTF</td>
<td>(1) Fixed, (2) OTF</td>
</tr>
</tbody>
</table>
# DDR2 to DDR3(3L) to DDR4 Comparison

<table>
<thead>
<tr>
<th>Features/Options</th>
<th>DDR2</th>
<th>DDR3(3L)</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Access (CL, tRCD, tRP)</strong></td>
<td>14ns +/-</td>
<td>14ns +/-</td>
<td>14ns +/-</td>
</tr>
<tr>
<td><strong>Additive Latency</strong></td>
<td>0, 1, 2, 3, 4</td>
<td>0, CL–1, CL–2</td>
<td>0, CL–1, CL–2</td>
</tr>
<tr>
<td><strong>READ Latency (RL)</strong></td>
<td>AL + CL</td>
<td>AL + CL</td>
<td>AL + CL</td>
</tr>
<tr>
<td><strong>WRITE Latency</strong></td>
<td>RL–1</td>
<td>AL + CWL</td>
<td>AL + CWL</td>
</tr>
<tr>
<td><strong>Data Strobes</strong></td>
<td>Single or Differential</td>
<td>Differential Only</td>
<td>Differential Only</td>
</tr>
<tr>
<td><strong>Driver / ODT Calibration</strong></td>
<td>none</td>
<td>240Ω Ext. Resistor</td>
<td>240Ω Ext. Resistor</td>
</tr>
<tr>
<td><strong>DQ Driver (STD)</strong></td>
<td>18Ω (13Ω to 24Ω)</td>
<td>34Ω (31Ω to 38Ω)</td>
<td>34Ω (31Ω to 38Ω)</td>
</tr>
<tr>
<td><strong>DQ Driver (ALT)</strong></td>
<td>40Ω (21Ω to 61Ω)</td>
<td>40Ω (36Ω to 44Ω)</td>
<td>40Ω (36Ω to 44Ω)</td>
</tr>
<tr>
<td><strong>DQ Bus Termination</strong></td>
<td>ODT</td>
<td>ODT</td>
<td>ODT</td>
</tr>
<tr>
<td><strong>DQ Bus</strong></td>
<td>SSTL18</td>
<td>SSTL15</td>
<td>POD12</td>
</tr>
<tr>
<td><strong>Rtt Values</strong></td>
<td>150, 75, 50Ω</td>
<td>120, 60, 40, 30, 20Ω</td>
<td>240, 120, 80, 60, 48, 40, 34Ω</td>
</tr>
<tr>
<td><strong>Rtt disabled at READs</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>ODT Modes</strong></td>
<td>Nominal, Dynamic</td>
<td>Nominal, Dynamic</td>
<td>Nominal, Dynamic, Park</td>
</tr>
</tbody>
</table>
### DDR2 to DDR3(3L) to DDR4 Comparison

<table>
<thead>
<tr>
<th>Features/Options</th>
<th>DDR2</th>
<th>DDR3(3L)</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>ODT Input Control</td>
<td>Required Driven</td>
<td>Required Driven</td>
<td>Not Required Driven</td>
</tr>
<tr>
<td>MultiPurpose Register</td>
<td>None</td>
<td>1 Defined, 3 RFU</td>
<td>3 Defined, 1 RFU</td>
</tr>
<tr>
<td>Write Leveling</td>
<td>None</td>
<td>DQS captures CK</td>
<td>DQS captures CK</td>
</tr>
<tr>
<td>RESET#</td>
<td>None</td>
<td>Dedicated input</td>
<td>Dedicated input</td>
</tr>
<tr>
<td>VPP Supply</td>
<td>none</td>
<td>none</td>
<td>2.5V</td>
</tr>
<tr>
<td>VREFDQ Calibration</td>
<td>none</td>
<td>none</td>
<td>Supported/Required</td>
</tr>
<tr>
<td>Bank Group</td>
<td>none</td>
<td>none</td>
<td>four</td>
</tr>
<tr>
<td>Low-power Auto SR</td>
<td>None</td>
<td>None (ASR opt.)</td>
<td>supported</td>
</tr>
<tr>
<td>Temperature Controlled Refresh (TCR)</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Fine Granularity Refresh</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>CMD/ADDR Latency</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Data Bus Write CRC</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Data Bus Inversion (DBI)</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
</tbody>
</table>
## DDR2 to DDR3(3L) to DDR4 Comparison

<table>
<thead>
<tr>
<th>Features/Options</th>
<th>DDR2</th>
<th>DDR3(3L)</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Per DRAM Addressability</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>C/A Parity</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Gear-Down Mode</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Connectivity Test Mode</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Max. Power Savings</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Program READ Preamble</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Program WRITE Preamble</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>READ Preamble Training</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Self Refresh Abort</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Command Input (ACT_n)</td>
<td>none</td>
<td>none</td>
<td>supported</td>
</tr>
<tr>
<td>Pin-out/Package (FBGA)</td>
<td>60-ball; x4, x8</td>
<td>78-ball; x4, x8</td>
<td>78-ball; x4, x8</td>
</tr>
<tr>
<td></td>
<td>84-ball; x16</td>
<td>96-ball; x16</td>
<td>96-ball; x16</td>
</tr>
<tr>
<td>UDIMM, RDIMM</td>
<td>240-pin</td>
<td>240-pin</td>
<td>288-pin</td>
</tr>
<tr>
<td>SODIMM</td>
<td>200-pin</td>
<td>204-pin</td>
<td>256-pin</td>
</tr>
</tbody>
</table>
Backup – DDR4 Features

Select New Features
DQ Output Driver

**DDR2, 3(3L) – Push-Pull**

**DDR4 – Pseudo Open Drain**
**DDR4 vs DDR3(3L)/2 Bank Architecture**

<table>
<thead>
<tr>
<th>DDRx</th>
<th>MT/s (min)</th>
<th>MT/s (max)</th>
<th>(t_{\text{CK}}) (max)</th>
<th>(t_{\text{CK}}) (min)</th>
<th>Prefetch</th>
<th>Internal Access (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>400</td>
<td>800</td>
<td>5ns</td>
<td>2.5ns</td>
<td>4n</td>
<td>5ns</td>
</tr>
<tr>
<td>3</td>
<td>800</td>
<td>1600</td>
<td>2.5ns</td>
<td>1.25ns</td>
<td>8n</td>
<td>5ns</td>
</tr>
<tr>
<td>4</td>
<td>1600</td>
<td>3200</td>
<td>1.25ns</td>
<td>0.625ns</td>
<td>16n</td>
<td>5ns</td>
</tr>
<tr>
<td>4</td>
<td>1600</td>
<td>3200</td>
<td>1.25ns</td>
<td>0.625ns</td>
<td>8n</td>
<td>2.5ns</td>
</tr>
</tbody>
</table>

\(t_{\text{CCD}_S} \text{ @ } 4CK = 2.5ns\)

\(t_{\text{CCD}_L} \text{ @ } 5CK = 5.3ns\)

---

**DDR3**

-CMD/ADD

**DDR4**

-CMD/ADD

**DDR4 adder if like DDR3**

@ 4CK = 2.5ns

@ 5CK = 5.3ns
MPR Operation

- Multi-Purpose Register is a useful tool that can be used for various ways
  - Training
    - DRAM controller receiver training
    - DRAM controller DQS to DQ phase training
    - Clock to address phase training
  - Debug
    - MPR provides a known response when rest is uncertain
  - RAS Support
    - Logging of C/A parity and CRC error information
  - Mode Register Confirmation
# MPR Registers

<table>
<thead>
<tr>
<th>Logical Page MR3[1:0]</th>
<th>Description</th>
<th>MPR Location [BA1:BA0]</th>
<th>MPR Bit Write Location [7:0]</th>
<th>Read Burst Order (serial mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UI0</td>
</tr>
<tr>
<td>00 = Page 0</td>
<td>Training Patterns</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>01 = MPR1</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>10 = MPR2</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>11 = MPR3</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>10 = Page 2</td>
<td>MRS Readout</td>
<td></td>
<td></td>
<td>PPR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VrefDQ Training Range</td>
</tr>
<tr>
<td>11 = Page 3</td>
<td>RFU</td>
<td></td>
<td></td>
<td>RFU</td>
</tr>
</tbody>
</table>

**Logical Page MR3[1:0]**

- 00 = Page 0
- 01 = MPR1
- 10 = MPR2
- 11 = MPR3

**Description**

- Training Patterns
- C/A Parity Error Log
- MRS Readout
- RFU
DDR4 Write CRC Error

The diagram illustrates the flow of data and CRC codes between the DRAM controller and DRAM. Data flows from the controller to the DRAM, where a CRC engine generates a CRC code. This CRC code is then compared with the CRC code generated by the controller to ensure data integrity.
C/A Parity

- C/A Parity provides parity checking of command and address buses
C/A Parity Flow

CMD/ADDR Process Start

- MR5[2:0] set Parity Latency (PL)
- MR5[4] set Parity Error Status to 0
- MR5[9] enable/disable Persistent Mode

CMD/ADDR Latched in

C/A Parity enabled

Persistent Mode enabled

MR5[4] = 0 @ ADDR/CMD Latched

C/A parity error

C/A parity enabled

MR5[4] = 0 @ ADDR/CMD Latched

C/A parity error

C/A parity error

Ignore Bad CMD

Command execution unknown

Alert_n Low 44 to 144 CKs

Log Error / Set Parity Status

Internal Precharge All

Alert_n High

Command execution unknown

Normal Operation Ready

Alert_n Low 44 to 144 CKs

Alert_n High

Log Error / Set Parity Status

Internal Precharge All

Alert_n High

Command execution unknown

Normal Operation Ready

MR5[4] reset to 0 if desired

Normal Operation Ready

MR5[4] reset to 0 if desired

Normal Operation Ready

Operation Ready
DDR3L vs DDR4 Power (with VPP)

- DDR3L vs DDR4 IDD specs
  - Both 30nm 4Gb x8
  - 1866
  - DDR4 power includes both IDD and IPP current

<table>
<thead>
<tr>
<th>Voltage</th>
<th>current</th>
<th>Power</th>
<th>PW DDR4 reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDD0</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>62</td>
</tr>
<tr>
<td>IDD1</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>70</td>
</tr>
<tr>
<td>IDD2N</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>35</td>
</tr>
<tr>
<td>IDD2P</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>37</td>
</tr>
<tr>
<td>IDD2Q</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>35</td>
</tr>
<tr>
<td>IDD3N</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>45</td>
</tr>
<tr>
<td>IDD3P</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>41</td>
</tr>
<tr>
<td>IDD4R</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>174</td>
</tr>
<tr>
<td>IDD4W</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>141</td>
</tr>
<tr>
<td>IDD5B</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>162</td>
</tr>
<tr>
<td>IDD7</td>
<td>DDR3 VDD</td>
<td>1.35</td>
<td>251</td>
</tr>
</tbody>
</table>
Backup - Clock Jitter

Highlight of JEDEC definitions
Clock Jitter: $t_{\text{CKavg}}$

- $t_{\text{CKavg}}$ is calculated as the average clock period across any consecutive 200 clock cycle window
  - Sometimes referred to as the “ideal” or “nominal” clock
  - Clock variations should fit within a random Gaussian Distribution
  - Does not include SSC effects
Clock Jitter: $t^{\text{JITper}}$

- $t^{\text{JITper}}$ is *Clock Period Jitter*; and is the deviation of any single clock period from $t^{\text{CKavg}}$
- $t^{\text{JITper}}_{\text{min/max}}$ is the largest deviation of any single clock period from $t^{\text{CKavg}}$

This is an absolute limit, not an RMS or Sigma value

- Micron Design Line article provides guidance on dealing with RMS clock jitter values, or jitter values that exceed the absolute clock period limit - TN-04-56
Clock Jitter: \( tE_{RR(nper)} \)

- \( tE_{RR(nper)} \) is defined as the cumulative error across consecutive \( n \) cycles relative to \( n \) \( tC_{Kavgs} \)
  - A period of \( tC_{Kavgs} \ast n \) (number of clocks) can not be deviated from by more than \( tE_{RR(nper)} \) (+ or -)
    - Negative is primary concern for a DRAM
- Clock periods greater than \( tC_{Kavgs} \) (slower) will offset clock periods less than \( tC_{Kavgs} \) (faster) when determining cumulative error
Clock Jitter: $t^{ERR}_{nper}$

- $t^{ERR}_{nper}$ is defined for different sets of cumulative jitter error parameters
  - $n$ is for 2, 3, 4, 5, 6-10, 11-50 clocks for DDR2
  - $n$ is for 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12; 13-50 clocks = $(1+0.68\ln[n]) \cdot t^{JITper}_{\text{min}}$ for DDR3/4
- Since jitter is a Gaussian distribution, the cumulative error, either positive or negative, is not a summation of the absolute values ($n$-clocks times $t^{JITper}_{\text{min}}$ or $t^{JITper}_{\text{max}}$).
Modulation frequency of 20 to 60KHz allowed, with up to 1% $t_{CKavg}$ deviation.

- If the DLL is locked prior to SSC being enabled, then $t_{CKavg}$ deviation can be up to 2% $t_{CKavg}$