Why do we need to study Signal Integrity, Power Integrity and EMI ALL-AT-ONCE?

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Kawka Piotr
An Example of Dramatic increase in HSD Systems

A look at Apple Macbook pro

- Increased Density
- High-speed everywhere
- Pressure to Reduce cost

<table>
<thead>
<tr>
<th>Interface</th>
<th>Bandwidth</th>
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<tbody>
<tr>
<td>USB 3.0</td>
<td>4.8 Gb/s</td>
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<tr>
<td>HDMI</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>DVI</td>
<td>8 Gb/s</td>
</tr>
<tr>
<td>DP</td>
<td>8.6 Gb/s</td>
</tr>
<tr>
<td>PCIe</td>
<td>5 Gb/s</td>
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<tr>
<td>SATA</td>
<td>3 Gb/s</td>
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<tr>
<td>DDR3</td>
<td>0.8-2.133 Gb/s</td>
</tr>
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</table>
Typical High Speed Digital Challenges

**Impedance Mismatch:**

- Line-width changes, Vias, Serpentines, Connectors, Cables
- Manufacturing tolerances for PCBs & Packages: effective dielectric constant, surface-roughness variations
- Tx output-impedance, Rx input-impedance vs. line impedance

**Crosstalk Noise**

- Electromagnetic coupling between signal lines
- Trace-to-Trace crosstalk, Via-to-Via coupling, Digital/RF coupling

**Power/Ground Noise**

- Tight requirements on PDN impedance as supply voltages decrease and currents increase to provide clean power to FPGA/ASICs
- Imperfect power/ground delivery system results in Simultaneous Switching Output (SSO) noise to propagate through the PDN

**EMI/EMC Performance**

- Most of the above effects produce EM radiation
High-Speed Digital PCB Analysis/Verification Methodology

Pre-layout Signal Integrity Analysis
Post-layout Signal Integrity Verification
Pre-layout Power Integrity Analysis
Post-layout Power Integrity Verification
EMI/EMC Analysis
Why do we need to study SI, PI and EMI all at once?

**SIGNAL INTEGRITY ANALYSIS**
Signal Degradation due to non-ideal channel

Low pass filter characteristic of transmission line (attenuates high frequency component in a signal which results in smearing out sharp edges)

Radiation, dispersion, resonance, and frequency dependent losses of transmission line degrades wave shape

Interference caused by cross talk (coupling between adjacent transmission lines) and radiations degrades wave shape

Impedance mismatch due to transmission line discontinuities

High frequency parasitics, delays, and asymmetric transmission paths

Through Hole Vias

Basic Microwave problem
Signal Integrity Analysis in ADS

Pre-layout SI analysis
- Choice of stack-up, components, net width and spacing, terminations
- After placement, detailed analysis of critical nets including crosstalk, via effects, connector effects etc.
- Derive layout routing constraints

Post-layout SI analysis
- Import board layout from Allegro (DFI link), Expedition, Boardstation etc. (ODB++)
- Complete EM analysis
- Verification of critical nets
Challenges in Pre-layout Design Space Exploration

- Multi-dimensional design space: Tx, channel, Rx
- Optimization goal is an extremely low BER
  ⇒ Megabit eye diagrams required for this figure of merit
  ⇒ Millions of simulation time steps
- BER at each point affect by:
  - Jitter: ISI, DCD, PJ & RJ
  - Channel impairments: attenuation, reflections, crosstalk
  - Tx and Rx equalizers
- Some components specified in frequency-domain
  ⇒ Beware of causality and passivity translation errors
- Traditional SPICE-like transient simulation requires
tens of hours per megabit
  ⇒ Optimization of Tx, channel, and Rx characteristics is impractical
Channel Simulator: Megabit Eye Diagram in One Minute per Point, not Ten Hours

Integrate layout artwork into schematic
Eye Diagram and BER Comparison of Channel Simulator in Statistical and Bit-by-bit Modes

ADS Channel Simulator
Statistical Mode

ADS Channel Simulator
Bit-by-Bit Mode

Timing Bathtub

Voltage Bathtub

ADS Channel Simulator
(1 M bits)

ADS Statistical Simulator

ADS Channel Simulator
(1 M bits)

ADS Statistical Simulator
Example:
Determine the Optimum Value of De-emphasis

Optimum de-emphasis value: 5.6 dB
Multilayer Transmission Lines Models in ADS

- Accurate models calculated by embedded 2D EM solver
- Fast simulation allows tuning/optimization
- Ideal for pre-layout analysis
Pre-Layout Case Study
Pre-layout Signal Integrity Analysis

Signal Analysis to determine modeling BW

Line analysis/optimization
- Width, intra-pair/inter-pair Spacing
- Impedance (TDR)
- Group delay (S-parameters)

Crosstalk analysis/optimization
- Line-to-Line crosstalk
- Via-to-Via crosstalk
- Connectors, cables

Margin verification using full-wave 3D EM models
Next Steps After Full Pre-layout Optimization

- Use optimized design rules, determined in pre-layout phase, as input to constraint editor in your enterprise constraint-based layout tool
  - Cadence Allegro
  - Mentor Expedition/Board station
  - Zuken CR-5000
- Post-layout predictive verification and fine tuning using ADS EM simulation on critical nets
Export Allegro Critical Nets to ADS “Sandbox”

1. Select critical nets
2. Select stackup layers
3. Cookie-cut power and ground planes
4. Create ports
5. Export to .ads file
6. ADS Layout “sandbox”
7. EM sim results OK?
   - Yes: Report fixes to physical designer who adjusts “golden” artwork in Allegro
   - No: Adjust layout

Agilent Technologies
Method Of Moments for PCB analysis

Claim:

MOM (Method of Moments) is the best full-wave technique for extracting S-parameters of Multi-layer PCBs and Packages

Why?

MOM does not need to discretize the Multi-layer Substrate if the substrate is homogeneous. MOM only discretizes areas with surface electric/magnetic currents

MOM is faster than other techniques (FEM, MOL, FDTD) that require substrate discretization
MOM results correlate to VNA measurements

S-parameter modeling of PCB & package interconnect

N1930B Physical Layer Test System (PLTS)

Courtesy of Gigatest
Need to model the following:
• Real cross-talk (not pre-layout)
• Signal layer transitions: L1-to-L3 is it same as L1-to-L5?
• Via stubs
• Serpentine routing for length-matching rules
• Stitching via impact (number & location)
8-Layer Package design: DDR3 memory channel

SODIMM for memory controller
Impact of GND PTH stitching
Impact of PTH GND stitching
Impact of GND stitching @ die-side

Reduced GND stitch @ die-side
Impact of stitching on IL

Transmission from memory controller to GPU chip

![Graph showing transmission with different numbers of vias (0, 8, and 15) at various frequencies.](image)
What about the x-talk impact?

Transmission from signal line to adjacent line
What about the jitter impact?

Eye diagrams from 9 lines going from memory controller to GPU interface

Initial grounding

Final grounding
Advantages of ADS for HSD

Not a collection of points tools. ADS is an integrated solution with:

- **Accurate models** refined over many years against measured data
  - Causal S-parameter and multilayer transmission line models
  - Jitter decomposition verified with Agilent EZ JIT Plus algorithm
- **ADS Channel Simulator** million bit per minute and statistical modes
  - Pre-layout design space exploration
- **Industry-leading ADS Transient Convolution** for pre-layout final verification e.g. overnight run on **non-linear components**
- **Design flow integration** with artwork from enterprise board tools
  - ADS Layout “sandbox” doesn’t force you to learn 3-D MCAD manipulation
- **Method of moments** is the fastest and most accurate EM technique for trace-and-via geometries
  - ADS Momentum G2 is the leading method of moments tool
  - Predictive post-layout verification and fine tuning of artwork
- **FEM** for non trace-and-via geometries
  - Balls, bond wires, dielectric bricks, connectors, etc.
Why do we need to study SI, PI and EMI all at once?

POWER INTEGRITY ANALYSIS
Simplified PDN Model
Important PI challenges that can affect design performance

- Analyze Power plane impedance vs. freq
- Find Power/Ground resonances
- Estimate Switching Noise spectrum
- Effective use of decoupling capacitors (On-die, On-PKG & On-PCB)

**Strategies that can improve power integrity:**

- Low-impedance path from power supply to die
- Optimize/validate discrete decoupling capacitor network
- Analyze Via Transitions
- Avoid return path discontinuities → define number and position of Stitching vias

![Diagram of FPGA circuit](image-url)
Conceptual Origin of Simultaneous Switching Output (SSO) Noise

What influences SSO Noise:
- Mutual inductance between the loops
- Number of SSOs
- $dI/dt$
Simple PDN model

Impedance seen by device

\[ Z_{\text{TARGET}} = \frac{\text{Voltage Rail} \times \left( \frac{\% \text{Ripple}}{100} \right)}{\text{Max Transient Current}} \]

\[
\frac{2.5V \times 0.05}{0.5A} = 0.25 \text{ Ohm}
\]
SSO Noise model

[Diagram of electrical components and models]
SSO Noise Simulation

- Voltage Regulator
- PDN Model 1
- PDN Model 2
- "Quiet" Buffer
- Differential Pair

Graphs showing time, nsec vs. voltage and current.
Case Studies

1. Simple Power/Ground planes
2. BGA package (DQ lines + Power/ Ground planes)
3. Full DDR module (Power/ Ground planes)

Area/Layers:
- Simple
- Medium large
- Large

Frequency:
- MOCHA project[1]
Case 1: Power Plane Impedance

Example: PDN impedance
Freq sweep 0-3 GHz
RF mode

Extracted power plane impedance

Momentum 2011

<table>
<thead>
<tr>
<th>Matrix Size:</th>
<th>15,042</th>
</tr>
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<tbody>
<tr>
<td>Process Size:</td>
<td>1345 MB</td>
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<tr>
<td>Elapsed Time:</td>
<td>31m56s</td>
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</table>

Intel Core2 Quad (4 cores)
RAM: 4 GByte
PDN Analysis
Case2: BGA Package (MOCHA project)

Example: BGA package VSS, VDD, DQ lines
Freq sweep 0-10 GHz, 200MHz step
RF mode
Using sheet conductor

MOCHA project [1]: Modeling and CHAracterization for SiP - Signal and Power Integrity Analysis

Momentum 2011
with bonding wire

Matrix Size: 49952
Process Size: 4632 MB
Elapsed Time: 2h51m6s

Intel Xeon X5482 x 2 (8 cores)
RAM: 32 GByte
Case 3: DDR Module

Momentum 2011

Matrix Size: 38,789
Process Size: 14406 MB
Elapsed Time: 6h38m54s

Example: DDR module Power/Ground
Freq sweep 0-3 GHz, 200 MHz step
RF mode
Using sheet conductor

Intel Xeon X5530 x 2 (8 cores)
RAM: 64 GByte
New in ADS2011

- Guided EM simulation setup
- Enables net based selection and simulation
- Allows Port grouping/clustering
- Computes PDN impedance
- Provide current distribution with SMD components
EMI/EMC ANALYSIS

Why do we need to study SI, PI and EMI all at once?
What are the different types of Radiated-Emission?

1. PCB of infotainment Emission:
   A. Traces on the PCB
   B. Substrate Edges by the PD noise
   C. Connector+Cables common-mode noise
2. PCB + Housing (Compartment) impact
3. PCB+Housing in Vehicle with other cables
Complexity of EMI problem

Badly routed traces generate EMI
High-speed connectors and cables **amplify** the EMI problems

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**Minimize IC, pkg, and PCB EMI to reduce overall system EMI**

*H-Field Measurement From EMscan of GPU Board*
Limiting EMI

Trace emission

- Emission on a Digital Video Interface (DVI) example
- Memory bus emission

PCB Edge emission to due Power Delivery Network

Cable emission
DVI/HDMI are standard interfaces for video transmission

To minimize EMI, DVI/HDMI standards are using TMDS (Transition Minimized Differential Signaling) technologies

TDMS operates at 10 times the pixel frequency (current DVI maximum for pixel frequency is 165 MHz)
Problem Statement (cont’d)

- In the context of a PC, DVI co-exists with other interfaces

- On this example, the ethernet card/cables exhibit a TMDS signature emission at 770MHz
Current solution

Put on band-aid to stop the radiation....

It is hardly optimal, does not always work, and costs lot of money

Which one?

Copper band-aid (well suited for E-coupling)

R4N Suppressor band-aid (well suited for H-coupling)
What if we could simulate it!

Using **Momentum** for 1 hour:

Analysis @ **770 MHz**
Confirm max radiation at the bottom of PCB due to TMDS routing

Max angle: 144/160

26 uW in total power

Antenna Gain is -48 dB

5uW / steradian
With metal shielding...

Using **Momentum** for 1 hour:

- **Analysis @ 770 MHz**
  - Confirm max radiation at the bottom of PCB due to TMDS routing
  - Max angle: 144/160
  - 27 uW in total power
  - Antenna Gain is -47 dB
  - 6uW / steradian

Metal shield and PCB ground with heat-sink screws

Worse!
With NEC/Tokin R4N shielding…

Using **Momentum** for 1 hour:

Analysis @ **770 MHz**
Confirm max radiation at the bottom of PCB due to TMDS routing

Max angle: 162/146
13 uW in total power
Antenna Gain is -51 dB
2uW / steradian

R4N material placed at the bottom of the PCB
Looking at it closer

Original

With R4N

Connectors

GPU
And in the chamber?

The measurement showed an improvement from 7.6 dB to 8.2 dB (0.6 dB).

Simulation predicted 3 dB and so the correct trend.
Limiting EMI

Trace emission

- Emission on a Digital Video Interface (DVI) example
- Memory bus emission

PCB Edge emission to due Power Delivery Network

Cable emission
4-layer PCB with Memory Emission problem

**Problem:**
Investigate Emission problem at 1.25 of the memory clock frequency (1.623 GHz)

**Notes:**
Address/Command Nets are routed on bottom-layer referencing Vddq power plane (due to lack of real-estate)
EMI Simulation Methodology

Step-1: Simulate and Visualize Current-density plot of the bottom of the card*

Method-of-Moments (Momentum) Simulations showing current-density plots and hot-spot regions on the PCB

*Using Agilent Momentum Field Solver
Step-2: Isolate Problem
Observe hot-spot area closely, and identify root-cause

Root-cause:
There is small $\lambda/8$ power-plane patch that is radiating like patch-antenna

Use Momentum UW with Antenna-Gain parameter to measure the merit of the PCB as non-intended antenna

Develop EMI guidelines along with SI/PI Guidelines using Antenna-Gain Parameter to compare Layout guidelines
Limiting EMI

Trace emission
- Emission on a Digital Video Interface (DVI) example
- Memory bus emission

PCB Edge emission to due Power Delivery Network

Cable emission
EMI Simulation challenges

- System level (source / coupling path)
- Full wave EM simulation is often needed
- Time and memory consuming
SSO Noise on the PCB

SSO current is obtained by a combined simulation of the power delivery network model and the memory IO channel model.
How does the SSO noise look like?

SSO noise is broadband.
Icc profiles are time-dependent.

FDTD is very well suited to handle SSO noise phenomena.
Importing PCB layout of the Memory-Channel

Stackup

- Signal
- Ground
- Signal
- VDD
- Ground
- VDD

board thickness: 1.57mm
PCB top layer: Including noise sources

VSS notches

Noise sources

IC
PCB bottom layer: Decoupling caps
Far field radiation of the SSO noise

With Decaps          Without Decaps          With Decaps          Without Decaps

0.5 GHz               1 GHz

Reduction of 3-4 dB
Current density at 500 MHz

Without Decaps

With Decaps
FDTD has an inherent parallel nature, which makes it extremely well suited for GPU acceleration.

<table>
<thead>
<tr>
<th>Acceleration</th>
<th>Runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>Over 1 week</td>
</tr>
<tr>
<td>GPU acceleration (1 card)</td>
<td>~ 12 hours</td>
</tr>
<tr>
<td>GPU acceleration (4 cards)</td>
<td>~ 1-2 hours</td>
</tr>
</tbody>
</table>

*Used 1.5 GB of RAM*
Limiting EMI

Trace emission
- Emission on a Digital Video Interface (DVI) example
- Memory bus emission

PCB Edge emission due to Power Delivery Network

Cable emission
- Emission due to connectors
- ESD protection
Board + Connector + Mate
Combining the board and the imported connectors

Precise landing of connector fingers on board signal pad
Near-field radiation

- Simulated with EMPro FDTD solver
- Simulation time ≈ 2 hrs with 3-GPU cards

Study if improved grounding & shielding of the connector improves EMI behavior
Improving grounding

No copper tape

Extra copper tape
Improving grounding: Far-field impact of CU-tape

Reduction of 5 dB for EMI emission in direction of chassis
Limiting EMI

Trace emission
- Emission on a Digital Video Interface (DVI) example
- Memory bus emission

PCB Edge emission due to Power Delivery Network

Cable emission
- Emission due to connectors
- ESD protection
ESD protection

Electrostatic discharges are meant to be temporary so only a transient-based engine can show their impact.

Protective system

I at 30 ns
I at 60 ns

I \sim 30 \text{ A} / 8 \text{ kV}

\text{tr} = 0.7 \text{ up to } 1 \text{ ns}
Location of ESD diodes

Excitation with esd current source
Excitation at connector side

- **Name**: ESD excitation
- **Type**: Feed
- **Resistance**: 50 ohm
- **Inductance**: 0 nH
- **Capacitance**: 0 pF
- **RLC Arrangement**: All Parallel
- **Feed Type**: Voltage
- **Amplitude**: 1 V
- **Phase Shift**: 0°
- **Time Delay**: 0 µs
- **Waveform**: ESD pulse

Excitation with ESD current source
Termination at board Side

Termination = 50 Ohm // 2pF
Voltages with no ESD Diode

Traditionally, a rule of thumb is to place the ESD diodes close the connector for a better efficiency.

Could we verify it on this case?
ESD output

ESD diodes close to the connector

≈ 30 V

ESD diodes close to the GPU

≈ 50 V
## Simulation Time

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<tr>
<td>CPU</td>
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</tr>
<tr>
<td>GPU acceleration (1 card)</td>
<td>~ 16 hours</td>
</tr>
<tr>
<td>GPU acceleration (3 cards)</td>
<td>~ 5 hours</td>
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</table>
Conclusion

No Single Methodology/Technique can do it all.

**Momentum** is best Full-wave EM modeling for PCBs and Packages

**FDTD** is best for wide-band phenomena like SSO noise Emission, Conducted Emission and ESD especially if it is accelerated by GPU.

**FEM** and FDTD for S-parameter modeling of PCB+Connector (Conducted-Emission → FDTD, S-parameter model → FEM)

Having the 3 most-renowned EM technologies, Agilent is here to help you finding the adequate engine to solve your HSD problem.