Chronicles of a High Speed PCB
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– Preface

– Book 1: Starting where the layout engineer left-off

– Book 2: Analyzing the board
  • What matters most
  • Does PDN matter? Take 1
  • Quick Tips

– Book 3: Extracted the board, now what?

– Book 4: System level simulation
  • Where it all comes together
  • Does PDN matter? Take 2

– Book 5: Ready for fabrication with confidence

– Epilogue
Chronicles of a High Speed PCB

Preface

– High Speed PCBs, then and now

– Role of a Signal Integrity System Designer

– Is the work done when the layout is completed?

– Task at hand
Book 1: Starting where the layout engineer left-off

Why perform pre-fab post layout simulations:
Segue: Understanding the board used in this presentation

Xilinx KCU105 Ultrascale FPGA Evaluation Kit

9.27 inch

5 inch

16 layers PCB

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Book 1: Starting where the layout engineer left-off
Preparing for board extraction:
Book 2: Analyzing the board: What matters Most

Is your ground ‘really’ at ground?

Voltage Drop

Current Density
Voltage and current reported per Via, Sink, VRM and more!

Power Dissipation and Current Density visualization

Xilinx KCU105 – VCC1V2 PDN
Why perform a DC analysis?
What is your PDN Impedance doing to you?

*Z-scale increased for visualization

E field at 300MHz; all layers

E field at 300MHz: GND layer immediately below power plane
Why do we need PDN Impedance analysis?

- **Power Plane**
- **Ground Plane**
- **VRM**
- **Sinks**

**Z(f)**

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Target impedance

- The highest impedance that will create a voltage drop still below the acceptable ripple spec

- Establishing the target impedance is hard

\[ Z_{\text{target}} < 2 \frac{V_{dd} \times \text{ripple}\%}{I_{\text{peak}}} = 2 \frac{V_{dd} \times \text{ripple}\% \times V_{dd}}{P_{\text{max}}} \]

- Limiting factors for Target Impedance:
  - Series Inductance of PDN
  - Package
  - On-die Capacitance

\[ Z_{\text{target}} < 2\pi L_{\text{pkgfmax}} \]
Decoupling Capacitors

No Capacitors

With Capacitors
ESR: equivalent series resistance
ESL: equivalent series inductance
SRF: self resonant frequency
Optimize decoupling capacitors based on parameters that matter in your design

- Cost
- Number of decaps
- Number of Vendors

Target Impedance
Book 2: Analyzing the board: What matters Most

Should you simulate ‘everything’?

– Plan which structures you want to simulate

DDR4 structure with PDN
Book 2: Analyzing the board: What matters Most

– Do you want to simulate “All” or a portion of the structure?

DDR4 structure with PDN – one bank

*Z-scale increased for visualization
Book 2: Analyzing the board: What matters Most

Should you include PDN

– The answer is: It depends!

DDR4 structure with PDN – one bank

DDR4 structure – one bank

*Z-scale increased for visualization

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Book 2: Analyzing the board: re-using the setup

Maximize efficiency

Scripts

- Easy and fast way to share setup with colleagues, or reuse setup on different revisions of the same board

- You can also create a script for a smaller section of your setup
  - Script containing Decoupling caps
Book 3: Extracted the board, now what?
Need for system level simulation
Book 3: Extracted the board, now what?

Need for system level simulation

- Much data has been collected, but what do they tell you?

- Can you interpret S-parameters into meaningful results?

- Does your system pass spec?
Book 3: Extracted the board, now what?

Need for system level simulation

– Need to run system level simulation
  • Eye height
  • Eye Width
  • BER Analysis
  • Time Domain Analysis
  • Statistical Analysis
  • Channel Simulation
Book 2: Analyzing the board: Quick Tip

What you don’t know can hurt you!

- Ability to generate test benches with a click of a button
  - Use for Post layout system simulations, such as ChannelSim
Book 4: System level simulation
Post layout simulation setup - DDR

Extracted PDN Model
Book 4: System level simulation
Does PDN Matter, Take 2

With Ideal supply
Book 4: System level simulation

Post layout simulation setup - PCIe

![Diagram of PCIe interface with parameters and terminations]
Book 4: System level simulation

Comprehensive System Analysis

PCle 3, P0 to P10
No Crosstalk
Book 5: Ready for fabrication with confidence
Post layout Simulation – Crosstalk Analysis

PCI-E Interface

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Book 5: Ready for fabrication with confidence

Confidence

Wild River Technology CMP-28 SI Kit

Stripline Beatty Standard Test Structure

Full-wave 3DEM (FEM)

SIPro
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Confidence

S21 SIPro vs. Measured

S11 SIPro vs. Measured

S22 SIPro vs. Measured

Red: SIPro  Blue: Measured

Measurement: Courtesy of GigaTest Labs

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Epilogue

Wrap up – what is next

– What we did

– Where to go from here

Layout Import into ADS
(Direct *.brd Import, Allegro ADFI or ODB++ flow)

SIPro / PIPro
PCB Characterization and Model Extraction

Signal/Power Integrity Analysis
(Transient Convolution, Channel Sim, DDR Bus Sim)
Any Questions?