Chronicles of a High Speed PCB
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– Book 4: System level simulation
  • Where it all comes together
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– Book 5: Ready for fabrication with confidence
– Epilogue
Chronicles of a High Speed PCB

Preface

– High Speed PCBs, then and now
– Role of a Signal Integrity System Designer
– Is the work done when the layout is completed?
– Task at hand
Book 1: Starting where the layout engineer left-off
Why perform pre-fab post layout simulations:

- Confidence
- Budget
- Failures
Segue: Understanding the board used in this presentation

Xilinx KCU105 Ultrascale FPGA Evaluation Kit

9.27 inch

5 inch

16 layers PCB
Book 1: Starting where the layout engineer left-off
Preparing for board extraction:
Book 2: Analyzing the board: What matters Most

Is your ground ‘really’ at ground?

Voltage Drop

Current Density
Book 2: Analyzing the board: What matters Most

DC IR Drop

Voltage and current reported per Via, Sink, VRM and more!
Why perform a DC analysis?
Book 2: Analyzing the board: What matters Most

What is your PDN Impedance doing to you?

E field at 300MHz: GND layer immediately below power plane

E field at 300MHz: all layers

*Z-scale increased for visualization

Demo!!!
Coppers’ temperature coefficient is 0.0393 at 20°C. The resistance increases 0.393% per 1°C

\[
R(\Delta T) = R_0 (1 + \alpha \Delta T)
\]

<table>
<thead>
<tr>
<th>Material</th>
<th>( \rho ) (Ω·m) at 20°C</th>
<th>( \sigma ) (S/m) at 20°C</th>
<th>Temperature coefficient ( (K^{-1}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon (graphene)</td>
<td>1.00 \times 10^{-8}</td>
<td>1.00 \times 10^8</td>
<td>-0.0002</td>
</tr>
<tr>
<td>Silver</td>
<td>1.59 \times 10^{-8}</td>
<td>6.30 \times 10^7</td>
<td>0.0038</td>
</tr>
<tr>
<td>Copper</td>
<td>1.58 \times 10^{-8}</td>
<td>6.96 \times 10^7</td>
<td>0.003862</td>
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<tr>
<td>Annealed copper[note 2]</td>
<td>1.72 \times 10^{-8}</td>
<td>5.80 \times 10^7</td>
<td>0.00393</td>
</tr>
<tr>
<td>Gold[note 3]</td>
<td>2.44 \times 10^{-8}</td>
<td>4.10 \times 10^7</td>
<td>0.0034</td>
</tr>
<tr>
<td>Aluminium[note 4]</td>
<td>2.82 \times 10^{-8}</td>
<td>3.60 \times 10^7</td>
<td>0.0039</td>
</tr>
</tbody>
</table>
Example: Insertion Loss vs. Temperature

3 inch transmission line on FR-4

- Temperature increases the chancel loss, including PDN at DC, due to the increased resistivity

![Graph showing insertion loss vs. frequency with temperature effects]
The Importance of Thermal Effects in PI Simulations

Electric Analysis Only IR-drop

Electro-Thermal IR-drop Analysis

PASS

FAIL
PIPro DC Electro-Thermal Capability

Start

Selected nets (PWR/GND)
Selected devices (VRM/Sink/Resistor)

Electric Only

Electro-Thermal

Electric Analysis

Power

Component thermal model
Convective conditions
Substrate anisotropy

Voltage IR drop
Current flow
Power Dissipation

Temperature

Temperature rise
Heat flow

Thermal Analysis

End

Ambient
Full Board (Metal/Stack)
All devices (Source/Cooling)
PCB Thermal Floor Planning

PCB Temperature Distribution w/ Heat Sources

- Temperature distribution plot provides an insight for the board temperature that affects the insertion loss and the DC IR-drop

- Thermal floor planning
  - Additional insights for channel loss
  - Useful PCB layout guidelines
Mitigating Potential Thermal Issues
By Cooling the Board with Air Flow

– Forced air flow such as fans will cool off the board temperature

– Available air flow entry options in PIPro DC Electro-Thermal
  • By natural convection
  • By air flow speed
  • By heat transfer coefficient

CFM*: Cubic feet per minute, with a duct size 5x5 inch
Mitigating Potential Thermal Issues
By Heat Sink / Thermal Pad

– Heat Sink
  • Rectangular shape
  • Circular shape

– Thermal Pad
  • Conductive adhesive
  • TIM (Thermal Interface Material)

Heat Source (5W)
Heat Source (2W)
Heat Source (1.5W)

0.5 °C/W Thermal Pads on 3 chips
20 °C/W Heat Sink on 1 chip
20 °C/W Heat Sink on 3 chips
20 °C/W Heat Sink on 3 chips

No Heat Sink
PIPro DC Electro-Thermal

- Case setup
  - One PDN (FPGA 1.2V power net), one VRM
  - 5 sinks: 2A sink for FPGA, 0.3A sinks for DDR4
- Various case studies

<table>
<thead>
<tr>
<th>Case #</th>
<th>Analysis condition</th>
<th>Voltage at FPGA</th>
<th>DC IR Drop</th>
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<tbody>
<tr>
<td>0</td>
<td>No Thermal</td>
<td>1.188V</td>
<td>13.5mV</td>
</tr>
<tr>
<td>1</td>
<td>+ Joule Heating</td>
<td>1.188V</td>
<td>13.5mV</td>
</tr>
<tr>
<td>2</td>
<td>+ Electric Dissipation</td>
<td>1.185V</td>
<td>16.8mV</td>
</tr>
<tr>
<td>3</td>
<td>+ Heat Source</td>
<td>1.182V</td>
<td>18mV</td>
</tr>
<tr>
<td>4</td>
<td>+ Heat Sink</td>
<td>1.185V</td>
<td>17.2mV</td>
</tr>
<tr>
<td>5</td>
<td>+ Fan</td>
<td>1.185V</td>
<td>16.9mV</td>
</tr>
</tbody>
</table>
Simulating Multiple VRMs and Sinks in PIPro

- Additional heat sources can be added to the analysis (thermal stimulus is not just the heat from VRMs, sinks and joule losses in the traces)

- Thermal boundary conditions: heatsinks, airflow, thermal pads, board boundaries
Why do we need PDN Impedance analysis?
Target impedance

– The highest impedance that will create a voltage drop still below the acceptable ripple spec

– Establishing the target impedance is hard

\[
Z_{\text{target}} < 2 \frac{V_{dd} \times \text{ripple}\%}{I_{\text{peak}}} = 2 \frac{V_{dd} \times \text{ripple}\% \times V_{dd}}{P_{\text{max}}}
\]

– Limiting factors for Target Impedance:
  
  • Series Inductance of PDN
  
  • Package  \[ Z_{\text{target}} < 2\pi L_{\text{pkgfmax}} \]
  
  • On-die Capacitance
Book 2: Analyzing the board: What matters Most

Decoupling Capacitors

No Capacitors

With Capacitors
Book 2: Analyzing the board: PDN Z-Impedance Analysis

Decoupling capacitors

ESR: equivalent series resistance
ESL: equivalent series inductance
SRF: self resonant frequency
Optimize decoupling capacitors based on parameters that matter in your design

- Cost
- Number of decaps
- Number of Vendors

Target Impedance
Decap Optimization in PIPro-AC

Fundamental setup items:

• AC analysis
• Decaps defined in Component Models

Launched from AC analysis:
“Decap Optimization”
Decap Optimization in PIPro-AC
Including optimization-specific information

- Decaps that should be excluded from the optimization procedure
- Target Impedance required as spec

- Can be imported in csv format
- Can be specified explicitly in table
DeCap Optimization in PIPro-AC

Design choice: Flexibility to identify effect of constraints

- Full calculation only launched for new setup and/or new target
- Instantaneous refresh of solutions when updating constraints
- Allows to easily update the suggested solutions

Optimization does not require a re-simulation of the PIPro AC EM sim!

Optimization divided in two distinct steps:
1. Main optimization step
   - Minimum set of solutions needed to be evaluated
2. Refinement step
   - Continues to evaluate the full set of solutions
   - Shows current best result to ensure existence of solution when stopped
DeCap Optimization
List Sorting

- 10 best results are presented
- Detailed overview of each results exits
  - Impedance graph wrt original solution
  - Detailed decap configuration with assigned model
  - Loop inductance table
- New AC analysis can be created for each result
Should you simulate ‘everything’?

- Plan which structures you want to simulate
– Do you want to simulate “All” or a portion of the structure?

DDR4 structure with PDN – one bank

*Z-scale increased for visualization
Book 2: Analyzing the board: What matters Most
Should you include PDN

– The answer is: It depends!

DDR4 structure with PDN – one bank

DDR4 structure – one bank
Book 2: Analyzing the board: re-using the setup

Maximize efficiency

Scripts: Easy and fast way to share setup with colleagues, or reuse setup on different revisions of the same board

- You can also create a script for a smaller section of your setup
  - Script containing Decoupling caps
Book 3: Extracted the board, now what?

Need for system level simulation
Book 3: Extracted the board, now what?
Need for system level simulation

– Much data has been collected, but what do they tell you?

– Can you interpret S-parameters into meaningful results?

– Does your system pass spec?
Book 3: Extracted the board, now what?

Need for system level simulation

- Need to run system level simulation
  - Eye height
  - Eye Width
  - BER Analysis
  - Time Domain Analysis
  - Statistical Analysis
  - Channel Simulation
Book 2: Analyzing the board: Quick Tip

What you don’t know can hurt you!

- Ability to generate test benches with a click of a button
  - Use for Post layout system simulations, such as ChannelSim
Book 4: System level simulation

Post layout simulation setup - DDR

Extracted PDN Model
Book 4: System level simulation
Does PDN Matter, Take 2

With Ideal supply

Ideal DC source used, 1.2V
Book 4: System level simulation

Post layout simulation setup - PCIe

PCI-E Interface

<table>
<thead>
<tr>
<th>Tx</th>
<th>Rx</th>
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<tbody>
<tr>
<td>Tx_{diff}</td>
<td>Rx_{diff}</td>
</tr>
<tr>
<td>BitRate = DataRate Gbps</td>
<td></td>
</tr>
<tr>
<td>V_{high} = 1 V</td>
<td>V_{low} = 0.0 V</td>
</tr>
<tr>
<td>RiseFallTime = 30 psec</td>
<td></td>
</tr>
<tr>
<td>Mode = Maximal Length LFSR</td>
<td></td>
</tr>
<tr>
<td>ExcludeLoad = no</td>
<td></td>
</tr>
<tr>
<td>EQMode = Specify FIR taps</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Clock</th>
<th>RX Lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>Termination</td>
<td></td>
</tr>
<tr>
<td>Termination</td>
<td></td>
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<tr>
<td>Termination</td>
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<tr>
<td>Termination</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>TX Lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>Termination</td>
</tr>
<tr>
<td>R = 50 Ohm</td>
</tr>
</tbody>
</table>

**Batch Simulation**

- BatchSimController
- Var = Start = 1.0, Stop = 10.0, Step = 1.0, Lin =
- UseSweepPlan = no
- Analysis[1] = "ChannelSim1"
- UseSweepModule = yes
- SweepModule = "CSV_List"
- SweepArgument = "TapValues_batch.csv"
- UseSeparateProcess = yes
- MergeDatasets = yes
- RemoveDatasets = yes

**Channel Simulation**

- ChannelSim
- ChannelSim 1
- NumberOFBits = 10000
- ToleranceMode = Auto
- EnforcePassivity = yes
- Mode = 8 bit, bit
Book 4: System level simulation

Comprehensive System Analysis

PCle 3, P0 to P10
No Crosstalk
Book 5: Ready for fabrication with confidence

Post layout Simulation – Crosstalk Analysis
Comprehensive System Analysis: Crosstalk

PCle 3, P0 to P10
With Crosstalk

Demo!!!
Book 5: Ready for fabrication with confidence

Confidence

Wild River Technology CMP-28 SI Kit
Book 5: Ready for fabrication with confidence

Confidence

**S21 SIPro vs. Measured**

**S11 SIPro vs. Measured**

**S22 SIPro vs. Measured**

Red: SIPro  Blue: Measured

Measurement: Courtesy of GigaTest Labs
Epilogue

Wrap up – what is next

– What we did

– Where to go from here

Layout Import into ADS
(Direct *.brd Import, Allegro ADFI or ODB++ flow)

SIPro / PIPro
PCB Characterization and Model Extraction

Signal/Power Integrity Analysis
(Transient Convolution, Channel Sim, DDR Bus Sim)
Any Questions?