Designing with 4G Modulated Signals for Optimized Multi-standard Transceiver ICs

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Agenda

• Introduction

• RF Design Challenges for 4G Systems

• Enabling RF-System Simulation within the RFIC environment

• Going beyond RF System Verification

• Summary
Time-to-Market – Today’s Tablets as an example

Data
Wi-Fi® 802.11a/b/g/n  
**Now:** 802.11ac

Location
A-GPS  
possible: Galileo, Beidou, GLONASS

Personal Connectivity
Bluetooth v4.0  
**Now:** 802.11ad

Communications
4G LTE  
**Now:** LTE-Advanced

o Multiple different complex systems placed in close proximity
o Tight design specs through increased bandwidth
Some RF Design Challenges for 4G

- Increased bandwidth to 100 MHz (LTE-A) and 160 MHz (802.11ac)
  - Drives Peak-to-Average Power Ratio (PAPR) to extreme levels and requires Efficiency trade-offs
  - Exposes frequency-dependence as well as Memory Effects and Nonlinearities

- No transmit filter definition in LTE, as for 3G technologies
  - In-channel performance (i.e. EVM) and out-of-channel performance (i.e. ACLR, SEM (Spectrum Emission Mask)) requirements need to be met by the design

- Dramatically increased Verification task
  - Fragmented spectral bands (e.g. – 43 defined bands for LTE)
  - Co-existence with older/multiple standards (MSR testing)

- Advanced compensation techniques require RF/BB interaction
  - Digital Pre-Distortion (DPD) or Envelope Tracking
### Example: Enhancements from 802.11n to 802.11ac

<table>
<thead>
<tr>
<th>Feature</th>
<th>Mandatory</th>
<th>Optional</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel bandwidth</td>
<td>20 MHz, 40 MHz, 80 MHz</td>
<td>160 MHz, 80+80 MHz</td>
</tr>
<tr>
<td>FFT size</td>
<td>64, 128, 256</td>
<td>512</td>
</tr>
<tr>
<td>Data subcarriers / pilots</td>
<td>52 / 4, 108 / 6, 234 / 8</td>
<td>468 / 16</td>
</tr>
<tr>
<td>Modulation types</td>
<td>BPSK, QPSK, 16QAM, 64QAM</td>
<td>256QAM</td>
</tr>
<tr>
<td>MCS supported</td>
<td>0 to 7</td>
<td>8 and 9</td>
</tr>
<tr>
<td>Spatial streams</td>
<td>1</td>
<td>2 to 8</td>
</tr>
</tbody>
</table>

#### Modulation and EVM (dB) Comparisons

<table>
<thead>
<tr>
<th>Modulation</th>
<th>Coding Rate</th>
<th>802.11n EVM (dB)</th>
<th>802.11ac EVM (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>…</td>
<td>…</td>
<td>…</td>
<td>…</td>
</tr>
<tr>
<td>64QAM</td>
<td>3/4</td>
<td>-25</td>
<td>-25</td>
</tr>
<tr>
<td>64QAM</td>
<td>5/6</td>
<td>-28</td>
<td>-27</td>
</tr>
<tr>
<td>256QAM</td>
<td>3/4</td>
<td>N/A</td>
<td>-30</td>
</tr>
<tr>
<td>256QAM</td>
<td>5/6</td>
<td>N/A</td>
<td>-32</td>
</tr>
</tbody>
</table>
RF Design Challenges for 256 QAM Modulation

• 256QAM requires **better** error vector magnitude (EVM) performance
  • Transmitter relative constellation error (EVM) spec for 256QAM is -32 dB vs. -28 dB for 64QAM
  • Achieving better EVM requires **better** linearity and phase noise

• Errors may be due to imperfections in
  • IQ modulator,
  • phase noise in LO
  • amplifier nonlinearity

→ But what means “**better**” exactly? How do you translate real RF limitations back up to system-level performances?
Need for “true” RF System simulations
Example: Expand test coverage

- Using modulated signals can point to problems that cannot be uncovered by traditional RF simulations
Need for “true” RF System simulations
Example: Build custom measurement scenarios

- Wireless standards can also be used to test some difficult configurations where traditional RF measurements would fall short

Low-level interferers

High-level interferers
802.11ac Transmitter and Receiver Tests

Transmitter Tests
(Section 22.3.19 in 802.11ac std)

- Transmit spectrum mask
- Spectral flatness
- Transmit center frequency tolerance
- Packet alignment
- Symbol clock frequency tolerance
- Modulation accuracy
- Transmit center frequency leakage
- Transmitter constellation error (EVM)

Receiver Tests
(Section 22.3.20 in 802.11ac std)

- Minimum input level sensitivity
- Adjacent channel rejection
- Nonadjacent channel rejection
- Receiver maximum input level
- Clear Channel Assessment (CCA) sensitivity

No mention of IP3, NF, …!
Need for “true” RF System simulations

In summary:

• Some system specifications are very hard to budget, because it involves mechanisms not modeled in the system simulations
  • Example: TX EVM involves third order nonlinearities, am/am and am/pm conversions, spectral regrowth, memory effects … while system studies are mainly based on simple models.

• This usually results in non optimal design (meaning that margin is taken to be “sure” to get the final spec) and potential overdesign (cost in die size, current consumption …)

• Traditional approaches are no longer sufficient
  • Example: IM3 is often used as approximation of ACLR

➔ Only solution is to optimize the design monitoring the final spec
  • This is particularly true for EVM/ACPR in TX and desensitization in RX
Cluttered Design Flows Prevent Efficient Design & Test

Ideas

System Design

Design Process

EDA World

RFIC Implementation

Pictures are courtesy of Chipworks

Validated Design

Connecting Design to Validation

Validation Process

RF Test

RF Test

Measurement World

EDA World

Pictures are courtesy of Chipworks

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“Designing with 4G Modulated Signals for Optimized Multi-standard Transceiver ICs”
Enablement of “true” RF System simulations

OK, I agree with the value of using modulated signals during my RFIC design, but:

• Can I really run EVM or ACPR measurements in reasonable simulation times?

• Where do I get modulated signals from and how can I perform such measurements in my IC environment?

• Does every designer has to understand a wireless standard? Looking at all these “system” parameters is really overwhelming!

• Can I perform the same measurement as later in the lab?
How to address the simulation speed bottleneck?

- You can’t perform RF System measurements (ACPR, EVM, …) with HB analysis and Transient would be too slow.

- Envelope analysis can simulate complex signals much faster than a Transient engine (> 100x speed-up).

- But also “Standard” Envelope engines can’t be used effectively as part of the design cycle.

- GoldenGate offers a “Fast Envelope” option as part of its Envelope Transient (ET) analysis that provides another dramatic speed improvement (up to several 1000x).
Fast Envelope – Flow integration

- The Fast Envelope technology is embedded so that designers would not have to perform additional tuning compared with classical Envelope.
- The internal flow is designed to be seamless for the designer.

Netlist & Run

Run HB with:
- power sweep: nonlinearity
- frequency sweep: memory effects

Create model kernels

Save "FCE" model

Run model with desired modulated waveform
## Envelope & Fast Envelope Engines
### Fast Envelope Transient - Basic Principles

<table>
<thead>
<tr>
<th>Level 1</th>
<th>“Simplified” Model Topology</th>
<th>Characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AM/PM</td>
<td>static input/output</td>
</tr>
</tbody>
</table>
| Level 2 | ![In-band filtering](image) | including:  
  I. in-band: the gain variations with the frequency over the modulation bandwidth |
| Level 3 | ![Out-band filtering](image) | including:  
  I. in-band: the gain variations with the frequency over the modulation bandwidth  
  II. out-band: the modulation resulting from low dynamic variations of biasing point |
Provide RF System Test benches in an IC Environment

- GoldenGate offers various approaches to enable standard-compliant system tests within the Virtuoso platform.

- These scalable links support various levels of interaction ranging from simple input/output file exchange to full co-simulation with data flow engines.

- 4G sources and sinks are either available through SystemVue and Agilent test equipment (Signal Studio / VSA software).
Consistent RF System Verification
System Design – RFIC Design – Lab Test

WLAN 11ac Receiver Sensitivity Testbench in SystemVue

Signal Studio
Create custom test signals

VTB source
RFIC in Virtuoso
RF RX Model
FCE
VTB sink

Signal Generator
Lab Test

WLAN 11ac 'Golden' Transmitter
802.11ac Source
Path Loss
Noise
Noise Density
BER & FER Tests
802.11ac Receiver

Baseband I&Q Output
Direct Conversion Receiver

Signal Analyzer
VSA
Enabling RF System simulations for RFIC Designer

New Verification Test Benches (VTB)

- VTB are parameterized, pre-configured Test Benches from SystemVue
- Allows RFIC designer using GG to easily validate his circuit performance against modulated metrics like EVM, BER, or ACPR
- User can also create custom VTBs
Enabling RF System simulations for RFIC Designer

New Verification Test Benches (VTB)

4G pre-configured VTB test benches:

- LTE
  - BS_Rx
    - 3GPP_LTE_BS_AdjacentChannelSelectivity.wsv
    - 3GPP_LTE_BS_InChannelSelectivity.wsv
    - 3GPP_LTE_BS_ReferenceSensitivity.wsv
  - BS.Tx
    - 3GPP_LTE_BS.Tx.wsv
    - 3GPP_LTE_BS.Tx_SourceOnly.wsv
  - UE_Rx
    - 3GPP_LTE_UE_AdjacentChannelSelectivity.wsv
    - 3GPP_LTE_UE_ReferenceSensitivity.wsv
  - UE.Tx
    - 3GPP_LTE_UE.Tx.wsv
    - 3GPP_LTE_UE.Tx_SourceOnly.wsv
  - LTE_Advanced
    - BS.Tx
      - LTE_Advanced_BS_CA.Tx.wsv
      - LTE_Advanced_BS_CA.Tx_SourceOnly.wsv
    - WLAN_11ac
      - Rx
        - WLAN_802.11ac.AdjacentChannelRejection.wsv
        - WLAN_802.11ac.NonAdjacentChannelRejection.wsv
        - WLAN_802.11ac.ReferenceSensitivity.wsv
      - Tx
        - WLAN_802.11ac.Tx.wsv
        - WLAN_802.11ac.Tx_SourceOnly.wsv

Also other examples are available:
ACPR & EVM measurement, QAM16_SER_vs_EbNo
Demo 1: New Verification Test Benches (VTBs)

1. Setup your ET analysis

2. Set “ET Stimulus” to VTB

3. Select a pre-defined VTB testbench

4. Run Envelope simulation

5. Results display
Going beyond RF System Verification
Leverage Modulated Signals during the Design Phase

• Refine the RFIC specification and optimize your design against RF-system critical metrics early on
  • Demo: Leverage FYC-ET to optimize the ACPR of a Power Amplifier

• Provide an accurate RF model representation back to the System lead for his comprehensive verification runs
  • Demo: FCE model used in an LTE Uplink test in SystemVue

• Using modulated signals to design and optimization compensation against true system metrics
  • Demo: Envelope Tracking
Optimize your design against RF-system metrics
Fast Yield Contributor (FYC)

- GoldenGate provides a Fast Monte Carlo analysis mode
- FYC permits fast mismatch & process variation analysis
  - Up to 60X speed improvement in harmonic-balance simulations
  - Little to no loss in accuracy
- Contribution Tables can optionally be produced
  - Provide detailed breakout of the impact of each device in the design
Demo 2: Using FYC in Envelope to optimize ACPR

R1 and R5 = 380 Ohms

R1 and R5 = 300 Ohms

Histograms of Output Power and ACPR for different R1 and R5 values

R1 & R5 show most contribution
Fast Circuit Envelope (FCE) Models for SystemVue

- FCE behavioral model is exported from RFIC circuit tools
- Runs *native* at the system-level in *seconds*
- Accounts for
  - Power-dependence
  - Frequency-dependence
  - Nonlinear memory effects
  - Frequency translation
  - ZeroIF/DC and RF carriers
  - Multiple I/O ports
  - Internal nodes
Demo 3: FCE model used in an LTE Uplink test

Coded LTE UL
5 MHz source
SystemVue W1910/W1918 library

Spectrum Analyzer
ResBW=30000Hz
Start=0ms
Mode=ResBW
Stop=0.01s
Start=0s
CCDF

Manage-Model
1. GoldenGate Cosim
2. FCE level 1, amplitude accuracy 5
2. FCE level 3, amplitude accuracy 5, frequency accuracy 1
2. FCE level 3, amplitude accuracy 5, frequency accuracy 2

RFIC CMOS PA
“FastCircuitEnvelope” model exported from GoldenGate

89600 VSA
LTE demod

SCRIPTTABLE ENVIRONMENT
SCRIPTTABLE PARAMETERS

NomGain = -15
-50 -15
Gain=0.178 \[10^{\text{NomGain}/20}\]

Anticipate — Accelerate — Achieve

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“Designing with 4G Modulated Signals for Optimized Multi-standard Transceiver ICs”
Reliable system-level performance in seconds

Nominal LTE result (0.4% EVM)

- **Pout** = +10.6dBm, **ACLR**=37dBC
- CPU time = 3 sec (150k points)

LTE result – Compressing PA (20% EVM)

- **Pout** = +19.3dBm, **ACLR**=23dBC
- CPU time = 3 sec (150k points)
Demo 4: Using modulated signals for Envelope Tracking

Simulate power amplifier with modulated input signal and corresponding envelope tracking bias voltage
Summary

• Bridging design and system-level verification by introducing new formalisms & technologies

• Fast Envelope enables reasonable simulation performance for “true” RF System measurements at IC level

• Pre-defined test benches allow RFIC designer to easily validate RF system performance specs

• Provides a complete solution across System Design, RFIC Design and Lab Test

➔ Go and try it out yourself!!
Additional Resources


Previous webcasts on this topic:

- LTE-Advanced: Overcoming Design Challenges for 4G PHY Architectures
- Accelerate 802.11ac/ad System-Level Design & Verification for Next-Generation WLAN
- Memory Effects in RF Circuits: Manifestations and Simulation
- A Model Based Approach for System Level RFIC Verification
- A Practical Approach to Verifying RFICs with Fast Mismatch Analysis
- RF Power Amplifier Design Series: Part 5: Envelope Tracking Simulation and Analysis
- YouTube Video: “Fast Circuit Envelope Models for RFIC verification” [http://www.youtube.com/watch?v=7k8TS2Due70](http://www.youtube.com/watch?v=7k8TS2Due70)
You are invited to our next webcast

Automating SPICE Library Validation

October 22 – 10AM PT

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