Embedded Debug
Overcoming Design Challenges
Using Agilent Logic Analyzers, Oscilloscopes, and Protocol Analysis Tools

Alex Dickson
Sales Development Engineer
Agenda

- Review of Embedded Systems
  - Definition
  - Examples of Embedded Systems
  - Challenges Faced by Embedded Designers
- Test Instruments for Embedded Debug
- Application Solutions by Technology Type
  - Field Programmable Gate Arrays (FPGAs)
  - PCI Express Embedded
  - DDR Embedded Memory
An **embedded system** is a special-purpose system in which the **computer** is completely encapsulated by the device it controls. Unlike a general-purpose computer, such as a personal computer, an embedded system performs one or a few pre-defined tasks, usually with very specific requirements.

Review of Embedded Systems
   Definition
   Examples of Embedded Systems
     Challenges Faced by Embedded Designers
Test Instruments for Embedded Debug
Application Solutions by Technology Type
   Field Programmable Gate Arrays (FPGAs)
   PCI Express Embedded
   DDR Embedded Memory
Examples of Embedded Systems

- MP3/Video Player
- Set Top Box
- Wireless Router
- Cell Phone
Examples of Embedded Systems

Xilinx Virtex 5 ML505 Development Board

- Xilinx Virtex 5 FPGA
- Can contain DDR memory controller, uP core(s), PCIe endpoint logic, DSP block, and/or custom design logic
Examples of Embedded Systems

Xilinx Virtex 5 ML505 Development Board

- Mictor 38-pin connector for Trace/JTAG
- Agilent Soft Touch Pro Landing Pad
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► Test Instruments for Embedded Debug

► Application Solutions by Technology Type
  ▪ Field Programmable Gate Arrays (FPGAs)
  ▪ PCI Express Embedded
  ▪ DDR Embedded Memory
Challenges of Embedded Design

► Be First to Market
  ▪ Win early adopter market share while also maximizing profits

► Miniaturization
  ▪ Consider the ever shrinking cell phone
  ▪ Integrate many functions inside ASIC/FPGA – reduce IC count (also for low power)

► Design for Low Power
  ▪ Maximize battery life

► Low Cost
  ▪ Strong competition in the consumer market drives cost efficient design

► Application Growth
  ▪ More applications and more features leads to greater performance demand

Then…

Now!!
Challenges of Embedded Design

What can Agilent Do To Help??

► Be First to Market
  ▪ Provide test tools with low learning curve and powerful debug capabilities to find elusive problems as quickly as possible

► Miniaturization
  ▪ Largest variety of probing choices w/ InfiniiMax compatible flying lead accessories
  ▪ 17-Channel Soft Touch probe

► Design for Low Power
  ▪ Provide minimal probe loading with accurate signal response
  ▪ Offer good signal integrity test tools to assist designers with the trade-offs between timing, power, and noise

► Low Cost
  ▪ Minimize design-for-test overhead

► Application Growth
  ▪ System performance characterization and analysis tools
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## Agilent Logic Analyzer Families

### Modular Systems

<table>
<thead>
<tr>
<th>Agilent 16900</th>
<th>2-slot Mainframe 16901A and 16950B and 16951B State/Timing Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Up to 256M Record Length</td>
</tr>
</tbody>
</table>

### Portable

<table>
<thead>
<tr>
<th>Agilent 16800</th>
<th>15” Display</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Optional Pattern Generator</td>
</tr>
<tr>
<td></td>
<td>4GHz Timing Zoom</td>
</tr>
<tr>
<td></td>
<td>Up to 32M Deep Memory</td>
</tr>
</tbody>
</table>

### Hosted

<table>
<thead>
<tr>
<th>Agilent 1690</th>
<th>Cost Effective Portable Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Utilizes Same Agilent Standard GUI Interface</td>
</tr>
</tbody>
</table>
Logic Analyzer Probe Options

Physical probes

First Logic Analyzer 1973
“3M” 40-pin Single-Ended 17 Channels

“Mictor” Single-Ended 34 Channels 3pf loading 600Mb/s
“Samtec” Single-Ended Differential 34 Channels 1.5pf loading 1500Mb/s
Soft Touch Connectorless Single-Ended Differential 34 Channels <0.7pf loading >2500Mb/s
Flying Leads Single-Ended Differential Accessories 0.9pf loading 1500Mb/s
½ Size Soft Touch Connectorless Single-Ended 17 Channels <0.7pf loading >2500Mb/s

Virtual probes

Soft Touch Pro Connectorless Single-Ended Differential 34 Channels <0.7pf loading >2.5 Gb/s
Industry Standard Footprint

FPGA Dynamic Probes for Xilinx and Altera
Logic Analyzer Probing – Soft Touch

Soft Touch Probes

- Half-size Soft Touch: E5396A, E5398A
- Soft Touch: E5387A, E5390A, E5394A
- Pro Series: E5402A, E5404A, E5405A, E5406A

= 40 pin probe cable compatible  = 90 pin probe cable compatible

Retainer used for alignment and retention only

Individual micro spring-pins adjust to target planarity

4-point “crown” tip makes reliable connection, even through contamination

Half-size Soft Touch

= 40 pin probe cable compatible  = 90 pin probe cable compatible

Agilent Technologies
View Scope

Deep scope waveforms integrated into logic analyzer display

Simple connection with standard BNC/LAN cables

Tracking timing markers between instruments

FREE – standard capability on all Agilent logic analyzers
## Agilent Mid-Range Oscilloscopes

<table>
<thead>
<tr>
<th>Portable 6000 Series</th>
<th>Infiniium 8000 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-4 ch, 100 MHz-1 GHz bandwidth</td>
<td>4 ch, 600 MHz-1 GHz bandwidth</td>
</tr>
<tr>
<td>Industry’s highest resolution displays: XGA with 256 intensity levels</td>
<td>Extensive applications suite including jitter analysis and compliance testing software</td>
</tr>
<tr>
<td>Vector signal analysis option</td>
<td></td>
</tr>
<tr>
<td>Fast waveform update rate: 100 k waveforms/s</td>
<td></td>
</tr>
</tbody>
</table>

### Analog:

- 16 digital timing channels time correlated with analog channels:
  - Mixed signal oscilloscope (MSO)
  - Pattern and mixed-signal triggering

### Digital:

- FPGA dynamic probe application

### Serial:

<table>
<thead>
<tr>
<th>Portable 6000 Series</th>
<th>Infiniium 8000 Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>I²C, SPI, CAN, and LIN trigger and decode (USB trigger)</td>
<td>I²C, SPI, CAN, USB and Ethernet serial decode and analysis</td>
</tr>
<tr>
<td>Up to 8 Mpts MegaZoom deep memory</td>
<td>Up to 128 Mpts MegaZoom deep memory</td>
</tr>
</tbody>
</table>
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  - PCI Express Embedded
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Field Programmable Gate Arrays (FPGAs)

► FPGA Based Embedded Designs
  ▪ Can be used to synthesize soft/hard processors, communication devices (ex. UART), and specialized state machine controllers
  ▪ Increasing performance and gate density allows integration of many embedded elements in one FPGA

► FPGA Test Challenges
  ▪ Limited number of debug pins
  ▪ Large number of internal nodes
  ▪ High design resource utilization
FPGA Solutions - Dynamic Probes

- B4655A Xilinx FPGA Dynamic Probe
  - Industry First FPGA Dynamic Probe
  - Intelligent Core
    • Auto state/timing setup, auto threshold setup
  - CDC File Import to Load Signal Names
    • CDC File (*.cdc) provides signal names from Xilinx tools
  - Auto-pin Mapping
  - Supports Virtex-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan-3

- B4656A Altera FPGA Dynamic Probe
  - NEW!
  - LAI File Import to Load Signal Names
    • LAI File (*.lai) also includes state/timing and threshold setup
  - Supports Stratix, Cyclone, MAX, APEX, Excalibur
FPGA Dynamic Probe - Overview

FPGA Dynamic Probe SW application supported by 1680/1690/16900

Probe core output

USB/Parallel

Control access to new signals via JTAG

ATC2 Core Or LAI Core

FPGA

Insert Core

PC Board

Also available on Agilent Mixed Signal Oscilloscopes
B4655A Xilinx FPGA Dynamic Probe

Industry first FPGA Dynamic Probe

Real Time Internal Measurements without:

- Stopping FPGA
- Changing the design
- Modifying design timing

Quick Logic Analysis Setup

- FPGA pins to logic analyzer channels
- Signal and bus names

Supports Virtex-5, Virtex-4, Virtex-II Pro, Virtex-II, Spartan-3
B4655A - Xilinx ATC2 Core

- Core Inserted Using Xilinx Chipscope Pro*
- Up to 64 Signal Banks
- Up to 128 Signals Per Bank (256 with 2X TDM)
- State (synchronous) and Timing (asynchronous) Core Types

*Core Inserter or EDK can optionally be used.
B4655A - ChipScope Pro ATC2 Core Insertion

Part of Xilinx ISE Tool Flow
Post Synthesis Core Insertion

- No modifications to source
- Finds signals in “Generate” blocks

ChipScope ATC2 Configuration

- ATC2 Pin Assignments
- Creates *.cdc file for signal name import to logic analyzer

Agilent Technologies
ATC2 MUX Core is Intelligent!!

- Tells Logic Analyzer What Type of Sampling
  - State or Timing Mode
- Tells Logic Analyzer Threshold Voltages
  - TTL, LVTTL, CMOS 5V, etc.
- Test Bank for Auto Deskew with Eye Finder
  - Eye Finder – Provides automatic sample position adjustment to align the logic analyzer’s sample timing to the middle of the data valid window for incoming signals, on a per channel basis.
- Auto Setup Enabled
  - Channel identification is automatic and when combined with signal names from the *.cdc file, means full automatic bus label setup!
B4655A – Configuring Logic Analyzer

1. Cable Connection
2. Device 1 Configuration
3. Import Bus/Signals
4. Core 0 Pin Mapping
5. Import Results

Imported the following bus/signals from F:\V7 Single Core Demo\eagle_demo_v7.cdc

/s2mon/tid<0>
/s2mon/s2mstate<2>
/s2mon/s2mstate<3>
/s2mon/s2mstate<4>
/s2mon/s2mstate<5>
/s2mon/s2mstate<6>
/s2mon/s2mstate<7>
/s2mon/tid<1>
/s2mon/tid<2>
/s2mon/tid<3>...

Mapping pin ATD6 78%
B4655A – Running Logic Analyzer

Highlight Bank and Press OK
What if I have an embedded MicroBlaze core?

- Limited number of debug pins?
- Want automatic setup of the logic analyzer?
- Perform Inverse Assembly with/without cache enabled?
E9524A - MicroBlaze Trace Toolset for Xilinx FPGAs

- Requires minimum number of pins
- Inverse Assembler to reconstruct SW execution
- Small IP block inserted into FPGA design for tracing processor activity
- Probes behind cache

MicroBlaze trace core

![MicroBlaze trace core diagram](image-url)
B4656A Altera FPGA Dynamic Probe

Market leading FPGA dynamic probe includes support for Altera FPGAs

- Multiplexer (Signal Mux)
- Auto channel naming
- Integrated into Agilent logic analyzer GUI

Supports Stratix, Cyclone, MAX, APEX, Excalibur
LAI Core Inserted Using Altera Quartus II Software

Up to 256 Signal Banks

Up to 256 Signals Per Bank

State (synchronous) and Timing (asynchronous) Core Types
B4656A – Quartus II Pin Planner

*.lai File
B4656A – Configuring the Logic Analyzer

1. Cable Connection
2. Configure Device
3. Import Bus/Signals
4. Pin Mapping

Agilent Technologies
Highlight Bank and Press OK
FPGA Dynamic Probes - Summary

► B4655A Xilinx FPGA Dynamic Probe
  ▪ Requires Xilinx ChipScope Pro 6.2i+ (8.2i for Virtex 5)
  ▪ Requires Xilinx JTAG Cable. Supported: Parallel 3 and 4, Platform Cable USB
  ▪ Available as B4655A-011 perpetual node-locked, or B4655A-012 perpetual floating server license

► B4656A Altera FPGA Dynamic Probe
  ▪ Requires Altera Quartus II Logic Analyzer Interface 6.0+
  ▪ Requires Altera JTAG Cable. Supported: Altera USB Blaster or ByteBlaster
  ▪ Available as B4656A-010 perpetual node-locked, or B4656A-020 perpetual floating server license
MSO FPGA Dynamic Probe Application Portfolio

Options for Xilinx
- With 8000 Series MSOs (N5397A)
- With 6000 Series MSOs (N5406A)

Options for Altera
- With 8000 Series MSOs (N5433A)
- With 6000 Series MSOs (N5434A)
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PCI Express Embedded

- Used for chip to chip communication (no slot)
- Supported with licensable IP for FPGAs
  - PCI Express Endpoint LogiCORE for Xilinx (hardened endpoint blocks in Virtex 5 LXT Family)
  - PCI Express IP Core for Altera
- 5.0Gb/s raw encoded data rate (2.5Gb/s per direction, bidirectional)
PCI Express Embedded Testing

Agilent Logic Analyzer & Future Plus Probe

- Agilent 16800/900 Logic Analyzer
- FSI-60112 Analysis Probe (FS4400) x1, x2, x4
- Mid-bus or flying lead (full 2.5Gb/s) probing
- Uses Agilent Packet Viewer Display
Displays parallel bus data at protocol level

Protocol trigger macro allows easy trigger setup, eliminates manual configuration of complex measurements

Time correlation with other system buses

Coverage includes:

- Rapid IO
- **PCI Express**
- USB
- Serial ATA
- Proprietary/Custom Protocols
The Agilent E2960B Series for PCIe2™ provides customers with the fastest time to insight by providing an integrated suite of analyzer and exerciser tools. With data capture users can trust and non-intrusive probing customers can spend their time analyzing their design and bringing their product to market quickly.
The first comprehensive and integrated x1 through x16 protocol analyzer and LTSSM exerciser solution for PCI Express® 1.0 and 2.0 with superior midbus probing

3. The Protocol to Logic gateway (P2L gateway) allows correlation to the Agilent Logic Analyzers → Obtain broad visibility into all parts of the system

2. Link Training and Status State Machine (LTSSM) exerciser for effective link negotiation testing → Isolate failures for expedited troubleshooting

1. Non-intrusive analyzer that provides authentic system view → Genuine and unaltered signal characteristics
Features of the Agilent E2960B Series for PCIe 2™

- **P2L gateway**
  - Full system viewing by using **P2L gateway** to connect the logic analyzer for cross correlation to memory and FSB (front side bus)
  - Unique logic and protocol functionality in a single solution understand the data from layer 1 to the transaction domain
  - Thorough link testing using the **X1 to X16 LTSSM exerciser** to generate training sequences at speed on all lanes
  - Exercising the DUT – the fully featured **x4 exerciser** drives the DUT to the limits

- **Protocol Analyzer**
  - Reliable traffic capture and analysis using the **X1 to X16 analyzer**
  - Superior midbus probing with Agilent midbus 2.0: Probe the signal without changing it in any way
  - Two-in-one: A single stimulus and response solution with the exerciser and analyzer

- **LTSSM Exerciser**

= Agilent unique functionality
PCI Express Embedded – SI Measurements

N5425A InfiniiMax ZIF Probe Head

N5426A ZIF Solder-in Tips
PCI Express Embedded - Summary

► Logic Analyzer Solution
  ▪ 16800 Series Logic Analyzer + FSI-60112
  ▪ For Use with PCI Express x1, x2, x4 (2.5Gb/s)

► E2690B Protocol Analyzer and Exerciser
  ▪ Supports PCI Express 1.0 and 2.0
  ▪ P2L Gateway for cross-correlation with logic analyzer

► Infiniium Real-time Oscilloscope SI and Compliance Test Solution
  ▪ Minimum of 6GHz Infiniium
  ▪ InfiniiMax 1134A or 1168A/1169A Probe
  ▪ N5425A and N5426A ZIF Probe Head (or one of other available probe heads)
  ▪ E2688A SDA Software (Clock Recovery and Real-time Eye)
  ▪ N5393A Compliance Test Software – if compliance testing is desired
  ▪ E2681A/N5400A EZ-JIT/EZ-JIT Plus Jitter Analysis Software
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  - DDR Embedded Memory
DDR Embedded Memory

- DDR1/DDR2
- No slot
- Typically BGA or TSOP chip package
- Clock rates from 100MHz to 667MHz (DQ data rates from 200MT/s to 1333MT/s)
Agilent E5381A Flying Leads are Full BW up to 1.5Gb/s!!
DDR Embedded Memory – Probe Position

DQS Read and Write Strobes (Read is Collapsed)

Probe at Controller for READ

Probe at DRAM for WRITE

WRITE Eye

READ Eye

Agilent Technologies
DDR Embedded Memory – Functional Test

Standard Listing Decode Display

Transaction Tracker Display
### DDR Protocol and Performance Checker

#### Statistics

<table>
<thead>
<tr>
<th>Statistic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commands Analyzed</td>
<td>12011</td>
</tr>
<tr>
<td>Errors Found</td>
<td>25</td>
</tr>
<tr>
<td>Average Refresh Time</td>
<td>7.808952 us</td>
</tr>
<tr>
<td>Min Refresh Time</td>
<td>7.5645 us</td>
</tr>
<tr>
<td>Max Refresh Time</td>
<td>8.1145 us</td>
</tr>
</tbody>
</table>

#### Errors &Warnings

<table>
<thead>
<tr>
<th>Command</th>
<th>Bank</th>
<th>Row Addr</th>
<th>Col Addr</th>
<th>Banks</th>
<th>Time</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td>3</td>
<td>800</td>
<td>PPAP</td>
<td></td>
<td>15.9645 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>810</td>
<td>PPAP</td>
<td></td>
<td>15.9795 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>810</td>
<td>PPAP</td>
<td></td>
<td>15.9945 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PPAP</td>
<td></td>
<td>16.0095 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PPAP</td>
<td></td>
<td>16.0245 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PPAP</td>
<td></td>
<td>16.0455 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>800</td>
<td>PAAP</td>
<td></td>
<td>72.723 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>810</td>
<td>PAAP</td>
<td></td>
<td>72.738 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>810</td>
<td>PAAP</td>
<td></td>
<td>72.753 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.768 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.783 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.798 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.813 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.825 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
<tr>
<td>Write</td>
<td>3</td>
<td>820</td>
<td>PAAP</td>
<td></td>
<td>72.836 us</td>
<td>Error - Write to bank that is not active</td>
</tr>
</tbody>
</table>

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**Agilent Technologies**
DDR Protocol and Performance Checker

[Image of DDR Protocol and Performance Checker software interface]

- **Functional & Performance Analysis**
  - CAS Latency: 2
  - Additive Latency: 0
  - Burst Size: 4
  - Chip Select: 1

- **Timing Analysis**
  - Read/Write Strobes: 1024
  - % with Data Transitions: 90%
  - Data Bit Max Width: 1.67 ns
  - Data Bit Min Width: 1.67 ns
  - Data Bit Avg Width: 1.67 ns

- **Results**
  - Show When Data Bit Width is <= 4 ns

<table>
<thead>
<tr>
<th>Command</th>
<th>Address</th>
<th>Bank</th>
<th>Card Time</th>
<th>Strobe Time</th>
<th>Bit(s) Meeting Criteria</th>
<th>Bit Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>01318</td>
<td>0</td>
<td>1.992886 ms</td>
<td>1.993787 us</td>
<td>0,4,18,40,41</td>
<td>1.67 ns</td>
</tr>
<tr>
<td>Read</td>
<td>01318</td>
<td>0</td>
<td>1.992093 us</td>
<td>1.993738 us</td>
<td>0,4,18,40,41</td>
<td>1.67 ns</td>
</tr>
<tr>
<td>Read</td>
<td>01318</td>
<td>1</td>
<td>1.992093 us</td>
<td>0.004044 us</td>
<td>0,4,18,40,41</td>
<td>1.67 ns</td>
</tr>
<tr>
<td>Read</td>
<td>01310</td>
<td>0</td>
<td>1.997090 us</td>
<td>2.02374 us</td>
<td>0,4,18,40,41</td>
<td>1.67 ns</td>
</tr>
<tr>
<td>Read</td>
<td>0131C</td>
<td>0</td>
<td>1.997397 us</td>
<td>1.995732 us</td>
<td>0,4,18,40,41</td>
<td>1.67 ns</td>
</tr>
</tbody>
</table>

[Agilent Technologies logo]
EyeScan Measurements

- Single Probe Point
  - Characterization
  - Functional test
- Fast Throughput
  - Minutes vs. hours or days on real time oscilloscope
- Full Bus Characterization
  - Many parallel channels measured simultaneously
Agilent 16800/16900 Series Logic Analyzer

- Depends on DDR speeds (compare MT/s data rates against logic analyzer state speeds in Mb/s)
- Depends on the number and size of DRAMs measured
- Various probe choices: E5381A differential flying leads, N4237A BGA probe (includes one E5381A), N4234A R-pack probe, or Soft Touch

Future Plus Embedded DDR Decode

- FS-1125 for DDR1 (up to 400MT/s) – Requires 16900 System
- FS-1124 for DDR2 (up to 533MT/s) – Requires 16900 System