Aliasing when $F_{\text{Harmonic}} > F_{\text{Nyquist}}$

- 500MHz Bandwidth Scopes
- Input = 50MHz Clock w/ 500ps rise time
Logic Performance

**Logic Channels:**
- Sample Rate = Max toggle or clock rate x 10
  - Timing Resolution = +/- one sample period

- Logic channel performance should be commensurate with scope channel performance

*Logic channel probes must deliver signals to the acquisition system*
Required Digital/Logic Performance

Agilent’s Recommendation: Logic-timing Sample Rate = Clock Rate x 10

200MHz Clock Input

Displayed Logic Waveform @ 2GSa/s

2.5ns

1ns Uncertainty

Sample uncertainty @ 2GSa/s = +/- 500ps
Digital & Analog Acquisition of a System Clock

Input Clocks = 200MHz, 1Vpp, 1ns delay

Analog Acquisition = 1GHz BW @ 4GSa/s
Digital Acquisition = 2GSa/s
How Much Memory is Required

- Step #1: Determine required sample rate
  - Usually based on fastest clock rate

- Step #2: Determine longest time-span to acquire
  - Usually based on slowest analog signal or digital packets

Memory Depth = Time-span/Sample Interval

Note that a scope’s sample rate is a function of memory depth.
Example: Capture 40MHz Clock (crystal output)
Capture 1.0 ms Time-span (100μs/div)

Required $BW_{\text{min}} = 200$MHz (clock rate x 5)
Required Sample Rate $\text{min} = 800$MSa/s (BW x 4) =~ 1GSa/s
Required Memory Depth $\text{min} = 1$MB (1ms/1ns)

Max-Specified Sample Rate = 5GSa/s
Memory Depth = 10kB
Auto-Adjusted Sample Rate = 10MSa/s

Max-Specified Sample Rate = 4GSa/s
Memory Depth = 4MB
Auto-Adjusted Sample Rate = 4GSa/s

Under-sampling produces seriously aliased waveform results!
What Type of Triggering is Required?

**Simple Pattern Triggering**
- Analog AND Digital?
- Synchronized?
- Time-Qualified?
- Non-Sampled-based?

**Advanced Digital Triggering**
- Pattern Duration?
- Pattern Sequencing?
- Serial (I²C, SPI, CAN, LIN, etc.)?

---

**CAN Duration**
- I²C
- LIN
- Sequence
- SPI (2&3 Wire Serial)
- TV
- USB

**Trigger**
- I²C

**Sequence Stages**
- First, find: Pattern 1 Entered
- Then, trigger on: Pattern 2 Exit
- Reset on: Timeout

**Pattern**
- Sequence Stages
  - First, find: Pattern 1 Entered
  - Then, trigger on: Pattern 2 Exit
  - Reset on: Timeout

**Pattern =**
- 1 XXXX 4 D15 XXXX XXXX XXXX LHL L D0
Why is **Synchronized** Pattern Triggering Important?

User-specified Trigger Condition: LHLL (0100)

Where should the scope trigger?

D3

D2

D1

D0

LHLL

Where should the scope trigger?
Stable Triggering Requires **Synchronized** Pattern Triggering

Non synchronized pattern triggering

Unstable pattern triggering when PRESENT.

Synchronized pattern triggering

Stable pattern triggering when ENTERED.

MSOs should trigger at **beginning** of pattern – not **WHENEVER**!
Why is **Time-qualified** Pattern Triggering Important?

User-specified Trigger Condition: HHLL (1100)

Where should the scope trigger?
Stable Triggering Requires *Time-Qualified* Pattern Triggering

**Non-time-qualified pattern triggering**

Without time-qualification, scope triggers on unstable/transitional states.

**Time-qualified pattern triggering**

With minimum time-qualification, MSO does not trigger on unstable conditions.

Minimum *time-qualified* triggering filters-out transitional switching states
Why is Real-time Pattern Triggering Important

Real-time Logic Triggering:

D0 – D7 Input
Threshold Level

Pattern Recognition Circuitry
Scope Trigger

Sample-based Logic Triggering:

D0 – D7 Input
Threshold Level

Pattern Recognition Circuitry
Scope Trigger
Logic Sample Clock
Stable Triggering Requires **Non Sample-based Triggering**

**Trigger Condition:** Trigger on rising edge of D4 (A4) during specified pattern

Sample-based pattern triggering induces **Trigger Jitter**

(±/− sample period of p-p jitter)

Analog/real-time pattern triggering minimizes **Trigger Jitter**

(10 ps RMS typical for 1-GHz scope)
Not All MSOs are Created Equal!

An MSO Provides

- *Time-aligned scope and logic channels*
- DSO *ease-of-use*
- *Full DSO functionality*
- Suitable *acquisition performance*
- *Mixed-signal* triggering
- *Synchronized* pattern triggering
- *Time-qualified* pattern triggering
- *Real-time* pattern triggering
- *Serial* bus triggering and analysis
When is an MSO Not the Right Solution?

- When more channels are required
- When state analysis, source code required
- When higher performance is required

Dual Instrument Solution

Trade-offs:
- Complexity of use
- Expensive
- Slow update rate
Other Oscilloscope Characteristics to Consider

- Waveform Update Rate
- Advance Analysis
- Display Quality
- Ease-of-use
- Probing
- Price
Polling Question #3

Which type of instrument(s) do you believe best fit your waveform measurement requirements?

A. Convention analog or digital oscilloscope
B. Logic analyzer
C. Mixed Signal Oscilloscope (MSO)
D. Oscilloscope + logic analyzer with time-correlation
## Agilent’s Family of MSOs

**MSO6000 Series:**
Optimized for bench-top troubleshooting with industry’s fastest waveform update rates (100,000 waveforms/sec).

**Infiniium MSO8000 Series:**
Optimized for waveform analysis including very deep memory applications (up to 128MB).

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>Sample Rate</th>
<th>Memory Depth (Max)</th>
<th>2+16</th>
<th>4+16</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 MHz</td>
<td>2GSa/s</td>
<td>8M</td>
<td>MSO6012A</td>
<td>MSO6014A</td>
</tr>
<tr>
<td>300 MHz</td>
<td>2GSa/s</td>
<td>8M</td>
<td>MSO6032A</td>
<td>MSO6034A</td>
</tr>
<tr>
<td>500 MHz</td>
<td>4GSa/s</td>
<td>8M</td>
<td>MSO6052A</td>
<td>MSO6054A</td>
</tr>
<tr>
<td>1 GHz</td>
<td>4GSa/s</td>
<td>8M</td>
<td>MSO6102A</td>
<td>MSO6104A</td>
</tr>
<tr>
<td>600 MHz</td>
<td>4GSa/s</td>
<td>128M</td>
<td>N/A</td>
<td>MSO8064A</td>
</tr>
<tr>
<td>1 GHz</td>
<td>4GSa/s</td>
<td>128M</td>
<td>N/A</td>
<td>MSO8104A</td>
</tr>
</tbody>
</table>
InfiniiMax Active Probe Extension

Allows for environmental chamber testing up 105 degrees C.
Move FPGA designs quickly through debug and validation

- **Increased visibility**—measure up to 64 internal FPGA signals for each debug pin, max 1024 internal signals
- **Faster probing changes**—move internal FPGA probe points in less than a second, no design recompiles
- **Automatic setup of MSO**—automatically turn on channels and/or busses and map design’s signal names to channel labels

Insert **ATC2** core with ChipScope Pro Core Inserter

**FPGA Dynamic Probe SW** running on Infiniium MSO or on PC, licensed either to MSO or PC

FPGA Dynamic Probe core output on variety of logic probe connectors to MSO cable

Control access to new signals via JTAG

Optional with Infiniium MSO

**XILINX**

Virtex-4
Virtex-II Pro
Virtex-II
Spartan-3

**Agilent Technologies**
Additional Technical Resources

- Agilent 6000 Series Oscilloscopes (data sheet)

- Agilent 8000 Series Infiniium Oscilloscopes (data sheet)

- FPGA Dynamic Probe for Mixed Signal Oscilloscopes (data sheet)

- Debugging Embedded Mixed-Signal Designs Using MSOs (application note)

- Why Oscilloscope Waveform Update Rates are Important (application note)

- Advantages and Disadvantages of Using DSP Filtering (application note)

- Evaluating Oscilloscope Vertical Noise Characteristics (application note)

- Deep Memory Oscilloscopes: The New Tools of Choice (application note)
Questions and Answers