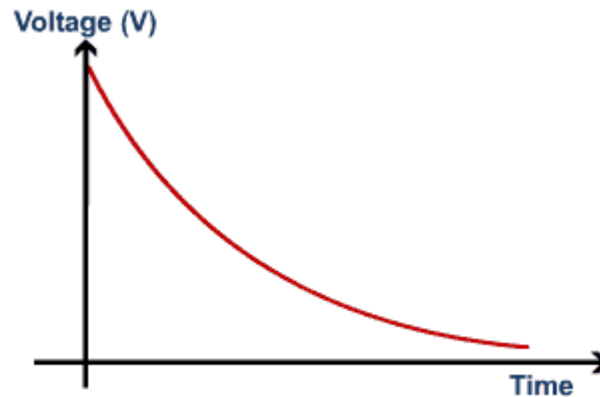


# 3070 PCB Discharge Tutorial



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# Agenda

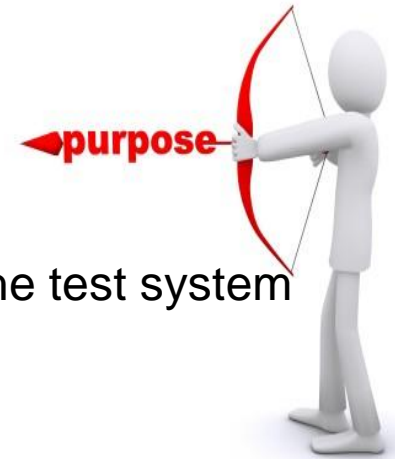
Overview of Discharge

Causes of Discharge Failures

Case Studies

Enhancement of Discharge in Version 8.20p/8.30p

# Overview of Discharge

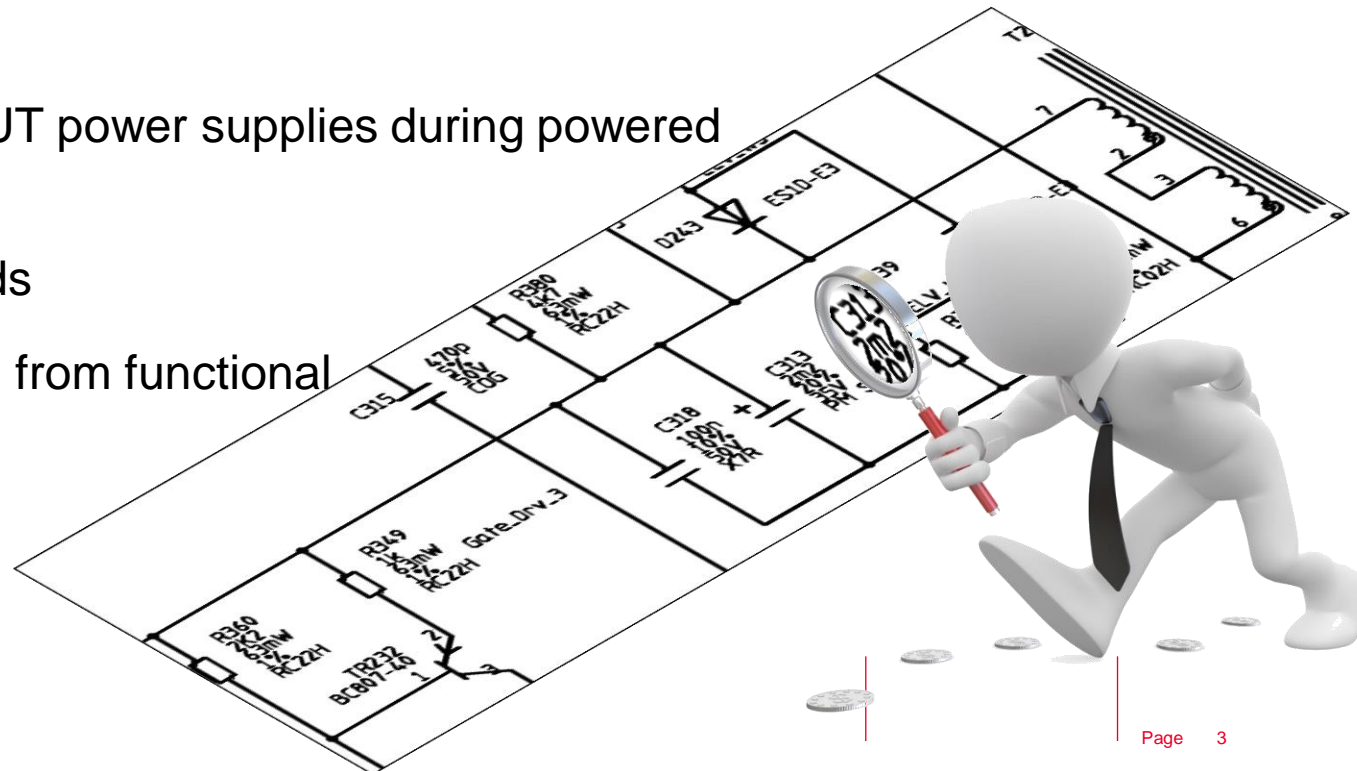


## Purpose of discharge

- To protect the operator, the device under test (DUT), and the test system itself, from damage caused by residual stored voltages.

## How are charges built up?

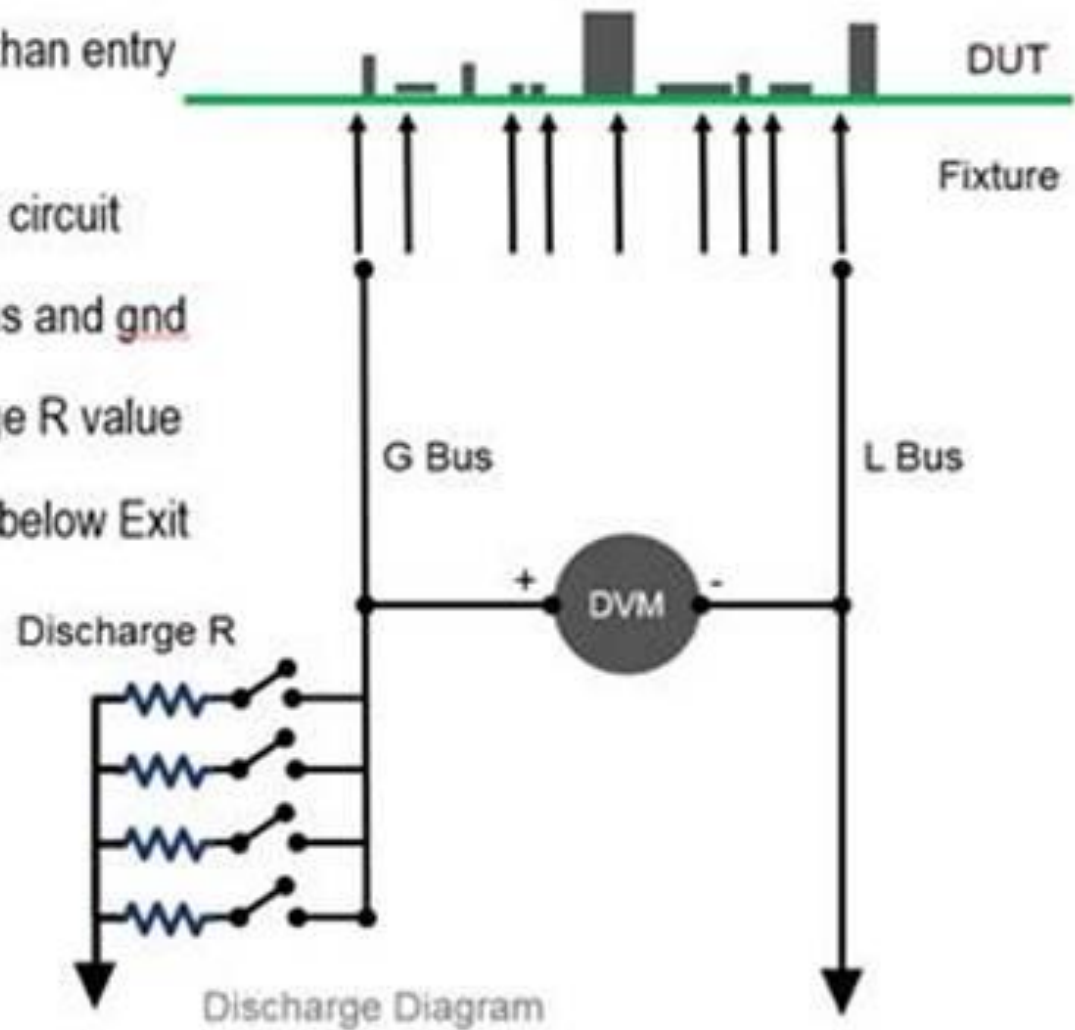
- Applying ASRU sources during in-circuit tests (for example, testing zener diodes).
- Applying the DUT power supplies during powered testing
- Retesting boards
- Returned board from functional test



# Overview of Discharge

How is discharge carried out?

- Voltage on discharge nodes higher than entry level, discharge initiated
- Connect G and L bus into discharge circuit
- Connect Discharge R between G bus and gnd
- Monitor voltage and switch Discharge R value
- Release Discharge R when voltage below Exit value



# DISCHARGE TEST SYNTAX

! Capacitor "c1 2.00m"

!

! Maximum capacitance = 2.20m; damage voltage = 426.4mv

clear connect l to "GND"

connect g to "u1\_3"

discharge "CD1", entry 426m, exit 0.05

- Damage Voltage is the minimum capacitor voltage that could potentially damage pin card relays.
- The capacitor will be discharged if its voltage is the Entry Voltage, or higher.
- The capacitor will be discharged until its voltage is less than the Exit Voltage.
- The "L" bus connection should be the node that is closer to ground.

# Overview of Discharge

**When** does the discharge operation get executed?

- The “unpowered” command.
- Commands to engage vacuum (“faon”, “faoff”, etc.), if the current test mode is “unpowered”.
- “Fixture verify” commands (for example “verify all nodes”), if the mode is “powered”.
- Directly executing the discharge test (test “analog/.discharge”).
- The “dps” command will run a partial discharge (make only 1 attempt to reduce the voltage below 0.05 volts)



# Overview of Discharge

When does the discharge operation **NOT** get executed?

- Incorrect or insufficient information provided during test development which results in a .discharge entry voltage setting that is higher than it should be.
- If the voltage measured between the two nodes was too high to discharge. (>100V)
- Discharge was aborted due to a voltage decrease of less than 20 millivolts per second.
- Discharge timeout. Each discharge subtest must complete in 29.5 seconds.
- If the system is unable to measure the discharge voltage.
- If an over-voltage error condition occurs in the testhead (e.g power supply OV error).
- On a full discharge only, if discharge test has been executed four times, and voltage is still greater than 0.05 volts.



# WARNING BCP718

After IPG, in “summary” file:

“Excessive trapped charges may be present on the board. The sum of all power supply voltages is more than 100 Volts. If trapped charge is present on the board in excess of 100 V, fixture electronics may be required to discharge the trapped charge. Please refer to "Test Methods: Analog" documentation for further details (WARNING BCP718)”

Node Name	PS #	Voltage	Current Limit
j1_3	4	50	.1
u1_3	1	13.8	.4
u2_2	3	37	.1

In “ipg/summary” file:

## Capacitor Discharge Test Summary

Discharge statements = 3

Capacitors not discharged = 0

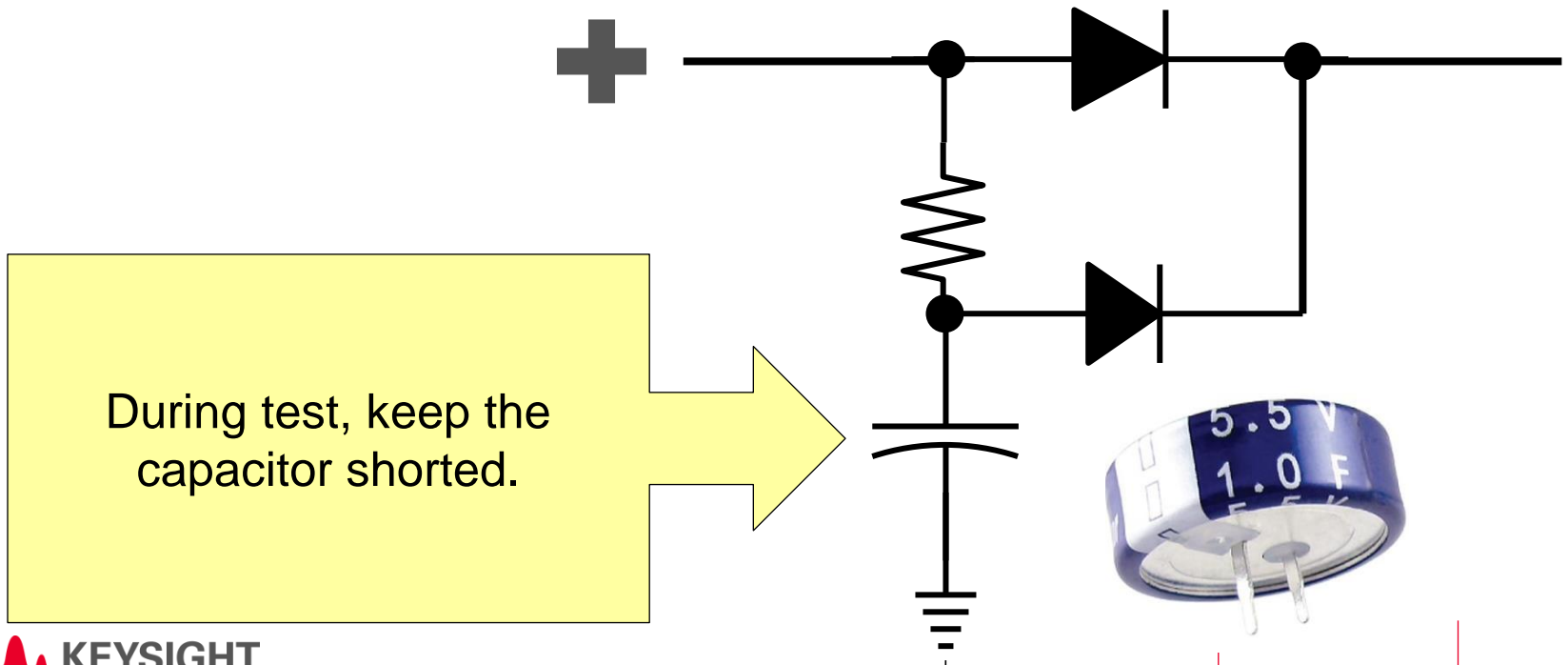
Maximum voltage = 101

Almost all occurrences of WARNING BCP718 are not a problem, because the power supplies are usually not connected in series. However, the test developer should examine the situation to see if any special discharge actions are necessary.



# SUPERCAPS

- May require many, many hours to discharge
- Don't let them get charged up!
- Develop a strategy to deal with boards that return from functional test



During test, keep the capacitor shorted.

# Causes of Discharge Failures

# Causes of Discharge Failures



## Conditions that will cause a testhead exception error

- If the voltage measured between the two nodes is too high to discharge. Greater than 100.0 volts on systems with Revision C/N ASRU cards.
- Discharge was aborted due to a voltage decrease of less than 20 mv/sec.
- Discharge timeout. Each discharge subtest must complete in 29.5 seconds.
- If the system is unable to measure the discharge voltage.
- If an over-voltage error condition occurs in the testhead.
- If the discharge test has been executed four times, and voltage is still greater than 0.05 volts



# Causes of Discharge Failures

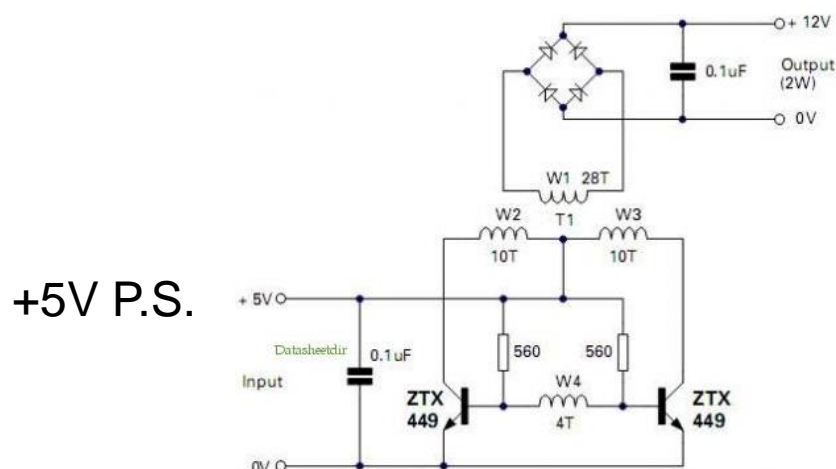
## Possible causes of discharge failures

- Batteries or “super caps” on the board that are not properly discharged. These devices should be discharged through GP relays or other fixture electronics. Batteries, generally, should not be installed on the board during test. If batteries must be on the board during test, you should avoid probing the nodes directly connected to the batteries. The battery should be isolated by an open jumper or other means.
- The discharge routine could actually be in error if an ECO has occurred and someone has mistakenly used the “permanent” option on the “.discharge” file in “testorder”. It is **STRONGLY RECOMMENDED** that the “permanent” option **NEVER BE USED** with the “.discharge” file.
- It is important to note that the automatically generated routine only discharges capacitors. If an inductor (or any other device) on the board under test has significant internal capacitance, you either need to enter that capacitance in the board forms, or create your own entry in the discharge file.

# Causes of Discharge Failures

## Possible causes of discharge failures

- Voltage converter which produces voltages higher than those supplied by the system power supply settings on the DUT, like a DC to DC converter.
- Enter the extra internal voltage into the IPG Global Options as “Additional Board Voltage”
- Add the associated internal power rail nodes into the “Fixed Nodes” list.



Additional Board Voltage: 7 volts

# Causes of Discharge Failures

## Possible causes of discharge failures

- **Fixture electronics.** If the fixture electronics contains any capacitors that the system doesn't know about, you could have problems. IPG will only create discharge tests for capacitors entered in board forms. It is best to model the additional capacitance by entering the fixture electronics into board forms.
- Supplemental discharge circuitry and/or routines may need to be added.
- Analyze all fixture electronics to make sure that an appropriate discharge mechanism is in place.

# Test Development Guidelines

- Define correct values for devices on board.
- Load and No-load devices needs to be accurate.
- Define Power/fixed nodes and high voltage nodes in “board” file.
- Fixtures that contains electronic circuits that retain charge should be described into the “board” file as well, so that discharge can be applied for them.
- Update board files and regenerate the discharge test if there are ECO's or changes to the voltages on the DUT.
- If fixture electronics are not able to be discharged through the system, then separate external discharge is required to be performed.
- Ensure sufficient ground probes.
- Ensure sufficient wiring for ground and power probes.



# Debugging Discharge

- Add an “unpowered” statement before the “faoff” statement
- Connect bleeder resistor(s) prior to “faoff”
- Add a “dummy” analog functional test as the last powered test. The test only needs two statements, “test powered analog” and “end test”.
- Make sure that any custom discharge actions are included in the “Error\_Trap” and “Break\_Trap” routines.





# Case Studies

# Case Study 1

The board under test contains a voltage converter/generator/transformer which produces voltages higher (or negative) than those supplied by the system power supply settings.

As this information usually is not made known to software, it will **not** be taken into consideration during discharge file generation.

Solution:

- Specify the additional voltage in the “board” file (Global Options)

Additional Board Voltage:  volts



- Declare the related nodes as fixed nodes.

# Case Study 2

There is a discrepancy between the “board” file and the real situation. For example, after an ECO, either the “board” file is not updated, or a “.discharge” file is not re-generated, or there are capacitors in the fixture electronics, or devices connected via Performance Port.

Solution:

- Make sure the data in the “board” file is complete, accurate and up to date.
- Always regenerate the “.discharge” file after anything changes in the DUT.

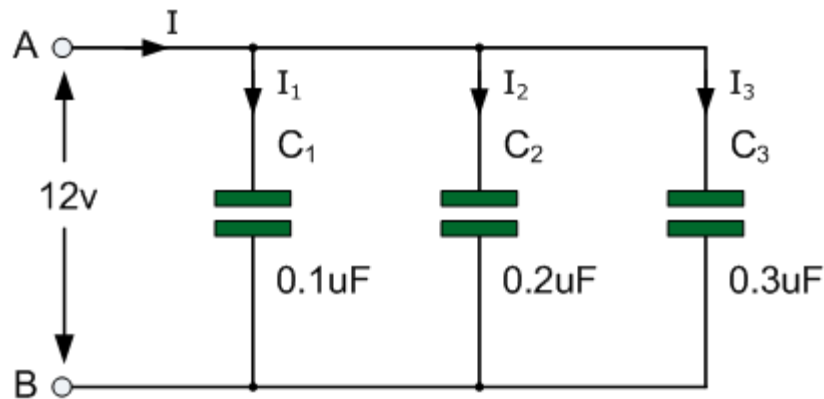
**PROBLEM SOLVED!**

# Case Study 3

The automatically-generated routine only discharges capacitors, while an inductor (or any other device) on the board under test has significant internal capacitance.

Solution:

- Enter this information to the “board” file before generating the “.discharge” file, or manually modify the “.discharge” file.
- Model all capacitances in “board”.



**PROBLEM SOLVED!**

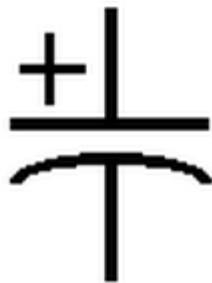
# Case Study 4

Large capacitors, especially electrolytics, have what is sometimes referred to as dielectric memory, or dielectric absorption.

If they are charged up, discharged, and then left alone, a voltage will build up (bounce back) on the capacitor. The voltage built up is not only a function of the voltage previously applied, but also the length of time it was applied.

Solution:

- Discharge the capacitor several times, perhaps at both the beginning and the end of the discharge file.
- In extreme cases, it may be necessary to add a bleeder resistor or GP relay across the capacitor inside the fixture. If this is not sufficient, you could create a loop of your own within the testplan.



# Case Study 5

To increase throughput, some the test engineers will reduce the “faon” vacuum-on delay.

As a result, the discharge routine may be run before the board is fully engaged. So, the discharge routine may be run incompletely.

Solution:

- Change the wait time for “faon” to “1.5s” as the default one, or make it longer if the fixture is slow to engage.
- faon 1.5 !1.5 second



# Enhancement of Discharge in i3070 version 8.20p/8.30p

# Enhancement of Discharge in i3070 version 8.20p/8.30p

## 8.30p software release (2011/2012)



- Users were given options to protect the test system and DUT from damage from the residual energy on the DUT.

Software Rev	Enhancement	Remark
08.20p	Entry Voltage $\leq 2v$ for discharge	
08.30p	Improve IPG discharge with more conservative calculations for .discharge file	APG_DISCHARGE_ROBUST = False (conservative) – Default for 08.30p and later APG_DISCHARGE_ROBUST = True (actual) For 08.20p or earlier





# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Rationale for the change

- Today, the device packaging has shrunk. The operating voltage of devices has also been reduced from 12V to 5V, to 3.3V, 1.8V and even lower.
- These new components are more prone to electronic overstress and need more protection from trapped charges on the board. That is the reason why Keysight has re-engineered and revamped the discharge algorithm for the i3070 test system. Based on the new calculations, the discharge algorithm is more conservative, and more capacitors may be added to the discharge subroutine.

# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Results from the enhancement

- We have received very positive feedback from users and partners worldwide.
- The failure rate for the board and system has dropped significantly. As a result, down time and support cost for the production has been reduced and product quality has been improved across the board.



# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Trade-off for a safer test

- With this enhancement, more on-board capacitors may be added to the discharge routine and this may increase the test time.
- For most cases, this is negligible. But for some, the increases are noticeable.



## Recommendation to minimize impact

- Identify which capacitors are consuming the most discharge time and deal with them separately. Some of the solutions could be adding bleeder resistors in the fixture to discharge them faster.
- Optimize the test program sequence to minimize the number of discharge events. For example, multiple “unpowered” commands in “testplan”.

# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Reverting to pre-8.30p discharge algorithm

- If engineers have thoroughly examined the board information and test programs for potential risk, and want to increase the throughput, the pre-8.30p discharge algorithm can be used.
- “APG\_DISCHARGE\_ROBUST” is an environment variable and by default it is set to “false”. To generate the pre-8.30p discharge test, it needs to be set to “true”.
- IPG will check this when it writes the .discharge test.

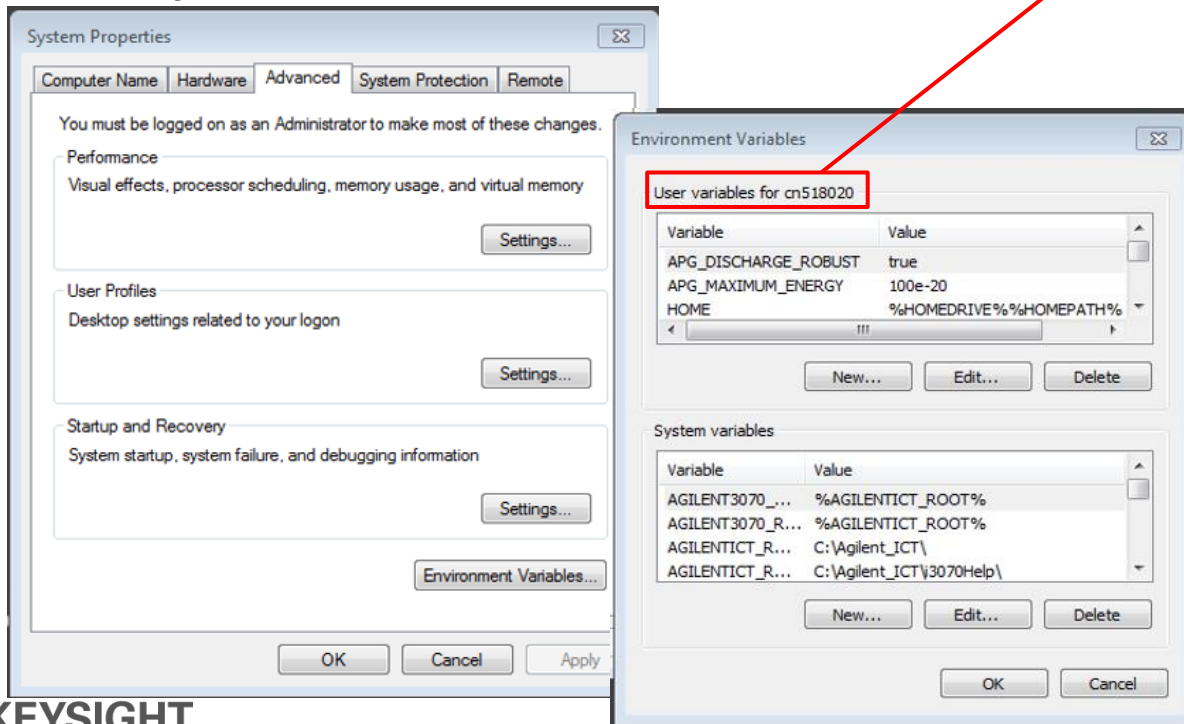


# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Changing the environment variable

- In test development station, “Windows” start menu, choose “Control Panel→System and Advanced system settings→Environment Variables...”
- In the new pop-up window, the first section is called “user variables for xxx” where “xxx” is login user name.

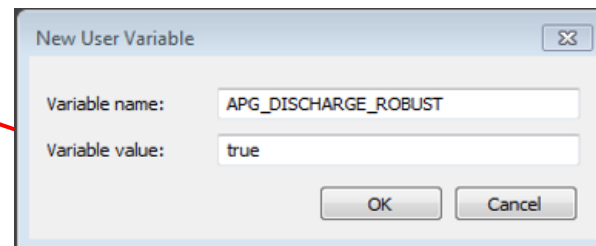
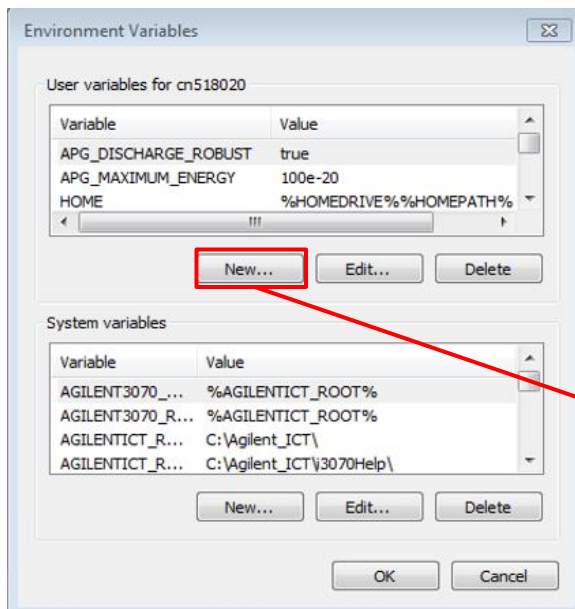


# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Changing the environment variable

- Click “New...” tab and a new a window pops up, enter “APG\_DISCHARGE\_ROBUST” as “Variable name:”, and enter “true” for “Variable value:”. Click “OK→OK→OK” to close all the windows.
- Restart i3070 software and launch IPG or run ‘ ipg on “.discharge” ‘. Open the new “.discharge” file and you will see the change.



# Enhancement of Discharge in i3070 version 8.20p/8.30p



## Changing the environment variable

- After the environment variable has been changed, run IPG test consultant to generate the discharge test for a new program.
- Or for an existing program, run the following command in BT-BASIC to regenerate the discharge file:

```
ipg on ".discharge" | compile ".discharge"
```



# Questions? Comments?





