ESSENTIAL TESTABILITY GUIDELINES FOR CURRENT TECHNOLOGY

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Essential Testability Guidelines for Current Technology

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Abstract

Testability has been addressed by numerous publications and papers in the past. Some of the guidelines proposed have become obsolete because of technology advances or have been difficult to justify and enforce by the manufacturing/test organizations of electronics manufacturers. This paper addresses the ***essential*** *testability considerations, both electrical and mechanical, and focuses on new requirements of current technologies. This paper provides practical insight into how printed circuit boards should be designed to make them testable. Developing discipline in design-for-test practices will inherently provide major savings in time and money in the test development process, reducing overall product costs.*

Introduction

In the past, the ability to test a board or device was limited by the automatic test equipment (ATE). Current ATE now accommodate complex boards and devices. Some new generation ATE can accommodate complex timing requirements, the need to provide deep pattern sets, and address mixed signal requirements. Advanced capabilities include sync-to-clock, triggering, pattern homing, supplemental analog functional capability, and tight coupling of the analog and digital subsystems. Because some of these core test challenges have been resolved, testability is surfacing as the major barrier to effective manufacturing test.

Testability Overview

Whether utilizing a purely in-circuit or functional (edge-card) test methodology, many of the testability requirements are similar. Since in-circuit is still considered a highly cost-effective test approach, most manufacturers strive to utilize this technique. Where design constraints *genuinely* dictate functional test, a combinational test method using in-circuit techniques coupled with selected functional cluster tests can be implemented. Since in-circuit test requires total nodal access and consideration of circuitry surrounding the device-under-test, the list of testability guidelines is more extensive. This discussion will not directly encompass some of the well known functional (both digital and analog) test practices of observability, circuit partitioning, and controllability [7]. However, if relegated to cluster testing, key test points should be provided for control and visibility and to reduce the test generation task. Testability guidelines can be divided into two classes: mechanical and electrical.

Mechanical Testability Guidelines

Test access with printed circuit boards (PCBs) is typically made with vacuum bed-of-nails fixtures. New, higher performance short wire fixtures are now available. In highly automated manufacturing environments, where boards can be delivered to the ATE via conveyors, mechanically actuated fixtures are available. These mechanical *presses* also have increased probing reliability. New mechanical testability guidelines must be considered for these applications.

Providing access to all nodal points is extremely important. Lack of access impacts manufacturability and increases product costs. Nodal access can be provided through device pins (through-hole), test pads (for Surface Mount Technology [SMT] this may be a requirement), connectors, and vias. SMT device pins cannot be probed since the leads may be damaged and open solder connections can be temporarily masked by the probe forcing the lead onto the solder surface [9]. If probing connectors, probe density should be considered

especially when using vacuum bed-of-nails fixtures. Vias are probably the least desirable, since they may not provide the best probing surface, and must be frozen through additional PCB revisions in order to protect the investment of the existing fixture and board test program.

If possible, all test access should be made on the bottom side of the board. In addition, all test pads should have a solder surface to ensure reliable probe contact. Pad diameters should exceed .035 inches (.9mm) when using standard (100-mil) probes [4]. This is true for some of the new vacuum fixtures currently available today. Poorer performance can be expected with other fixture designs. The use of 100-mil (or 75-mil) probes is preferred. 50-mil probes have less probing accuracy (more flex). If utilizing 50-mil probes, pad diameters should exceed .040 inches (1mm). In addition, 50-mil probes are fragile, more expensive, increase fixture maintenance, and provide a less reliable contact.

Test pads should be evenly distributed over the PCB surface. A high probe density on a specific board area may not allow proper sealing with vacuum fixtures, as previously mentioned for connectors. Test pad density should be limited to less than 12 per square inch (8 ounce probes). This will ensure that the board will be coplanar, increasing probing accuracy and decreasing damage to components (PCB flexing). Mechanical fixtures will allow considerably high probe densities, but care must be taken in fixture design.

Standard probes handle approximately 1 amp of current. For probes supplying power to the board, a conservative limit of ½ amp will ensure long term probe reliability and reliable power distribution. Power should be distributed throughout the board. Providing at least three access points for the first 1 amp and an extra access point for additional increments of ½ amp is acceptable. Grounds and returns require considerably more access points especially when testing digital logic. Extra access points should be provided for power supply sense lines.

Engineering change orders (ECO's), including jumpers of components on the probe surface, must be positioned to not interfere with probing. If via probing is required, the vias should be soldered in order to provide a proper probe surface and to ensure probe tips are not caught in unfilled holes. Filling all vias will prevent leakage when using vacuum bed-of-nails fixtures.

For fine-pitch devices, any test pads added can be staggered to attain 100-mil spacing (figure 1). During fixture generation some type of 50-mil probe minimization algorithm should be run to eliminate the requirement for 50-mil probes or significantly reduce their numbers. Typically, an electrical trace can be accessed at more than one location, allowing the use of 100-mil probes by accessing these alternative probe points.

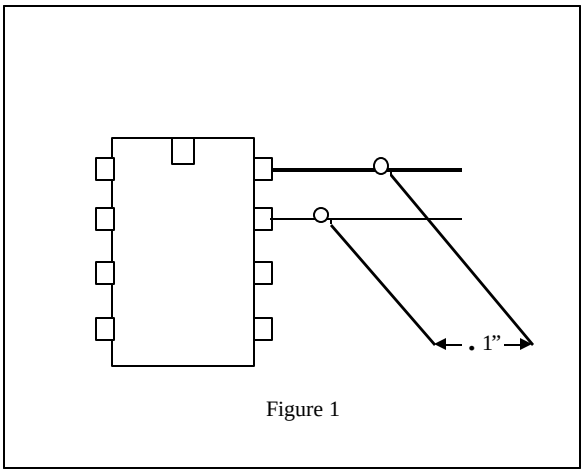


Figure 1

If tall components (> .2 in.) are located on the PCB probe surface, the fixture must be milled and some extra clearance provided for the part. For proper probe socket support, test pads should not be located within .20 inches (5mm) of the component.

If components are located on the probed side of the PCB, clearance should be made between test pads and component leads to avoid damage to the component and to eliminate probe induced shorts (figure 2). Leave a clearance radius of .05 inches (1.27mm).

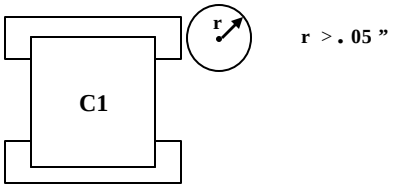


Figure 2

At least .125 inches (3.2mm) of free area should be left around the edge of the board for vacuum fixture seal. Mechanical board handlers may require as much as .138 inch (3.5mm) clearance to accommodate conveyor rails. At least .12 inch (3mm) diameter tooling pins should be used to limit tooling pin flex. Tooling holes should not be plated to avoid contamination with solder and to decrease problems caused by variations in plating thickness. Also, a clearance of .125 inches (3.2mm) should be provided around the tooling pin to provide a seal. Mechanical fixturing systems may require as much as .375 inches (9.5mm) of clearance for self-registering tapered tooling pins. Tooling holes should be diagonally opposed and staggered to prevent incorrect placement on the fixture.

Electrical Testability Guidelines

The most essential electrical testability requirement for a PCB design is to allow all free-running clocks to be disabled (figure 3). Overdriving an oscillator may cause test instability, due to the inability to squelch transients. In addition, free-running oscillators may induce noise not only into the immediate circuit, but into adjacent circuits. The device or circuit is often easier to control if the clock is provided by the test system. Standard device tests can be used if the test system provides the clock. All ATE systems will exhibit some latency if clock synchronization is required. However, some of the newer generation ATE have effectively limited some of this latency improving the resultant edge placement accuracy.

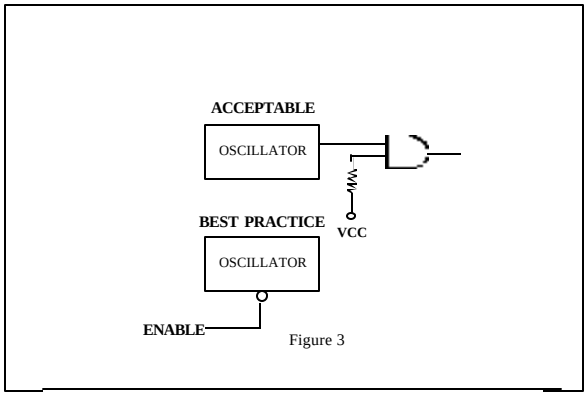
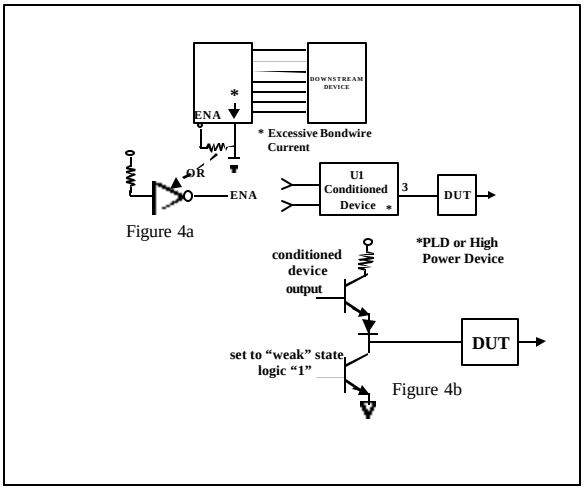


Figure 3

High current/high fan-out devices (e.g. AS, FAST) should incorporate a disabling method. Some of the new generation ATE provide high current backdrive capability and short wire fixtures which offer the ability to provide good signal fidelity at the board/device under test when overdriving high current devices. However, when high fan-out devices are overdriven, the sum of the currents may limit the backdrive time. Therefore, downstream devices/circuits requiring long bit-streams must be identified. A means should be provided to disable or at least condition to a *weak* state high current/high fan-out devices (figure 4a). In this example, the pull-down resistor may be replaced with an unused active device (buffer/inverter) to improve noise immunity on the enable line.

PLDs, ASICs, and other custom devices have a major impact on testability. It is desirable to be able to tri-state (disable) device outputs. Some of these devices may oscillate when they are backdriven. This may cause test instability for all downstream devices. Typically this occurs when the device output is at a logic low (bipolar) and is backdriven to a logic high (figure 4b). Backdriving multiple outputs aggravates the problem. Alternatively, if the outputs can all be placed in a weak state (logic "1" for bipolar), the problem can be eliminated. Remember, this is a consideration that impacts the test of all *downstream* devices. In addition, device enable lines should not be tied in common so that devices can be disabled independently.



Mixed-signal devices can now be exhaustively tested with high performance ATE. However, these devices impose some important design for testability considerations. Analog measurements require long integration times. Upstream device backdrive limitations must be addressed. A

means to disable upstream devices must be provided (figure 5).

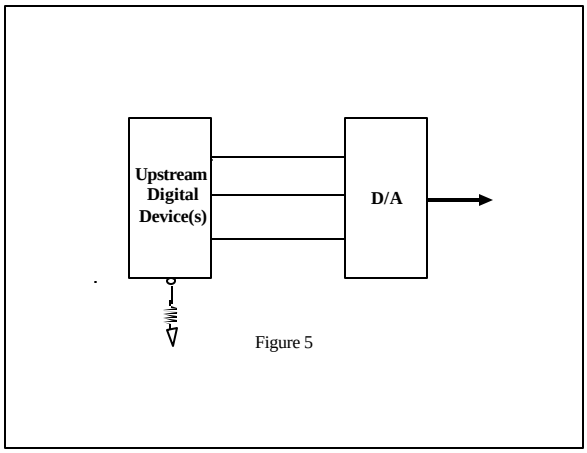


Figure 5

For testability reasons, it is advantageous to provide a means to easily initialize a device. Disabling and initialization with a single pin and test vector is advantageous. The requirement to drive more than one pin with a complex set of vectors complicates the test of surrounding devices. PLDs and custom ASICs should be designed around these criteria.

VLSI devices that operate off internal ROM data may provide a major test dilemma (e.g. 8048 and 8035 micro family). The internal device data may change from board to board and between ECO revisions and cause some unpredictable results. Most of these devices incorporate an *external access* line that allows the ATE to force the device to access external program memory. ATE can then take control and supply the desired repeatable operations if access is provided and the pin is not tied (figure 6). Though not required for product functionality, access to additional lines thatprovide self-test or single-step functions may be valuable [7].

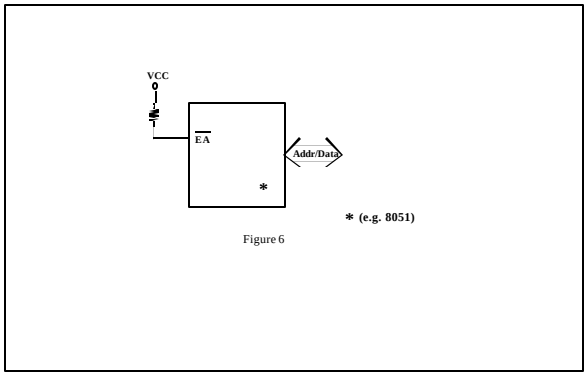


Figure 6

Digital devices should be isolated from RC timing circuits. ATE drivers cannot instantaneously drive these lines to the required states. This will overcomplicate test development and can greatly increase test time. These circuits should be isolated through a resistor, an active buffer, or jumper(least desired) with no effect on circuit function (figure 7).

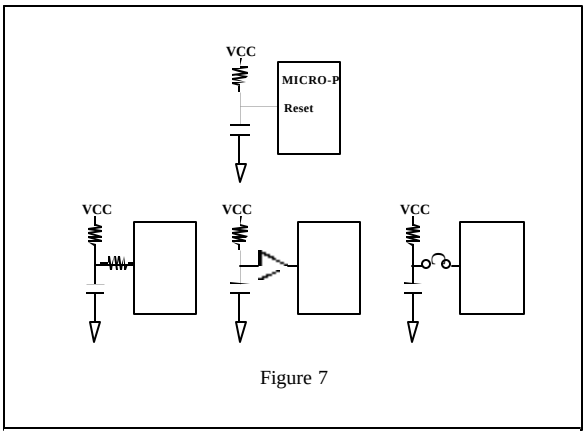


Figure 7

Feedback paths do not create as many problems with some new generation ATE. Some ATE are equipped with high current pin drivers and short wire fixtures which increase the chances that transients will be squelched. For the rare occurrence in which a critical edge-triggered pin is connected in a feedback loop with a high slew-rate/high current device, provision should be made to break the feedback path (figure 8). There may be some good reasons to be able to break the feedback path (add extra gates or disables) for functional test diagnostics [5].

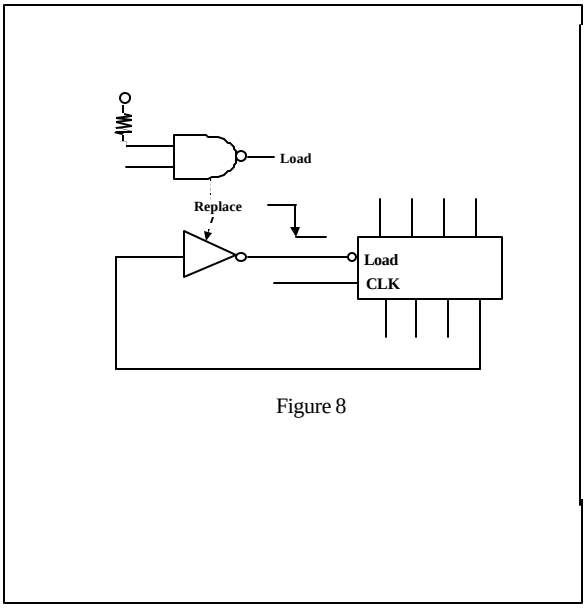


Figure 8

The integration of Electrically Eraseable Programmable Read-Only Memories (EEPROMs) on PCBs has become relatively

common. Traditionally, EEPROMs/FLASH have been tested on ATE, but it may also make sense to *program* the parts during the test process. Most EEPROMs require 10-20 milliseconds to *burn* a location. Often pin states need to be held during this entire write operation. The backdrive limitations of upstream devices must be considered (figure 9). The board design may need to include a provision to condition or disable upstream parts. Some ATE may have a limitation on the amount of backdrive current that can be delivered over time. Specific ATE characteristics should also be included in a testability design study.

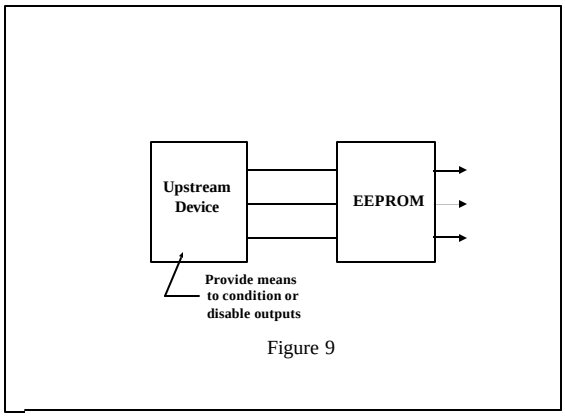


Figure 9

Logic Cell Programmable Gate Arrays (LCAs) have become extremely popular in the last three years. In the LCA the functions of the logic, I/O, and the routing of logic interconnect networks are defined by a configuration program stored in internal memory. A serial PROM (programmable read-only memory) is typically provided on the PCB to provide the configuration program (figure 10). This configuration program will be uniquely defined depending on the application. The personality of all pins may also change between applications, where pins may be programmed as inputs, outputs, or bidirectionals. Also, some input pins may be tied high, low or tied together. Therefore, a generic test program cannot be written. To test each LCA, the functionality of the device in the design will need to be mastered and the patterns developed. This investment in time may not be feasible.

Software tools now exist that allow the test engineer to create a configuration program and test program. The test engineer begins by defining the personality of the pins for the particular application. This program may be installed in fixture PROM's, but a means to deselect the on-board PROM must be provided in the design. Some advanced ATE have the capability to provide long serial bit streams (e.g. Xilinx 3090 requires 64K bits). Rather than complicate the test development process by incorporating PROMs in the fixture, the long contiguous serial bit streams may be provided by the ATE. Once the program is downloaded, the device can then be tested.

In order to program and test the LCA, the on-board PROM needs to be disabled and access to any mode or control pin needs to be provided. Since the LCA controls the PROM chip enable line, provision must be made to allow this line to be overridden during the programming operation (by adding an extra gate or series isolation resistor). In the example (figure 10), the LCA provides a signal to clock data out of the serial PROM. For the ATE to control the configuration function, the device should be configured so that the ATE supplies the clock. This requires the LCA to be set up in a *slave* mode controlled by the *mode* pins. Therefore, the three mode pins shown should be tied to ground through pull-down resistors.

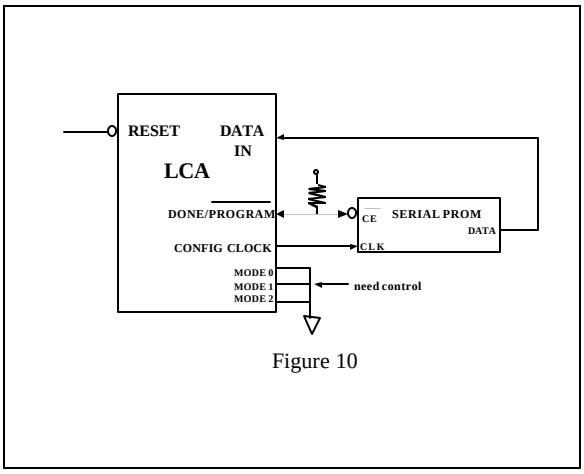


Figure 10

Some of these devices begin their configuration routine after a power-on reset sequence. It is imperative that any external reset line not be tied directly to power or ground so that the ATE can control its function. Also, the reset line should be accessible since it typically allows all pins to be disabled, a possible testability requirement for *downstream* devices. One final consideration is the number of vectors contained in the actual test program (the configuration program is typically a fixed length). When testing for pin faults only, vector reduction may be achieved by testing pins configured as bidirectional in only one direction

(e.g. as outputs only).

It has never been a good design practice to leave unterminated input pins floating. Some new high speed devices (ACT, AS, FCT, F) are prone to oscillate if input pins are not terminated (figure 11). These input pins may be connected to board edge pins where a termination is provided by another board in the product. If possible, terminations should be provided on the PCB. The floating input pins may be driven to a known state by the ATE while other functions are being tested inside the device package. However, an adjacent device with floating inputs may induce noise into the device under test. In this case, it is recommended that pull-up (pull-down) resistors be added to the fixture. Adding pull-up resistors to all floating inputs when the fixture is initially built will simplify test management.

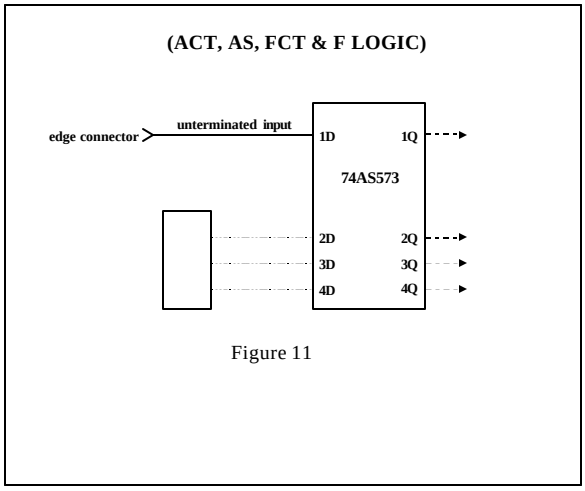


Figure 11

Unused device pins should always be probed and a shorts test performed to eliminate the possibility of undetected shorts (figure 12). The probing of unused gates is also advisable in case they are used in a subsequent ECO of the board. This will also reduce the impact of the ECO on the existing fixture.

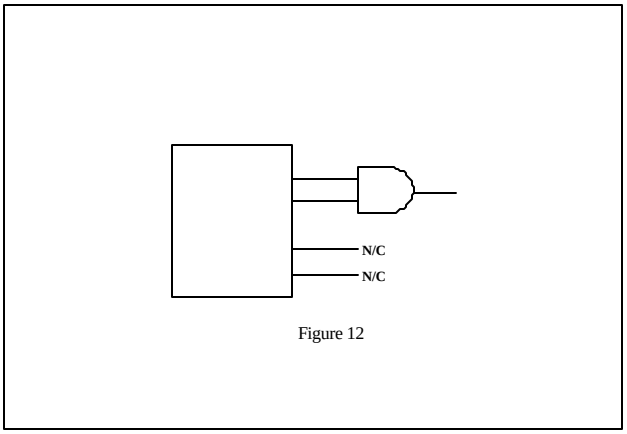


Figure 12

Initialization problems associated with in-circuit testing have been minimized with advanced ATE capabilities including homing loops and triggers. However, not providing a means to easily initialize a device may complicate the test development process. Devices requiring long initialization sequences may increase test times, and may even cause excessive backdrive times. In the case of a cluster functional test, long sequential chains may make test and diagnosis difficult [1]. Access to reset/clear lines should be provided in a design (figure 13).

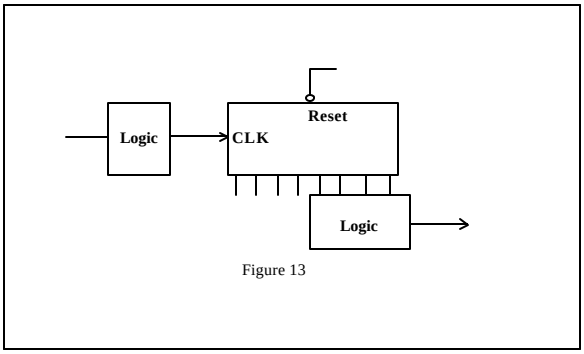


Figure 13

Design for Visibility and Controllability

Two approaches may be taken to provide full nodal access. Test points could be added to all nodes on the board. This assures full nodal access, but is not efficient. Many redundant access points may be added since *natural* access points (device pins, vias, connectors) may already exist. For dense boards, this extra *real estate* requirement may not be acceptable. The other method is to lay out the board and then determine what test points come naturally [2]. These natural access points are then supplemented with extra test pads. Some CAD systems or *third-party* software packages help automate the selection and definition of test pads.

A New Practical Testability Tool – Boundary-scan

In the past, a number of concepts to improve testability have been developed and partially implemented (e.g. LSSD and BILBO)[6]. However, none of these concepts have developed into a standard or have earned the attention that boundary-scan has received. Boundary-scan was conceived, evolved, and developed into a standard in a very short time. These efforts were initiated by the Joint

European Test Action Group, later the Joint Test Action Group (JTAG) and eventually evolved into the standard we have today; IEEE 1149.1-1990.

Boundary-scan solves a major testability problem that is more critical with complex devices. To find a simple manufacturing fault such as an open on a digital device, all device pins must be exercised. On a complex part this presents a major challenge. The function of the device must be thoroughly understood and then the test must be constructed and finally debugged. For complex LSI devices this may take weeks or months. Boundary-scan provides the ability to develop a test to exercise all device pins with a limited amount of effort, rendering these complex devices testable.

In order to support boundary-scan, circuitry must be added to the standard logic function of the device. As a minimum, this includes hardware called a Test Access Port to control the boundary-scan operation and *boundary cells* that are connected to the device pin drivers and receivers. Either 4 or 5 extra control pins must be added to the package to support the boundary-scan function. In the most basic test function, data is scanned into the device serially through a line called TDI (test data in), clocked around the boundary-scan cell chain, applied to the outputs; the results are sampled by the ATE (figure 14). Patterns are then applied to the inputs, captured by the input boundary cells, then clocked out the TDO (test data out) line; the results are sampled by the ATE. This is called the EXTEST function (external test). This verifies that the device input/output drivers are functional, the bond wires are intact, and the device is properly soldered to the board. The core logic has not been verified during this function. However, experience has shown that if a device passes this level of test, there is an extremely high probability the device will function. This was experienced by a manufacturer who was using boundary-scan equipped 68040 microprocessors. No additional processor fallout occurred at later process steps after invoking the simple EXTEST test function.

An optional test method may be incorporated in boundary-scan parts to test the core logic function. These two functions are called RUNBIST and INTEST. When a RUNBIST instruction is activated in a boundary-scan part,

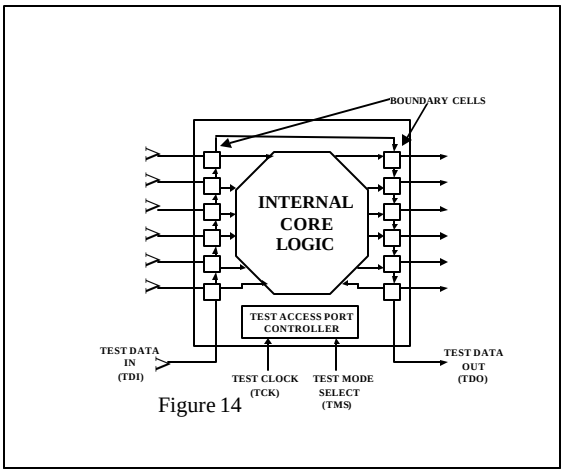


Figure 14

an internal self-test is performed and after a prescribed number of clock cycles, the results are scanned out TDO for verification; INTEST provides the means to shift *static* test patterns into the device through the boundary-scan chain, apply to the core logic, and shift out the resultant patterns through TDO for analysis by ATE.

Additionally, boundary-scan has the potential to address *genuine* node access testability problems. This may be mandated for technologies such as multi-chip modules. Boundary-scan components may be connected in a chain with only edge connector node access to the boundary-scan components (figure 15). Patterns are scanned in serially (TDI) and applied in parallel to the internal nodes through the output pins. These patterns are then captured from the inputs of the connecting boundary-scan devices and scanned out serially (TDO). Connections internal to the board become controllable or visible through the boundary-scan chain. During this *interconnect* test, power is applied to the board. It is imperative that the ATE can provide these patterns, quickly determine whether any shorts exist, and immediately power down the board to avoid damage when a short is detected. If the manufacturing process for a product is immature (high shorts fault spectrum), this *functional* test approach should not be used.

Some advanced ATE systems provide the means to test conventional logic (non-boundary-scan parts) connected through the boundary-scan chain with no node access (figure 15). In this scenario, patterns are scanned in serially through the appropriate boundary-scan device and applied in parallel to the conventional device. The output states are captured by other

boundary-scan devices, and scanned out serially and verified by the ATE. Accessible pins on conventional logic can be stimulated or measured using traditional methods. Two caveats must be understood. Complex, dynamic parts cannot be tested at a high clock rate. The effective parallel pattern application rate is relatively low since the patterns must be scanned in serially. Also, complex timing cannot be emulated. The other caveat is that faults can be masked. Consider the fact that if the nand gate in this example has a bridge fault across both inputs, the circuit functions properly (premise: logic "0" is stronger than a logic "1"). However, the long term reliability of the upstream part may be diminished.

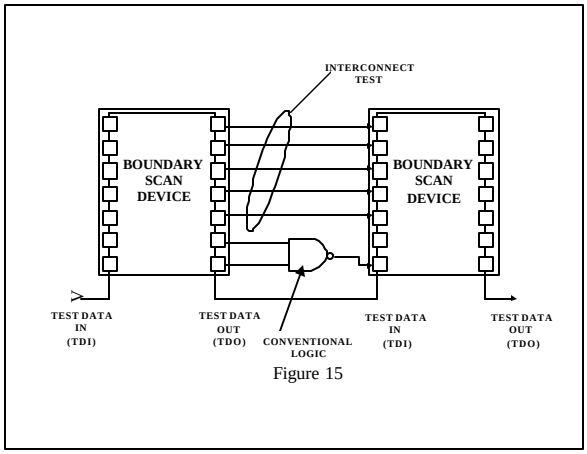


Figure 15

In addition to the identified limitations of boundary-scan, the test of the existence or functionality of active and passive analog parts cannot be addressed with current boundary-scan techniques (e.g. pull-up on boundary-scan *internal* node). However, there are also some inherent improvements to test and failure diagnosis with the approach. Most test methodologies have difficulty in accurately resolving that a trace is *open*, or a device solder connection is faulty. The diagnostic may only identify a device or node as being faulty. Implemented properly, boundary-scan offers the potential to correctly identify the real problem as an open. Optionally, some boundary-scan components contain an ID (identification) register that can be read to determine the device type. For example, if an LS part with the same logic function is improperly inserted in a board requiring an AS part, this could be detected by reading the ID register. Since the part has a similar logic function, traditional test techniques may not detect the problem and the circuit may marginally operate.

A Testability Tool Also Imposes Its Own Testability Constraints

Boundary-scan can be a viable tool to make complex devices testable. However, when a boundary-scan test is performed on a device, it no longer functions in its normal operating mode. Care must be taken to ensure that while the device is being exercised in the boundary-scan mode or *returns* to its normal mode that board-level conflicts do not occur [3]. For example, device conflicts could occur if two or more device chip selects are enabled simultaneously, causing a potentially damaging bus conflict (figure 16). This situation will not occur during normal circuit operation, but when entering boundary-scan mode normal circuit operation is interrupted. Careful selection of patterns shifted during boundary-scan operations or circuit modifications to make the design insensitive to these anomalies may be required.

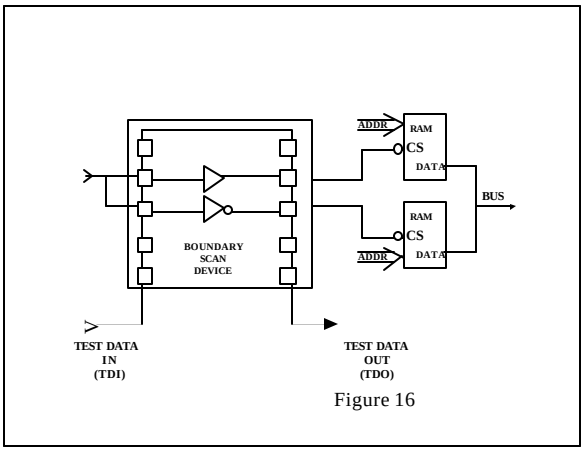


Figure 16

Providing full access to all device pins simplifies test development and allows accurate fault diagnosis. If node access is limited due to bonafide design requirements, care must be taken to make sure topological conflicts do not arise. For example, a means to disable a conventional device that shares a bus with a boundary-scan device must be provided. This not only means that the disable node needs to be accessible, but if driven by an *upstream* device it must be able to be backdriven for the relatively long time required to perform the serial boundary-scan test function.

If node access is limited and numerous boundary-scan devices are present in the board design, false consideration may be given to separate the board into multiple scan chains. In

general it simplifies test development and diagnosis if all devices are strung together in one chain. All devices are driven by a common TMS line and a common TCK line while TDO drives TDI of each successive device throughout the chain. It might be concluded if boundary-scan devices are connected in two or more chains that the chains could be loaded in parallel and throughput would be improved. However, the actual application of the pattern set is eclipsed by the test overhead of downloading the patterns to the ATE pin electronics and managing the test function. In addition, current ATE tools may not easily accommodate multiple scan chains. One final note concerning access is that providing access to all *internal* TDO and TDI lines will offer added visibility and control, aiding test diagnosis and test generation.

Fault Coverage and Test Stability

Once testability guidelines have become a standard part of the design/manufacturing process, a procedure should be in place to verify that all device tests are stable and all pins have been exercised. Histogram reports provide a means to verify analog test stability. For digital devices, it is important to verify that all pin faults are found. Fault simulation may provide this confidence for all *properly* modeled parts, but a process to determine pin coverage should be used on a *real* device or cluster on an *actual* board. Each test should be run while every input pin is successively stuck-at "1", stuck-at "0", and every pin is disconnected from the ATE. Any device tests that *do not* fail are suspect and should be evaluated and tests added. Through experience it has been found that if all pins are exercised and tested, extremely high yields will result. This process can only be realistically implemented if the ATE provides a tool to *automatically* and *safely* perform this process.

To ensure test stability, nominal drive/receive levels can also be *margined*. For example, if drive levels are set to 3.5 volts and .2 volts and receive levels are set to 2 volts and .8 volts, then drive and receive levels can be varied slightly (e.g. 10% of difference between high and low levels) while running the test to ensure stability. Driver levels would be shrunk to 3.17 volts and .53 volts and receiver thresholds expanded to 2.12 volts and .68 volts. This will help eliminate intermittent tests and avoid the *no-fault-found* syndrome experienced by many test processes, where good boards fail. Slight dut-to-dut load variations and fixture contact impedances will now have a negligible effect. Making a circuit testable, verifying all pins are tested, and eliminating intermittent tests will significantly reduce recurring re-work costs.

Yield Enhancement Through Board-Level Built-In Self-Test

Costs may be reduced by merging some test process steps. Some board level tests performed at product test may be done through a bed-of-nails fixture. Some high performance short wire fixtures may offer low parasitics and allow high speed testing or a *self-test* to be performed through a full bed-of-nails fixture. The most common example is a ROM based self-test resident on a processor board. Two-stage fixturing has been an alternative when proper board operation is sensitive to parasitics. Now with the advent of the new *shuttle-plate* fixture designs, a simpler, more reliable, less expensive two-stage operation is available. These fixtures operate by shifting in a shuttle-plate carrying probe plate stops, allowing the top plate to stop at different heights. The fixture is built with probes of different heights, only the taller probes make contact when the shuttle-plate is energized (typically with a solenoid or motor). Access is made only to points necessary to perform the self-test.

A means should be provided to communicate with the board and control the operation of the self-test. Rather than design a special test bus into the board, it is advantageous to use an existing board I/O port. It is common to perform this function through an available serial I/O line versus a parallel interface since less access is required. A serial RS-232 line may be controlled through a spare ATE system's terminal port rather than a traditional ATE driver/receiver, simplifying this control function. If possible, the self-test should be partitioned so that selected board regions/functions are tested separately, providing some level of device or circuit diagnostics. Providing a handshake with the self-test through an I/O line will allow the ATE to control the flow of the self-test and provide an indication of where a failure occurs. If I/O ports are not available, a communication channel between the ATE and DUT through its RAM memory or special latches may be implemented. Product-resident ROM-based

diagnostics may be used, or if a means is mandated in the design, a special fixture-resident diagnostic ROM may be switched in at the appropriate time. Access to busses (address and data) and control points must be provided to implement the fixture-resident ROM scheme [8].

Testability of a board may be increased if the board is designed with built-in self-test and the function of the target ATE is considered (e.g. ROM deselection, test control through I/O or memory interface, and fixturing scheme). One other aspect to consider is the operation of the board's I/O devices. Board I/O devices that are asynchronous and allow data to be latched can easily be tested using most ATE. Complex peripheral circuits may be difficult to test using a built-in self-test, since synchronization to the ATE may be difficult. Self-test implementation may be more straightforward if these device outputs can be looped back to other inputs and tested in this manner by the built-in self-test.

Summary

The practice of testability is continually evolving. Technology advances have fostered new requirements and have obsoleted others. ATE can perform complex test functions. The test process must now accommodate PLDs, ASICs, LCAs, and complex mixed-signal circuits. The test process may also be required to accommodate non-traditional tasks such as programming EEPROMs. New logic families like AS, FAST, ACT, FCT, carry their own testability requirements. Also, new ATE fixturing schemes offer the flexibility to consolidate some process steps. New testability tools such as boundary-scan never existed before. Boundary-scan solves some major testability problems, but incorporation of boundary-scan devices into a design imposes some new testability considerations.

The discipline of test engineers is still required to review designs. Some ATE includes software tools that help to uncover testability problems. Ignoring testability requirements will ultimately increase product costs. Not only will subsequent manufacturing processes be affected, but who wants to placate angry customers when a product fails due to a component that the test process failed to catch? Adding test points may not impact performance or require significant real-estate. For those circuits that are truly critical, at least some control and observation points can be added. Not all paths are critical.

Organizations change, products change, technology changes, ATE changes. A constant vigilance must be exercised to ensure that design-for-testability guidelines are followed.

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