How to anticipate Signal Integrity Issues: Improve my Channel Simulation by using Electromagnetic based model
HSD Strategic Intent

Provide the industry’s premier HSD EDA software.

- **Integration of premier simulation technologies** for microwave effects (which are inherent in the multigigabit/s regime), tuned to the needs of high speed digital designers.

**IC Model Builder:**
SystemVue

**HSD Designer:**
ADS/EMPro

**Physical Designer:**
Constraint-based tool e.g. Allegro, Expedition, CR-5000 etc.
Analyze complete serial links by co-simulating individual components, each at its most appropriate level of abstraction: link, circuit, or physical level.
Outline

- Pre-Layout “Getting to know the Channel”
  EM for Component Modeling
  - Extraction of High Frequency PCB Material Properties
  - Accurate Time skew
  - Connector footprint and Via modeling

- Post-Layout “Avoiding costly Re-Spins”
  Full-Path EM Simulations
  - Thales Testcase
    High Density 4000 HD Connections
  - Agilent Example
    HSD board along with SATA and USB connectors

- Conclusion
HSD Design Flow – “Getting to Know the Channel”

CHECKLIST

- Design Topology Exploration
- Component Selection
- Tx and Rx Model Validation
- Optimized Design Constraints

Engineer the topology and simulate the design constraints!
Agilent EM Simulation Portfolio

**ADS**
- Parameterized 3D EM Components
- ADS Layout Export

**EMPro**
- Parameterized 3D EM Components

**Momentum Simulator**
- Method of Moments
- Planar Simplifications

**FEM Simulator**
- Finite Element Method
- 3D Accuracy

**FDTD Simulator**
- Finite Difference Time Domain
- Time Domain Excitation
Pre-Layout Co-Simulation with EM Simulators

Channel co-simulation with PCB EM model including crosstalk and 8B10B encoding

With 8B10B Coding

EM Model

Integrate layout artwork into schematic

3D-EMPro Connector Model

Generation of Design Constraints

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver (Tx) Speed</td>
<td>Fast</td>
<td>Typical</td>
<td>Slow</td>
</tr>
<tr>
<td>Trace Impedance</td>
<td>45 ohms</td>
<td>50 ohms</td>
<td>55 ohms</td>
</tr>
<tr>
<td>Trace Width</td>
<td>4 MIL</td>
<td>8 MIL</td>
<td></td>
</tr>
<tr>
<td>Trace Length</td>
<td>8000 MIL</td>
<td>12000 MILL</td>
<td></td>
</tr>
<tr>
<td>Trace Spacing</td>
<td>5 MIL</td>
<td>10 MIL</td>
<td></td>
</tr>
<tr>
<td>Max Uncoupled Length</td>
<td>100 MIL</td>
<td>10000 MIL</td>
<td></td>
</tr>
<tr>
<td>Routing Layer (Layer Set)</td>
<td>TOP</td>
<td>Inner Layers</td>
<td></td>
</tr>
<tr>
<td>Crosstalk Rule (Diff pair to other trace)</td>
<td>8 MIL</td>
<td>16 MIL</td>
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<tr>
<td>Allowable Phase Mismatch</td>
<td></td>
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<tr>
<td>Allowable Via Usage (Back drilling)</td>
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<tr>
<td>Stack-up consideration (optional)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tx De-emphasis settings (optional)</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Rx DFE settings (optional)</td>
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</table>
Constraint Examples for Impedance Mismatch

**Stub Resonance**
50 Ohm Stub Length from 1 mm to 10 mm

- 5 GB/s, PRBS 7
- 1 mm Stub
- 10 mm Stub

**Series Resonance**
25 Ohm Discontinuity with Length 1 mm to 25 mm

- 5 GB/s, PRBS 7
- 1 mm Mismatch
- 25 mm Mismatch

Signal Loss S21

freq, GHz

[dB(S21)]

- -10
- -9
- -8
- -7
- -6
- -5
- -4
- -3
- -2
- -1
- 0

freq, GHz
HSD Design Flow – “Getting to Know the Channel”

Benefits in using 3DEM in Pre-Layout

- Extraction of High Frequency PCB Material Properties
- Accurate Time skew
- Connector footprint and Via modeling

Capturing the physics of components in the channel
Measurement Based Verification of EM Simulation

**Simple Series Resonant Change in Impedance**

EM Simulations are only as accurate as the PCB specifications.

**EM Simulation Fails to Match Measurement**

Frequency Domain

Time Domain
PCB Frequency Dependent Losses can be separated into **Conductor** and **Dielectric** Losses

\[ \alpha_{dB} = \alpha_{cond} + \alpha_{diel} \]

Stripline Conductor Losses require more then 1 line width to determine **dielectric height** and **trace width**.

\[ \alpha_{cond} = \frac{36}{wZ_0} \sqrt{f} \quad Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln \left( \frac{2b + t}{0.8w + t} \right) \]

Stripline Dielectric Losses only require 1 line length to determine **dielectric loss** and **electrical delay**.

\[ \alpha_{diel} = \frac{\pi}{c_o} f \tan \delta \sqrt{\varepsilon_r} \]

- \( Z_0 \), characteristic impedance (Ohm)
- \( b \), the dielectric height between reference planes (mil)
- \( t \), copper thickness of the PCB trace (mil)
- \( w \), trace width (mil)
- \( \varepsilon_r \), dielectric constant
- \( c_o \), is the speed of light in vacuum
- \( \tan \delta \), loss tangent
Typical Method for Measured PCB Material Properties

Two PCB Test Structures with Different Line Lengths

- Excellent for determining T-Line loss and delay characteristics
- Does not provide information on as-built trace width and dK height.

**SYMMETRICAL 2x FIXTURE THROUGH PATH**

**FIXTURE A S-PARAMETERS**

**FIXTURE B S-PARAMETERS**

**Step 1**
Splitting of the S-Parameters

**Agilent PLTS AFR Algorithm**

**Step 2**
Fixure Removed Transmission Line Length L

**T-LINE LENGTH MATERIAL PROPERTIES**

**Fixure Removed Transmission Line Length L**

**T-Matrix**
Additional PCB Resonant Beatty Structure

- **Beatty Style Series Resonant Change in Impedance Test Structure**
  - Enables estimation of as-fabricated $dK$ height and trace width.
  - Only requires one additional test structure on the PCB.
  - Simple layout construction.

**FIXTURE + Resonant Beatty Structure**

- **Step 3**
  - **FIXTURE DE-EMBED**
  - **T-Line Change in Z Fabrication Properties**
    - Series Resonant Beatty Structure
    - $W \ x \ 3W \ x \ W$
    - ~2.54 cm (1 in)

**S-Parameters before Fixture De-Embed**

**Measured S-Parameters after Fixture De-Embed**

![Graphs showing frequency response](image)
Enables Estimate of Trace Width and DK Height

Series Resonant Beatty Structure

W 3*W  W

~2.54 cm (1 in)

As-Fabricated Material Properties

- Dielectric Constant
- Loss Tangent
- Dielectric Height
- Trace Width
- Etching Tolerance
- Trace thickness
- Copper Trace Conductivity

Tune Model Variables to Match Measurement

<table>
<thead>
<tr>
<th>Var Eqn</th>
<th>VAR6</th>
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<tbody>
<tr>
<td>Er</td>
<td>3.22 {t}</td>
</tr>
<tr>
<td>b</td>
<td>7.9 {t}</td>
</tr>
<tr>
<td>W</td>
<td>9.4 {t}</td>
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<td>W_tol</td>
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<tr>
<td>TanD</td>
<td>0.0058328 {t}</td>
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<tr>
<td>t</td>
<td>0.6</td>
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<tr>
<td>sigma</td>
<td>42936000 {t}</td>
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</tbody>
</table>
2-Step Process: Fast Tuning with 2D-Planar Model then Fine Tune with EM Simulator

Fast Tune 2D-Planar Model Parameters to Match Measured Data

Fast Tuning: Parameter Matching

2-D Planar EM Solver Model for fast tuning and optimizing of dielectric height and trace width to match measurements.

* Simple T-Line model without the complexity of fixture connections.
Matching Measured Data – Time and Frequency

Transmission Line Through Segment

Series Resonant Beatty Structure

Insertion Loss (dB)

freq, GHz

Measurement Based Simulation
(Causal $\varepsilon'$r and $\tan \delta$)

Unwrapped Phase (Degree)

freq, GHz

Measurement Based Simulation
(Causal $\varepsilon'$r Model)

Impedance

time, nsec

3D-EM Simulation
(Same Transmission Line Settings from 2-D Planar Models)

2D-Planar Model
Optimized to Measured Data

Measured
Fine Tune EM Model Parameters to Match Measured Data

Parameters for Tuning

- Dielectric Constant
- Dielectric Height
- Trace Width
- Etching Tolerance
- Loss Tangent
- Copper Trace Conductivity
HSD Design Flow – “Getting to Know the Channel”

Benefits in using 3DEM in Pre-Layout

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Capturing the physics of components in the channel
DDR4 PCB Layout Design Rules

- Routing Impedance
- Trace Width and Spacing
- Material stack-up
- BGA Trace Necking
- Via Transitions
- Reference Plane Transitions
- PDN Impedance
- Skew Routing Compensation

Losses, Crosstalk, and EMI

DDR DQ Byte Lane Model for Design Exploration

Model Variables Available for Tuning, Optimizing, and Design of Experiments
DDR Skew Compensation with Serpentine Routing

Source Synchronous Clocking of DQ Byte Lanes Requires Matched Channel Lengths
Squeezing a Transmission Line While Maintaining its Length

ADS Layout allows to modify an existing transmission line to squeeze it into a smaller space, specifying several characteristics in the process, such as corner type, lead length and minimum spacing.
Electrical Length not Physical Length for DDR4

**PHYSICAL LENGTH MATCHING**
- Start: *Edges Aligned*
- 33 mm Matched Length
- End: *Edges are Skewed 12pS*

**ELECTRICAL LENGTH MATCHING**
- Edges Aligned, No Skew
- 2 mm Length Difference
- 31 mm
- 33 mm
- Electrical Skew = 12 pS
- 0 pS Skew

Minimum Bends “Switchback” Routing

Maximum Bends “Serpentine” Routing
Limited PCB Routing Space – Maximizing Density

Serpentine with minimum layout width requires significantly more length for skew matching as compared to switchback routing.

Switchback routing results in less skew when utilizing Physical Lengths in a PCB CAD tool for length matching.
HSD Design Flow – “Getting to Know the Channel”

Benefits in using 3DEM in Pre-Layout

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**Capturing the physics of components in the channel**
One commonly overlooked source of channel discontinuity is the signal via. Vias can add jitter and reduce eye openings that can cause data misinterpretation by the receiver.

3DEM simulation can be used to evaluate / optimize:

- Impedance signatures
- Insertion / Return losses
- GND Return Vias
- Pads and Anti-Pads
- Via stubs
- Backdrilling
- PCB Stackup
Evaluate S-parameter profiles for a standard SMA footprint using PTH for 2 different cases:

- ETCH_TOP to ETCH_INT3 (long stub)
- ETCH_TOP to ETCH_INT10 (short stub)

Where:

- ETCH_INT4 and ETCH_INT9 are power planes
- ETCH_INT5 and ETCH_INT8 are GND planes

Simulate using MoM or FEM
Longer via stub lengths cause larger impedance discontinuity and present more loss to the signal path.

You can eliminate the via stub by routing only microstrip traces on the top and bottom layers of the board.

However, this might not be possible because of layout constraints, electromagnetic interference (EMI) related concerns, or other board design considerations with microstrip traces.

S-Parameter simulation results
Current visualization can help in identifying root causes of unexpected resonances.
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• Conclusion
HSD Design Flow – “Avoiding costly Re-Spins”

CHECKLIST

✓ Verify the layout before Fabrication
✓ Full 3D EM extraction for Accurate models
✓ Meet all the Requirements

Avoiding costly Re-Spins with full-path Electro-Magnetic simulation
Post-Layout ADFI for Importing PCB Designs

1. Layer Selection Tools and Fabrication Details
2. Intelligent Net Selection Cookie Cutting
3. EM Simulation
4. EM S-Parameter Model Co-Simulation
5. Q Signal Eye Diagrams
6. DDR Compliance Report
HSD Design Flow – “Avoiding costly Re-Spins”

Benefits in using 3DEM in Post-Layout

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Avoiding costly Re-Spins with full-path Electro-Magnetic simulation
Why this test case?

- Models not available, unusable routing, diff pair + single-ended coupling,

We must be able to detect the signal integrity problem using simulations.

- Differential pair MGH_DIA
  - Length: 190 mm
  - Width of the trace: w=130 \, \mu m
  - Spacing between P & N channels: s=150 \, \mu m
  - Embedded microstrip on layers 2 & 3

- Single-ended SSN_SIGA
  - Length: 160 mm
  - Width of the trace: w=130 \, \mu m
  - Embedded microstrip on layers 2 & 3
Presentation of the test case

Test case

- Spacing between MGH_DIA2_P and SSN_SIGA_79: 120 µm (< s)
- MGH_DIA2_P between 2 power planes (VCCH et VCCINT)
**S Parameters extraction with Agilent’s Momentum**

**Settings:**
- Bandwidth range: DC – 10 GHz
S Parameters extraction with Agilent’s Momentum

Coupling between MGH_DIA2_P and SSN_SIGA_79

Momentum gives better eye diagram compared to measurement than hybrid solvers. Hybrid solvers are not able to correctly take into account this topology.
IBIS AMI models are used for the Tx, Rx and aggressors. IBIS AMI models for Stratix chips are available from Altera. ADS also has built-in non-AMI models if the IC vendor is not ready 😊 10^6 bits were simulated in this case.
Comparison simulations vs measurements

- **MGH_DIA2** without single-ended aggressor (MGH_DIA1 active)
  - Data rate: 1 Gbps
  - Pattern: PRBS7
  - VOD: 800 mV

Jitter Separation processed with Agilent’s Infiniiview

<table>
<thead>
<tr>
<th>Jitter</th>
<th>Measurement</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>TJ (BER-12)</td>
<td>375 ps</td>
<td>333 ps</td>
</tr>
<tr>
<td>RJrms</td>
<td>24 ps</td>
<td>20 ps</td>
</tr>
<tr>
<td>DJpp</td>
<td>41 ps</td>
<td>50 ps</td>
</tr>
<tr>
<td>PJrms</td>
<td>5 ps</td>
<td>1 ps</td>
</tr>
<tr>
<td>DDJpp</td>
<td>31 ps</td>
<td>41 ps</td>
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<tr>
<td>ISIpp</td>
<td>27 ps</td>
<td>40 ps</td>
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<tr>
<td>BUJpp</td>
<td>34 ps</td>
<td>40 ps</td>
</tr>
<tr>
<td>DCD</td>
<td>5 ps</td>
<td>0 ps</td>
</tr>
</tbody>
</table>

RJ is abnormally high -> the setting of the SERDES clock is wrong

Despite the inability of simulating the PJ, the correlation is quite good.
HSD Design Flow – “Avoiding costly Re-Spins”

Benefits in using 3DEM in Post-Layout

- Thales Testcase
  High Density 4000 HD Connections

- Agilent Example
  HSD board along with SATA and USB connectors

Avoiding costly Re-Spins with full-path Electro-Magnetic simulation
In such applications, the main cause of impedance discontinuities and crosstalk is the area where the connector is attached to the RF board differential traces, so without taking complete integrated system into SI consideration, it is difficult to get accurate answers and error-free solution.
HSD board along with SATA and USB connectors
EM simulation using Finite Element Method solver

Samtec works with users to provide connector models for use in the following well-known EDA tools:
• Advanced Design System (ADS) from Agilent
HSD board along with SATA and USB connectors
Post Layout Analysis of complete system

Channel Simulation in ADS with a single transmitter and no aggressors.

Enable the DFE in the "Rx_Diff" to get the better Eye Opening

Differential Trace: The Bit Rate is taken as = 1 Gbps
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• Conclusion
High density complex designs with analog, digital, and an array of power supplies lead to complex electromagnetic interactions that are best evaluated by full EM simulation.

High volume low cost resulting in highly perforated power and ground planes with non-ideal return currents rely on EM simulators to predict the true interactions in the multi-gigabit domain.

Questions