Demystifying Vias in High-Speed PCB Design

Keysight HSD Seminar
Mastering SI & PI Design

dB(S21)
What is Via?

Vertical Interconnect Access (VIA)

– An electrical connection between layers to pass a signal from one layer to the other

– Single layer designs do not require vias. Vias are only for multi-layer PCBs or packages to route signals

– Why do we really care about vias?
  • Vias produce discontinuity from the signal transition and significantly affect signal and power integrity in high speed designs
  • Parasitic capacitance of via can increase signal rise time, making the signal speed slower
  • Designers should maintain a good impedance transition

Reference: https://en.wikipedia.org/wiki/Via_(electronics)
Via Effect to High Speed Channels

3 inch microstrip + 3 inch stripline

Just channel @ 10Gbps
Via Effect to High Speed Channels
3 inch microstrip + 3 inch stripline
Via Effect to High Speed Channels
3 inch microstrip + 3 inch stripline

- Just channel @ 10Gbps
- Via inserted between @ 10Gbps
- Via Stub Removed @ 10Gbps

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Via Effect to High Speed Channels
3 inch microstrip + 3 inch stripline

- Just channel @ 10Gbps
- Via inserted between @ 10Gbps
- Via Stub Removed @ 10Gbps
- Via Stub Resonance @ Nyquist Freq

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Types of Via
PTH, Blind, Buried, and μ-vias

– By physical implementation…
  • PTH (Plated Through Hole) via
  • Blind via
  • Buried via
  • μ-via (laser via), via-in-pad

– By signaling…
  • Single-ended via
  • Differential via
  • Signal via
  • Ground via
Anatomy of Via

Via pads, anti-pads, barrel, NFP…

– Via barrel
  • Conductive tube filling the drilled hole

– Via pads
  • Connects each end of the barrel to the component, plane, or trace

– Via anti-pads (or clearance)
  • Clearance hole between barrel and metal layer to which it is not connected

– Non-functional via pads
  • Internal or external pads that are not connected to any traces or components

Reference: https://en.wikipedia.org/wiki/Via_(electronics)
Return Current Path for Vias

- The return current must find a path to return to the source.
- At high frequencies, return currents will favor the path(s) of least impedance.
- Due to the skin effect, the current flows along the metal surface, not penetrating through.
- The closer the ground via to the signal via, the smaller the inductance of via is.

Graphic Source: "High-Speed Signal Propagation", Fig. 5.33, p. 353
Electrical Model for Vias

– No simple via model for multi-gigabit signals or higher frequencies
  • Lumped or distributed…
– Is the via inductive, capacitive or something else?
  • For example, can we say that the impedances of three cases below are the same?

• The answer is “it depends”
  - The return path affects the impedance characteristic of via
Via Impedance By Various Return Path
Simple single ended via w/o pads case

- Test structure
  - Substrate thickness = 100 mil
  - Substrate material = FR-4
  - 6 metal layers
  - Via barrel radius = 5 mil
  - No via pads

- Tested for:
  - Various sizes of via anti-pads
  - Various number of ground vias
Via Impedance By Various Return Path
Magnitude of Z11

Blue: 2 ground vias, 100 mil via anti-pad
Green: 2 ground vias, 50 mil via anti-pad
Red: 2 ground vias, 25 mil via anti-pad
Black: 8 ground vias, 25mil via anti-pad
Pink: 8 ground vias, 12.5mil via anti-pad

It depends!!!
TDR(t) or Impedance, Z(f)

- TDR (Time Domain Reflectometry)
  - Plots impedance vs. time or distance
  - The minimum resolution depends on the rise time of step signal or signal bandwidth
    \[ L_{\text{min}} = \frac{T_R \cdot C_0}{2 \cdot \sqrt{\varepsilon_R}} \]
    , \( \text{BW} = \frac{0.35}{T_R} \)
    
    - Example: \( T_R = 10 \text{ps}, \varepsilon_R = 4 \Rightarrow L_{\text{min}} = 0.75\text{mm} \text{ or } 29.53\text{mil} \)
      
    - Therefore, it is challenging to use TDR for the via itself since the feature size of via is typically very small

- Impedance, Z
  - Plots impedance vs. frequency
  - Shows frequency dependent impedance characteristic
Via Impedance By Various Return Path

Magnitude of Z11

- **Inductive:** Larger loop area or longer ground return
- **Capacitive:** Closer ground return
- **Matched:**
  - Larger via anti-pad → Increased inductance
  - Smaller via anti-pad → Increased capacitance
  - More ground vias → Reduced inductance
Another View of Vias
As a Coaxial Transmission Line

- In coaxial transmission lines, the electric and magnetic fields are transverse to the direction of propagation, which makes TEM wave propagation.

  • Capacitance per unit length
    \[ C = \frac{2\pi \varepsilon}{\ln \left( \frac{b}{a} \right)} \text{[F/m]} \]
  
  • Inductance per unit length
    \[ L = \frac{\mu_0}{2\pi} \ln \left( \frac{b}{a} \right) \text{[H/m]} \]
  
  • Characteristic Impedance
    \[ Z_0 = \sqrt{\frac{L}{C}} = \frac{1}{2\pi} \sqrt{\frac{\mu_0}{\varepsilon}} \ln \left( \frac{b}{a} \right) \]
  
  • Phase constant
    \[ \beta = \omega \sqrt{LC} = \omega \sqrt{\mu_0 \varepsilon} \]
  
  • Propagation Velocity
    \[ v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{\mu_0 \varepsilon}} = c \frac{1}{\sqrt{\varepsilon}} \]

Example:
- a = 5 mil
- b = 25 mil
- \( \varepsilon = 4.6 \)
  - \( C = 159 \text{ pF/m} \)
  - \( L = 321.89 \text{ nH/m} \)
  - \( Z = 45 \text{ ohm} \)
Via Pads
Capacitive or Inductive?

– Via pads, in general, add a capacitive characteristic to the impedance

– The larger the via pad size is, the lower the via impedance is, due to the increased capacitance

– By removing the non-functional via pads, the total capacitance can be decreased
Transmission Line Routing with Via
Microstrip input + Via + Microstrip output

- The impedance of the fullwave EM result (Blue) is not the same as the cascaded impedance (Red) of three sections, “Microstrip + via + Microstrip”

- This is due to the dangling tail edge of the microstrip transmission line close to the via, which adds inductance to the impedance
How Much of Inductance?

Estimating Microstrip to Via Transition

- The inductance value can be simply extracted by matching the impedance between fullwave and cascaded results with additional inductors
  - The estimated inductance for the transition is ~0.22nH in this case
- This inductance may be compensated by decreasing the via anti-pads or increasing via pads
Improving Impedance Match
With Smaller Via Anti-Pads

– Smaller radius for the via anti-pad could improve the impedance match performance by providing a little more capacitance.

– However, the impedance variation (profile) is complex behavior; so, many other possible approaches may be available - for instance, a larger via pad.
Via Stub

Stub Resonance

- A dangling via stub acts as an open stub resonator, similar to a series LC resonator
  
  • At a quarter wavelength, the impedance turns into a short impedance; therefore, the insertion loss at that frequency becomes the maximum

- Depending on the Q value, the loss at other frequencies can be significant as shown in the dB(S21) plot
Via Stub

Stub Resonance vs. Stub Length

- The resonance frequency varies with the length of the stub
- By making the stub length shorter (moving the strip layer down), the stub resonance frequency can be pushed up to a higher frequency

**dB(S21)**
Via Stub

Estimating Via Stub Resonance Frequency

– First order approximation formula

\[ F_{\text{resonance}} = \frac{1.18 \times 10^9}{4 \times \text{Stub Length} \times \sqrt{\varepsilon_R}} \text{ [stub length in inch unit]} \]

– Example: 93mil stub \( \rightarrow \) 14.79GHz

– Or, using ADS Open Stub Transmission Line model
Via Stub Back-Drilling

- The via stub resonance can be removed or pushed up to a higher frequency by back-drilling the via.

- The stub resonance at 15GHz with 3rd layer stripline case is completely removed by the back-drilling.

Graphic source: Courtesy of Sanmina-SCI
Via Stub

Stub Resonance Electric and Magnetic Field View

Electric Field @ 16.3GHz

Magnetic Field @ 16.3GHz
Differential Via

Differential Signaling

- Two single-ended vias used for differential signaling
- The minimum via pitch size is determined by the manufacturing specification
- The coupling (overlap of E, H field lines) changes the differential impedance, \( Z_{\text{diff}} = 2 \times (Z_0 - \Delta Z) \)
  - The larger the coupling (tight coupling) is, the lower the differential impedance is

![Graph showing the relationship between |Z11| and via pitch.](image)

- Bigger pitch
- Smaller pitch

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Differential Via Crosstalk

Tight coupling vs. Loose coupling

- Tight coupling uses less area, but with a little higher loss
- Tight coupling is better for crosstalk performance
- Tight coupling is less sensitive to common signal noise
Differential Via
Different Signaling Electric Field View

Differential Signaling Electric Field @ 40GHz

Common Signaling Electric Field @ 40GHz
Summary

– It is preferable to design vias as coaxial transmission lines to maintain a good impedance match

– Via stubs act as a series LC resonator, adding significant loss to the channels, that can be minimized by back-drilling the via stubs

– Differential vias are used for differential signaling and tight coupling is more favored

– Tools for modeling vias:
  
  • ADS: Design environment for high speed PCB analysis
    - Transient/Convolution & S-parameter circuit simulators
    - FEM: Finite Element Method
    - Momentum: 3D Planar EM simulator
    - Via Designer: new utility in ADS 2017 (coming this summer)
  
  • EMPro: 3D modeling and EM simulation environment
    - FEM: Finite Element Method EM simulator
    - FDTD: Finite Difference Time Domain EM simulator
Thank you for attending! Questions? Want More Resources?

ADS Bundle Used for VIA design:

- **W2223BP ADS Core, TransConv, Channel, CILD, Layout, SIPro, PIPro Bundle**
- **W2404BP EMPro Core + FEM + FDTD + Compliance Bundle**

Signal Integrity & Power Integrity Resources

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