Powering Collaboration and Innovation in the Simulation Design Flow

Agilent EEsoph Design Forum 2010

Channel Simulator and AMI model support within ADS
Contributors to this Paper

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Special thanks to Chad Morgan, Tyco Electronics for providing measured and simulated data for STRADA Whisper and HM-Zd backplanes
Agenda

• Introduction to Channel Simulation
• Brief introduction to IBIS AMI Model
• AMI model simulation in ADS2010
• AMI model Generation using System Vue
Introduction to Serial Link

- Behavioral models
- Transistor level models
- IBIS AMI

Passive Interconnect

- Behavioral models
- Transistor level models
- IBIS AMI

Received Signal
## Comparison of Simulation Techniques in ADS 2009

<table>
<thead>
<tr>
<th>Method</th>
<th>Transient Simulator</th>
<th>Channel Simulator: Bit-by-bit mode</th>
<th>Channel Simulator: Statistical mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Method</td>
<td>Modified nodal analysis of Kirchoff’s current laws for every time step</td>
<td>Bit-by-bit superposition of step responses</td>
<td>Statistical calculations based on step response</td>
</tr>
<tr>
<td>Applicability</td>
<td>Linear and non-linear circuits</td>
<td>LTI, any specific bit pattern, adaptive eq. taps, IBIS AMI</td>
<td>LTI, fixed (general) bit pattern, fixed eq. taps</td>
</tr>
<tr>
<td>BER floor in one minute simulation</td>
<td>~10^{-3}</td>
<td>~10^{-6}</td>
<td>Arbitrarily low</td>
</tr>
</tbody>
</table>
Channel Simulator Methodology

Step response is calculated

Bit by bit mode: Superposition of bits

Statistical mode: Statistical techniques
Channel Simulator: Bit-by-bit and Statistical Modes

Integrate layout artwork into schematic

Agilent Technologies
STRADA Whisper 11.5” System (w/ Cables)
Verification of Simulated data

Short, High-Quality Channel

- Eyes measured with Scope
- S-parameters measured and run in fast statistical simulators

![Graph showing Differential Insertion Loss (Blue) & Return Loss (Red)]

<table>
<thead>
<tr>
<th>6.25 Gbps PRBS $2^{31}$ $10^{-15}$ Contour</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scope</strong></td>
</tr>
<tr>
<td>Error Threshold 5</td>
</tr>
<tr>
<td>Height: 33%</td>
</tr>
<tr>
<td>Width: 63%</td>
</tr>
<tr>
<td><img src="contour.jpg" alt="Image of 6.25 Gbps Contour" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>12.5 Gbps PRBS $2^{31}$ $10^{-15}$ Contour</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scope</strong></td>
</tr>
<tr>
<td>Height: Closed</td>
</tr>
<tr>
<td>Width: Closed</td>
</tr>
<tr>
<td><img src="contour.jpg" alt="Image of 12.5 Gbps Contour" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ADS Overlay (Red Contour)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Height</strong>: 40%</td>
</tr>
<tr>
<td><strong>Width</strong>: 74%</td>
</tr>
<tr>
<td><img src="overlay.jpg" alt="Image of ADS Overlay" /></td>
</tr>
</tbody>
</table>

| **Height**: 6%                             |
| **Width**: 28%                             |
| ![Image of ADS Overlay](overlay.jpg)       |
STRADA Whisper 27” System (w/ Cables)

Verification of Simulated data

Long, High-Quality Channel

• Eyes measured with Scope
• S-parameters measured and run in fast statistical simulators

![Graph showing Differential Insertion Loss and Return Loss](Image)

<table>
<thead>
<tr>
<th>Scope</th>
<th>ADS Overlay (Red Contour)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.125 Gbps PRBS 2^{31} 10^{-15} Contour</td>
<td>Height: 37% Width: 66%</td>
</tr>
<tr>
<td>6.25 Gbps PRBS 2^{31} 10^{-15} Contour</td>
<td>Height: 4% Width: 21%</td>
</tr>
<tr>
<td></td>
<td>Height: 42% Width: 76%</td>
</tr>
<tr>
<td></td>
<td>Height: 4% Width: 7%</td>
</tr>
</tbody>
</table>

STRADA Whisper 27” System (w/ Cables)
Crosstalk Validation: Synchronous Noise

Verification of Simulated data

HM-Zd 10” System ‘In-Row’ Near- and Far-End Crosstalk

- Highest magnitude crosstalk in available systems
- 6.25 Gbps, PRBS $2^{31}$, no EQ, & no induced jitter

![Measured NEXT](image1)

![ADS NEXT](image2)

![ADS Overlaid on Test Data](image3)

![Measured FEXT](image4)

![ADS FEXT](image5)

![ADS Overlaid on Test Data](image6)
Crosstalk Validation: Asynchronous Noise
Verification of Simulated data

HM-Zd 10” System ‘In-Row’ Near- and Far-End Crosstalk

• Highest magnitude crosstalk in available systems
• 6.25 Gbps, PRBS $2^{31}$, no EQ, & no induced jitter
STRADA Whisper 11.5” System (w/ Cables)

Verification of Simulated data

Short, High-Quality Channel

- ADS (statistical mode) optimize 3 FFE taps automatically
- Sim taps used with Oscilloscope

Verification of Simulated data

6.25 Gbps
PRBS $2^{31}$
$10^{-15}$ Contour
t(0) = +0.825
  t(1) = -0.145
  t(2) = -0.030

12.5 Gbps
PRBS $2^{31}$
$10^{-15}$ Contour
  t(0) = +0.762
  t(1) = -0.202
  t(2) = -0.036
STRADA Whisper 27” System (w/ Cables)

Verification of Simulated data

Long, High-Quality Channel

• ADS (statistical mode) optimize FFE taps automatically
• Sim taps applied to Scope

Verification of Simulated data

<table>
<thead>
<tr>
<th>3.125 Gbps</th>
<th>6.25 Gbps</th>
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<tbody>
<tr>
<td>PRBS 2^{31}</td>
<td>PRBS 2^{31}</td>
</tr>
<tr>
<td>10^{-15} Contour</td>
<td>10^{-15} Contour</td>
</tr>
<tr>
<td>t(0) = +0.810</td>
<td>t(0) = +0.745</td>
</tr>
<tr>
<td>t(1) = -0.165</td>
<td>t(1) = -0.222</td>
</tr>
<tr>
<td>t(2) = -0.025</td>
<td>t(2) = -0.033</td>
</tr>
</tbody>
</table>

Scope

- Height: 41%
- Width: 79%

ADS Overlay (Red Contour)

- Height: 46%
- Width: 88%
Algorithmic Modeling Interface (AMI): Introduction and Ecosystem

- Customized IC models representing actual device behavior
- Compiled models protects vendor IP
- Portable and supported by EDA tools
- Two aspect
  - Model Generation (mostly semiconductor vendors)
  - Model Simulation (mostly system companies)
Introduction to Algorithmic Modeling Interface (AMI)

- System is simplified to three blocks: TX + channel + RX
- TX and RX models: regular IBIS model + AMI extension
- AMI extension: DSP blocks that model equalization (EQ) and CDR

- Assumption 1: linear time invariant (LTI) system
- Assumption 2: zero impedance at TX AMI output and infinite load at RX AMI input
- Simulation is reduced to TX DSP + channel impulse convolution + RX DSP
- Orders of magnitudes faster than transistor level SPICE simulation
Simulation Flow

Initialization

Channel impulse

TX Init

RX Init

Time domain simulation

AMI Models implement three interface functions:

- *Init*: takes channel impulse response as input, performs initialization, allocates memory, and returns modified impulse (optional).
- *GetWave*: takes input waveform and returns modified waveform. RX also returns clock times.
- *Close*: free memory.
AMI Model Files

Each model includes following files:

• DLL or/and shared object (so): three functions
  
  * `Init(char * params_in, ...)`
  * `GetWave(waveform_in, waveform_out, clock_tick_array)`
  * `Close()`

• .ami file: an ASCII file specifies model parameters input to `Init()`

• .ibis file: specifies file names of .ami and DLL and compilation platform
The file specifies:

- **Platform_Compiler_Bits**

- **DLL file name**

- **Parameter file name**
AMI Model Simulation within ADS

Supported in ADS2010

ChannelSim
ChannelSim1
EnforcePassivity=yes
Mode=Statistical

VAR
VAR1
Gain=1
tap1=0.5
tap2=-0.1
tap3=0

Eye_Probe
Eye_Probe1
The AMI Model Lifecycle... disconnected flows

AMI Modeling
Matlab, C/C++, Code Generation

SerDes Design
HDL, Verilog-A/AMS, Matlab, C/C++, Spice

AMI-Modeling adds significant engineering requirement for coding, without any major benefit for IC vendor

System Architect, IC Designer

Modeling Engineer

AMI Testing/Validation
Channel Simulators, Correlation with Spice & Measurements

Platform & Compiler Version dependencies, Correlation with Spice and Measurements

End Customer
Channel Simulators

SI/Application Engineer

System Design Engineer

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EEsof 2010
AMI Modeling supposes to speed-up System Design Cycle, BUT, Model-generation takes significant time & resources.

...System Vendors have to wait a long time before Vendor models become available.

0 months  AMI 101, Decipher Code  8 months  First-model to Customer
4 months  Early Model prototypes  12 months

Note: Vendors with NO experience in AMI modeling are spending 8-16+ months to come up with first-generation models.

Models come very late in Design Cycle → used only for Validation, NOT Design.
In-house AMI Model Development: Why and How?

Protect your SERDES IP with heart and Soul: Do not leave it loose

AMI model generation key requirements:
- Efficient Tops-down “Electronic-System-Level” Design Methodology
- Basic (customizable) system algorithmic building blocks representing SERDES
- Integration with HSPICE based data
- Efficient simulation and validation of system Performance before model creating
- Automatic and efficient C++ Code-generation along .dll compilation
- Auto .ami file generation

ESL Design Flow with Automatic AMI model-generation
Introduction to “System Vue” (ESL) and AMI Model Generation Design Flow
**Step-1:** Starting Architecture Design with Generic Model

Different blocks represent high-level TX architecture.
More on FIR Filter...
How to bring in Spice or Measured data?

**Challenges:**
1. Typical Simulation and Measured Data is not equally time-stepped

   Sampling Rate determines Simulation Accuracy

   **FIR model should support “Arbitrary” Sampling Rate**
SERDES and Channel Modeling using System Vue

- TX De-emphasis
- TX Jitter
- RX Equalization (CTLE+DFE)

6.25 GHz SerDes

FlexDCA
1A Transmitted Signal
1B Received Signal after Channel
2A Received Signal after CTLE
2B Received Signal after CTLE & DFE
6.25 Gbps Channel : Eye Diagram Verification

Integrated Flex DCA software
6.25 Gbps Channel : Eye Diagram @ Various Probe Points

Eye Diagram @ TX O/P

Eye Diagram @ Channel O/P

Eye Diagram @ After CTLE

Eye Diagram @ After CTLE + DFE
6.25 Gbps Channel Simulation: Jitter Analysis

The image shows a screenshot of a simulation software interface for jitter analysis. The interface displays various graphs and histograms related to jitter and noise analysis, including DDJ (Data Dependent Jitter) vs Bit, TJ (Total Jitter) Histogram, and Composite DDJ Histogram. The software appears to be used for analyzing the performance of a 6.25 Gbps channel, focusing on the statistical distribution of the jitter and noise impacts. The data is presented in a graphical format, allowing for a visual understanding of the jitter distribution and its effects on the signal quality.
**Step-2:** Customize IP -> Bring in M-code or C++ Code

Fine-tune and Customize models with Matlab Syntax and/or C++ code
**Step-3:** One-click AMI Code-Generation

Define Reserved and Model Specific Parameters -> Automatically configure appropriate AMI wrapper

One-click AMI Code-generation
**System Vue: TX Modeling Example (4)**

**Step-4:** Automatically Generated .ami and Visual-Studio

The visual studio project automatically created -> One click to create .dll
Benefits of System Vue Design Flow

Automated AMI-Model Generation

1. Complete “Automation” of Code-generation and Model Compilation
   
   *a task that routinely takes months because of its complexity*

2. Basic building blocks that can used to start model development
   
   *FIR/IIR filters, FFE, DFE, CDR etc.*

3. Easily customize models in include custom IP
   
   *Custom C++ and M-code*

4. Easy to use

5. Link with Flex DCA
Next steps: Go to EEsof.com to evaluate ADS

### Products
- Advanced Design System (ADS)
- Electromagnetic Pro (EMPro)
- Genesys RF & Microwave Design Software
- GoldenGate RFIC Simulation Software
- IC-CAP Device Modeling Software
- SystemVue ESL Software

### Design Flows
- MMIC Design
- RFIC Design
- RF & Microwave Board Design
- Signal Integrity Analysis

### Resources
- Knowledge Center
- Foundry & Industry Resources
- University Donation Resources

### Related Links
- **Agilent EEsof EDA Design & Simulation Software** - Electronic Design Automation software for high-frequency system, modeling, and RF circuit design applications.
- **Signal Integrity** - Agilent Blog on Multigigabit/s Chip-to-Chip Links
- **Agilent EEsof FDA Evaluation Code Request Form** - Use this form to request an evaluation license, redeem an evaluation ticket, or renew an existing evaluation license.