E-Band Wireless Backhaul: System Design & Test Challenges

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Outline
System-level approach to modeling, simulating and verifying E-Band Systems

1. E-BAND SYSTEM OVERVIEW
2. ADVANCED MODEM TECHNOLOGIES
3. RF INTEGRATED VERIFICATION & TEST
4. HARDWARE & MEASUREMENTS
Future mobile network infrastructure

*Where does the data actually go?*

- **Device-to-device communications**
- **Vehicular communication**
- **Wireless backhaul**
- **Ultra dense deployments**
- **Multi-hop**
- **Machine type devices**

**Frequencies**
- Sub-GHz
- 100GHz
- 200GHz
- 300GHz

*E-band*(71-76/81-86GHz)

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E-Band Webcast, March 2014
E-band applications

Small Cell Backhaul – inexpensive, compact, capacity, easy deployment
E-band applications

Mobile Backhaul – flexible locations, multiple services
E-band applications

Lower-cost infrastructure complement to fiber
Light Licensing of ITU “e-band” Spectrum

71-76/81-86 GHz License light regime in USA and Europe
- 2005, USA FCC Light licensing
- 2007, UK office of communications (OFCOM)
- 2007, Australian Communication and Media Authority (ACMA)

Why e-band for wireless backhaul?
- Uncongested frequency band
- High antenna directivity with pencil beam
- Separate two frequency band without interference concern
- Light licensing scheme
ITU-R Radio-Frequency Arrangements F.2006

Combining the 250 MHz channels from 71-76/81-86 GHz bands into a single FDD arrangement with duplex separation of 10 GHz.

Example of aggregating multiple 250 MHz channels, possibly alongside with original 250 MHz wide channels within the joint 71-76 GHz and 81-86 GHz FDD arrangement.
## E-Band Products, Technical Information

<table>
<thead>
<tr>
<th>Functionality</th>
<th>1&lt;sup&gt;st&lt;/sup&gt; Generation</th>
<th>2&lt;sup&gt;nd&lt;/sup&gt; Generation</th>
<th>Scalable 2&lt;sup&gt;nd&lt;/sup&gt; Generation</th>
<th>Future</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation</td>
<td>Single Carrier, QPSK/BPSK</td>
<td>Adaptive Modulation – 64 QAM or Higher</td>
<td>Adaptive Modulation – 64 QAM or Higher</td>
<td>Multi-level modulation or other</td>
</tr>
<tr>
<td>Channel Width</td>
<td>Fixed or Variable Channels 250 MHz – 1 GHz</td>
<td>Variable Channels 250 MHz – 500 MHz</td>
<td>Variable Channel Size &lt; 250 MHz</td>
<td>Variable Channel Size</td>
</tr>
<tr>
<td>Capacity</td>
<td>Less Than 1 Gbps</td>
<td>1 ~ 2 Gbps</td>
<td>2.5 Gbps, Extension to 5 Gbps with polarization</td>
<td>10 Gbps or More</td>
</tr>
<tr>
<td>Latency</td>
<td>&gt;150 µSeconds</td>
<td>21 – 150 µSeconds</td>
<td>20 µSeconds or Less</td>
<td>?</td>
</tr>
<tr>
<td>Channel Coding</td>
<td>RS</td>
<td>RS, LDPC</td>
<td>RS, LDPC</td>
<td>LDPC</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>35+ Watts</td>
<td>21-34 Watts</td>
<td>20 Watts or Less</td>
<td>?</td>
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</tbody>
</table>
Design and Verification Challenges

**SYSTEM ARCHITECT**
- System-level specs
- Accurate cross-domain
  - Modeling & Simulation
  - Architectures, Partitioning
  - Troubleshooting, Verification

**BASEBAND**
- Advanced modem techn.
- Concurrent TX Channels
- Adaptive
  - Coding
  - Modulation
  - Channel spacing
  - Channel compensation

**T&M VERIFICATION**
- Higher sampling rate
- Wider bandwidth

**RF / mm-WAVE**
- Signal routing & losses
- Limited performance
- Lack of characterization data

**ECOSYSTEM, REQUIREMENTS**
- Complexity, density
- Concurrent teams
- Evolving Stds, regulations, vendors, macro-economy, etc
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Signal processing approaches to RF/System challenges

- Millimeter-wave frequencies are difficult, expensive to engineer
- “Where is the least expensive place to address key issues?”

<table>
<thead>
<tr>
<th>RF Challenge</th>
<th>Signal Processing Approach</th>
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</thead>
<tbody>
<tr>
<td>Channel / Propagation</td>
<td>Adaptive <strong>Equalization</strong> can maximize available analog dynamic range vs. time</td>
</tr>
<tr>
<td>RF performance margins</td>
<td>Powerful <strong>Coding</strong> techniques maximize the data throughput for a finite SFDR</td>
</tr>
</tbody>
</table>
Adaptive Signal Processing

Changing environment
• Decision-directed adaptive equalizer

Analog impairments
• Automatic correction of TX and RX quadrature impairments in DSP
• Closed-loop adaptive digital pre-distortion (DPD)

Baseband efficiency
• Adaptive coding and modulation, with software-defined profile
• Re-configurable symbol rate and bandwidth
• Reed-Solomon and LDPC FEC, with configurable codeword length and payload amount
• Convolutional interleaver, with configurable depth
Channel Equalization

Why use EQ?

- Inter-symbol Interference (ISI) is created by multipath with time dispersive channels ($W > B_C$)
- “Equalization” compensates for ISI

EQ Types

- **Linear**: Time-invariant channels
- **Nonlinear**: Time-varying severe channel distortion
  - Decision Feedback Equalization (DFE)
  - Maximum Likelihood Symbol Detection
  - Maximum Likelihood Sequence Estimator (MLSE)
Adaptive Equalization

- Equalizer suppress time-varying communications channel distortion by set $d[k] = t[k-u]$

- Relationship between $d[k]$ and $y[k]$ determines the mode of the equalizer
Decision Feedback Equalizer (DFE)

Use feedback of detected symbols

Figure 2. Decision Feedback Equalizer
EQ convergence and Mean-Squared Error (MSE)

- **RLS** converges faster than LMS algorithm towards the final mean squared error
- But, **LMS** is simpler
- **RLS/LMS** algorithm successfully combines speed & efficiency
2 Coding Algorithms

Typical behavior of the bit error probability versus bit signal-to-noise ratio for uncoded and coded systems

Potential coding gains of coded transmission v.s uncoded
High Performance Coding Algorithms being adopted in E-Band Modems

Ingredients of Shannon’s proof?
- Long, structured, “pseudorandom” codes
- Practical, near-optimal decoding algorithms

For example?
- **Turbo** codes (1993)
- Low-density parity-check (**LDPC**) codes (1960, 1999)
- Bring Shannon limits to within reach, on a wide range of channels.

What’s the problem?
- complexity
Bit Error Rate & Channel Coding Performance

**Major E-band Modem Modulation Schemes**

- **1st Gen**: BPSK, QPSK
- **2nd Gen**: 16, 32, 64 QAM
- **3rd Gen**: Higher Order?

**Optimum receiver with feed forward AGC, differential correlation frame synchronization, correlation frequency synchronization, phase estimation, no equalizer, DD-PLL frequency tracking.**

**LDPC Coding Gains**

**Optimum receiver with FEC sub-system (BCH and LDPC Coding)**

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Figure. Simulated BER v.s Eb/N0 curves in AWGN channel.

Figure. Simulated BER v.s Eb/N0 curves with Custom LDPC Code.
Digital Modem – Algorithmic Verification

Building a robust DSP chain, then validating the architecture
Digital Modem – Algorithmic Verification

Building a robust DSP chain, then validating the architecture
Algorithm Verification Methodology

Integrate your BB algorithm IP into the system-level verification

- Working TX/RX
- Individual algorithms parameterized
- Probe inside
- Make test vectors
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E-Band RF Transceiver

UP Stream / Down Stream Communication

E-Band Transceiver Block Diagram Example

RFIC
Modeling RF System Architectures

**TRANSMITTER**

- **Source1=FTXIF MHz at -12 dBm**
- **TX_IF_IN {MultiSource}**
- **Fhi=21750MHz [FTXIF+1500]**
- **Flo=18750MHz [FTXIF-1500]**
- **N=3**
- **IL=0.01dB**
- **BPF_Butter_3 {BPF_BUTTER}**
- **LO=7dBm**
- **ConvGain=0dB [TXRFMIXERG]**
- **Mixer_3 {MIXER_BASIC}**
- **NF=9.49dB [TXPANF]**
- **G=14dB [TXPAG]**
- **RFAmp_4 {RFAMP}**
- **IP1dB=100dBm [TPAKIP1dB]**
- **L=0dB [TXPAKG+1]**
- **Attn_1 {ATTN_NonLinear}**
- **Pwr=7dBm**
- **F=60750MHz [3*FTXIF]**
- **LO4 {PwrOscillator}**
- **F=86.5GHz**
- **Flo=80.5GHz**
- **N=5**
- **IL=0.01dB**
- **BPF_Butter_7 {BPF_BUTTER}**
- **ZO=50Ω**
- **OP1dB=8dBm [RXIFOP1dB]**
- **NF=10dB [RXIFNF]**
- **G=4dB [RXIFG]**
- **RFAmp_2 {RFAMP}**

**RECEIVER**

- **Source1=FTXRF MHz at -12 dBm, BW: CS MHz**
- **TX_IF_IN {MultiSource}**
- **OP1dB=4dBm [RXLNAOP1dB]**
- **NF=8dB [RXLNANF]**
- **G=22dB [RXLNAG]**
- **RFAmp_1 {RFAMP}**
- **LO=20125MHz [FTXIFCS2]**
- **F=86.5GHz**
- **Flo=81GHz**
- **N=3**
- **IL=0.01dB**
- **BPF_Butter_6 {BPF_BUTTER}**
- **LO7 (PwrOscillator) F=60750MHz [3*FTXIF] Pwr=7dBm**
- **OP1dB=4dBm [RXIFOP1dB]**
- **RF Amp_2 [RFAMP] G=4dB [RXIFOP1dB]**
- **LO7 (PwrOscillator) F=60750MHz [3*FTXIF] Pwr=7dBm**
- **PhaseN=(4) [-60; -80; -100; -96dB]**
- **BPF_Butter_9 {BPF_BUTTER}**
- **ZO=50Ω**
Rx Front End Modeling – Direct Conversion

81-86GHz EBAND

LNA

IFA

PRIMARY LO

I-channel

Q-channel

2nd IF

Source1=EBAND_FREQ GHz at EBAND_PWR dBm

Source2=EBAND_FREQ GHz at EBAND_PWR dBm, w Phase Noise
Key system questions

- Do the baseband PHY algorithms work with the RF?
- What are the root causes of each problem?
- Which domain is the best place to address these problems?
- Can you correlate measurements with simulations?
- If not, what assumptions are “baked into the results”??
System Level Modeling – integrated approach

E-band Source

E-band Golden Transmitter

E-band Receiver

BER & FER
System Level Modeling

E-band Receiver Sensitivity Measurements

DATAFLOW SIMULATION

E-band Golden Transmitter

E-band Source

RF SYSTEM ANALYSIS

SpectraSys Receiver Model

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Transmit Chain Analysis - EVM

E-Band Reference Source
- Randomized payload data generation
- Baseband transmission source
- Generalized data frame
- Multiple type of modulation

Up-Converter Impairments
- D-to-A converter level and range
- LO phase noise
- Modulator phase gain and phase imbalance

Tx Non-linearity and channel
- Fast circuit envelop co-simulation
- ADS co-sim
- White Gaussian noise

Measurement and waveform download
- EVM, CCDF, Spectrum measurement
- Waveform download into wide band AWG
- Vector signal analysis

Digital Modem Source for Linear Modulation
DSSS System

1 1 0 1 0
Fast Circuit Envelope Simulation with Jitter Injection

- Modulation Envelope is Represented in the Time Domain
- Carrier is Represented in the Frequency Domain

FCE nonlinear model advantages:
- Direct behavioral-modeling extraction method
- Convenient use model
- Fast & accurate system simulations:
  - RF Nonlinearities
  - Freq Response Variations
  - Memory Effects
  - Noise spectral density (NEW)
  - Frequency conversion between pins
- Supports multiple I/O pins and internal nodes

At lower frequencies, X-parameters are also a good modeling option
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Bit Error Rate

Easy math but difficult test bench implementation

**Bit error rate**

\[
BER = \frac{\text{# of error bits received}}{\text{# of transmitted bits}}
\]

**Probability of error**

\[
P_e = \frac{1}{2} (1 - \text{erf}) \sqrt{\frac{E_b}{N_0}}
\]

**Variance of Pe**

\[
VAR = \frac{1 - P_e}{P_e \times N}
\]
BER Measurement Considerations

• Transmit enough number of bits
  - for a $P_e$ of $10^{-6}$, with a relative variance of 0.01, a sample size $N$ of approximately $10^8$ bits is required

• Use PRBS to avoid deterministic jitter
  - Use a randomizer or scrambler in transmitter
  - Make sure all constellation points are approximately equally populated

• Synchronize test and reference signals

wrong sync:  ... 0 1 1 0 0 1 0 0 1 ...
correct sync: ... 0 1 1 0 0 1 0 0 1 ...
... 0 1 0 1 1 0 1 0 0 1 ...
t₀ t₁ t₂
E-Band RFIC Loopback BER Measurement

**SYSTEMVUE**
- **E-band Golden Source**
  - Digital modem library
  - Automatic waveform creation & download
  - Replaceable
- **E-band Reference Receiver**
  - BER/FER Measurement

**RFIC DUT**
- **M8190A** 12 GSa/S Arbitrary Waveform Generator
- **M9703A** AXIe 12-bit High-Speed Digitizer/Wideband Digital Receiver
  - Interleaving to get 4ch @ 3.2 GSa/s

**BER/FER Measurement**
- C++, .m or SV DSP parts formats

- **Wider BW (8 GHz BW)**
- **Higher Sampling (40 GSa/s)**
System Level Verification
Leveraging test vectors out of the simulation environment

DATAFLOW SIMULATION

E-band Golden Transmitter

E-band Source

RFIC DUT

BBIQ→RF

RF→BBIQ

BER & FER

E-band Receiver

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Anticipate Accelerate Achieve
A Top-down Design & Verification Flow
Consistent EVM, BER measurement across RF/BB domains, and throughout the R&D lifecycle

System design
RF Architecture
Baseband design
PHY Reference

Handwritten HDL
Custom IP

Algorithms
C++, .m

Target-neutral HDL Generation

Dataflow Simulation
.m/C++ ALGORITHM
HDL Simulator(s)

SIMULATED H/W

FPGA Synthesis

.FPGA Target

.bit Files

REAL HARDWARE

MEASUREMENT, ANALYSIS

FlexDCA software

VSA software

Infiniium Scope

MXA / PXA

Logic Analyzer

MXG / ESG

Wideband AWG

Wideband Digitizer

DIGITAL BITS, or MODULATED CARRIERS

Target-neutral HDL Generation

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RF Architecture
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C++, .m

Target-neutral HDL Generation

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.m/C++ ALGORITHM
HDL Simulator(s)

SIMULATED H/W

FPGA Synthesis

.FPGA Target

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REAL HARDWARE

MEASUREMENT, ANALYSIS

FlexDCA software

VSA software

Infiniium Scope

MXA / PXA

Logic Analyzer

MXG / ESG

Wideband AWG

Wideband Digitizer

DIGITAL BITS, or MODULATED CARRIERS
Design and Verification Challenges

ECOSYSTEM, REQUIREMENTS
- Concurrent approach
- Earlier validation
- Higher confidence

System-level simulation
- SystemVue Dataflow, Reference IP, RF-DSP co-verification, Links to Test

Baseband Algorithm Modeling, Implementation
- Math algorithms, C++, VHDL/Verilog, SystemC, Hardware-in-Loop

3rd Party API
- Scenarios, Embedding Automation

Design & Test Integration

RF System Arch.
- IC/Board/Module Physical Design

Pkg/Connectors 3DEM Antenna
The industry is moving into very challenging areas. **A step forward is needed** for concurrent DSP, RF, and T&M design lifecycle methodologies, not just raw technology.

“Golden Reference” blocks and open, system-level modeling alongside RF effects **provides earlier confidence** in modem algorithm development, **reducing net overall verification effort**

A system-level approach **integrating both RF & BB** reduces guesswork in setting specifications and produces higher-performing system designs.

**E-Band measurements are challenging**, so using simulation to fill gaps and leverage test-vectors can reduce costs, re-use assets

**Allows concurrent development and joint RF/BB architectures** for earlier, more robust E-Band Systems.
Questions? - Connect with Us

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to see the latest solutions that can be used for 4G and 5G

Specifically featured: W1902 Digital Modem library