Nonlinear Characterization and Modeling Through Pulsed IV/S-Parameters
OUTLINE

– Introduction

– Core device model extraction

– Model Enhancement

– Model Validation
Types of Large-Signal Transistor Models

- Physic model
- Compact model
- Behavioral model
Commercial compact FET models

- Mostly used models for GaN HEMTs

<table>
<thead>
<tr>
<th>FET models</th>
<th>Number of parameters</th>
<th>Electro-thermal effect</th>
<th>Trapping Effects</th>
<th>Original Device Context</th>
</tr>
</thead>
<tbody>
<tr>
<td>Curtice3 [1]</td>
<td>59</td>
<td>No</td>
<td>No</td>
<td>GaAs FET</td>
</tr>
<tr>
<td>CFET [2]</td>
<td>53</td>
<td>Yes</td>
<td>No</td>
<td>HEMT</td>
</tr>
<tr>
<td>EEHEMT1 [3]</td>
<td>71</td>
<td>No</td>
<td>No</td>
<td>HEMT</td>
</tr>
<tr>
<td>Angelov [4]</td>
<td>80</td>
<td>Yes</td>
<td>No</td>
<td>HEMT/MESFET</td>
</tr>
<tr>
<td>AMCAD HEMT1 [5]</td>
<td>65</td>
<td>Yes</td>
<td>Yes</td>
<td>GaN HEMT</td>
</tr>
</tbody>
</table>

- AMCAD GaN HEMT1 is the only model here with a complete extraction flow based on pulsed IV/RF measurements
Compact FET model extraction flow

Various effects are successively added
Parameter extraction methodology

- Based on 18-element AMCAD original current source
- Compatible with Agilent ADS
OUTLINE

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Parameter extraction methodology

Core device model

1st step: bias-dependant S parameters

Multibias set of linear models

2nd step: large signal fitting

Nonlinear model

Measurements

Modeling
Parameter extraction methodology

1st step: bias-dependant S parameters

Multibias set of linear models

2nd step: large signal fitting

Nonlinear model

Measurements

Modeling
Pulsed IV measurements

Short pulse: Quasi-isothermal conditions

Low duty cycle: Constant mean temperature

Quiescent bias point: Thermal conditions fixed
Compact FET model extraction flow

Modelling Process

Pulsed S parameter measurements

Bias T

Bias

DUT

Bias T

Rs
Rd
Ld
Cpd
Ls
Cpg
Gd
Gm
τ
Cd
Ri
Rg
Lg
Cds
Rg
Lg
Cpg
Ls
Cpd
Ld
Rs
Rd

Your complete measurement & modeling solutions partner!
Pulsed S parameter measurements

The first & most important point:

- Pulsed S parameter measurements must not be noisy
- Small S2P measurement variation = strong influence over the linear model extraction: optimization algorithm

Requirements:

Dynamic range in pulsed mode > 90dB for Duty Cycle ~ 5%
Pulsed S-parameter Measurements

Pulsed S-parameter measurements must not be noisy at low duty cycle with narrow pulse width

Pulse detection methods

**Wideband detection**
- No pulse desensitization
- Increased noise with narrow pulse width due to wider IF bandwidth
- Limited pulse width by maximum available IF bandwidth

**Narrowband detection**
- Narrower minimum pulse width than wideband pulse
- Reduced dynamic range with low duty cycle due to pulse desensitization by $20\log(\text{duty cycle})$
PNA/PNA-X Noise reduction techniques and performances

Peak-to-peak noise with wideband detection at 10% duty cycle

No averaging in calibration and measurements

Averaging 20 times in calibration and measurements

<table>
<thead>
<tr>
<th>Pulse width (IFBW)</th>
<th>No Averaging</th>
<th>Averaging 20 Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 us (150 kHz)</td>
<td>0.03 dB</td>
<td>0.005 dB</td>
</tr>
<tr>
<td>5 us (280 kHz)</td>
<td>0.04 dB</td>
<td>0.006 dB</td>
</tr>
<tr>
<td>1 us (1.5 MHz)</td>
<td>0.06 dB</td>
<td>0.012 dB</td>
</tr>
<tr>
<td>500 ns (3 MHz)</td>
<td>0.09 dB</td>
<td>0.013 dB</td>
</tr>
</tbody>
</table>
PNA/PNA-X Noise reduction techniques and performances

Dynamic range with wideband detection at 10% duty cycle with 10 us, 5 us, 1 us, 500 ns pulse width

No averaging in calibration and measurements, 1% smoothing on

Averaging 20 times in calibration and measurements, 1% smoothing on
PNA/PNA-X Noise reduction techniques and performances

Peak-to-peak noise at 10% duty cycle

*Wideband detection* with 20 times averaging in calibration and measurements

*Narrowband detection* with no averaging in calibration and measurements
PNA/PNA-X Noise reduction techniques and performances

Dynamic range with narrowband detection at 500 ns pulse width

- Hardware gating
- Crystal filter
- Software gating
- Spectral nulling

No Averaging, 1% smoothing on, 500 Hz IF bandwidth

- >100 dB at 10%
- >100 dB at 5%
- 90 dB at 1%
- 85 dB at 0.5%
<table>
<thead>
<tr>
<th></th>
<th>E836x Legacy PNA</th>
<th>N524xA PNA-X</th>
<th>N522xA New PNA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pulse generator</strong></td>
<td>External</td>
<td>Internal/External</td>
<td>Internal/External</td>
</tr>
<tr>
<td><strong>Pulse modulator</strong></td>
<td>External</td>
<td>Internal/External</td>
<td>Internal/External</td>
</tr>
<tr>
<td><strong>Wideband detection</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max BW/Min PW</td>
<td>35 kHz / 50 us</td>
<td>15 MHz / 100 ns</td>
<td>15 MHz / 100 ns</td>
</tr>
<tr>
<td>High level noise*</td>
<td>0.006 dBrms</td>
<td>0.002 dBrms</td>
<td>0.002 to 0.003 dBrms</td>
</tr>
<tr>
<td>Dynamic range**</td>
<td>114 to 123 dB</td>
<td>124 to 129 dB</td>
<td>127 dB</td>
</tr>
<tr>
<td><strong>Narrowband detection</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min IF gate width</td>
<td>20 ns</td>
<td>&lt;20 ns</td>
<td>&lt;20 ns</td>
</tr>
<tr>
<td>Dynamic range***</td>
<td>85 dB</td>
<td>&lt;105 dB</td>
<td>&lt;105 dB</td>
</tr>
</tbody>
</table>

* Specified as trace noise magnitude, at 20 GHz, at 1 kHz IF bandwidth
** Specified performance at 20 GHz, at 10 Hz IF bandwidth
*** Measured performance at 10 GHz at 10 Hz IF bandwidth, 1% duty cycle
Compact FET model extraction flow

Small-Signal

- $R_g$
- $L_g$
- $C_{pg}$
- $L_s$
- $C_{pd}$
- $L_d$
- $R_s$
- $R_d$

IV Model

- $R_i$
- $C_{ds}$
- $G_m$
- $G_d$
- $C_{gs}$
- $C_{gd}$
- $R_{gd}$

- $D_{gs}=f(V_{gs})$
- $D_{gd}=f(V_{gd})$
- $I_{ds}=f(V_{gs},V_{ds})$

Compact FET model extraction flow

Your complete measurement & modeling solutions partner!
Pulsed IV parameter measurements

- Pulsed IV measurements must be accurate from low to high voltage/current values

- Accurate IV data =
  - Reliable current source
  - Transconductance
  - Leakage current
  - Ideality factor schottky diode

IVCAD
Pulsed IV parameter measurements

How to get accurate pulsed IV measurements?

- PIV system
How to get accurate pulsed IV measurements?

Pulsed IV parameter measurements

- Gate voltage ranges: +15V to -15V
- Drain voltage ranges: 25V to 250V
- Pulse shape monitoring with 20ns time resolution
- 15 bits + sign
- 16 bits
Pulsed IV parameter measurements

How to get accurate pulsed IV measurements?

Measurement Resolution

Voltage Absolute Accuracy

Voltage Range

0.6mV

65mV

15V

0V

-15V

0mA

20mA

200mA

9μA

400μA

200mA

1μA

40μA

20mA

Measurement Resolution
Voltage Absolute Accuracy
Voltage Range
Pulsed IV parameter measurements

How to get accurate pulsed IV measurements?

Measurement Resolution
Voltage Absolute Accuracy
Voltage Range

0V  25V  250V

0.53mV  4.9mV

0A  1A  10A  22µA  2mA  200µA  20mA

0V  25V  50mV  500mV
Pulsed IV & S parameter measurements

How to get accurate pulsed IV measurements?

Synchronisation between Pulse IV and pulse S parameters
Pulsed S parameter measurements

How to get accurate pulsed IV measurements?

Synchronisation between Pulse IV and pulse S parameters
Parameter extraction methodology

1st step: bias-dependant $S$ parameters

Multibias set of linear models

2nd step: large signal fitting

Nonlinear model

Measurements

Core device model

Modeling
Small signal FET modeling

- **Extrinsic parameters**
  - pad capacitances $C_{pg}$, $C_{pd}$
  - port metallisation inductances $L_g$, $L_d$, $L_s$
  - port ohmic resistances $R_g$, $R_d$, $R_s$

- **Intrinsic parameters**
  - channel capacitances $C_{gs}$, $C_{gd}$
  - voltage-controlled current source with transconductance $g_m$ and transit time delay $\tau$
  - ohmic resistances $R_i$, $R_{gd}$
  - output capacitance $C_{ds}$ and resistance $R_{ds}$
Small signal FET modeling

- Extraction of extrinsic and intrinsic parameters:
  - There is only one set of extrinsic parameters for which intrinsic parameters are independent from the frequency.
  - For a given set of extrinsic parameters, intrinsic admittance matrix of the device is extracted from measured [S] parameters.

- Set min. and max. for each extrinsic parameter:
  - User choice
  - Initiated by cold FET meas.

- Optimization algorithm: annealing, fast simulated diffusion (intrinsic parameters calculus)

- Fit?
  - No
  - Yes

Multi-biasing extraction of the linear model
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Model Enhancement
- Specific measurements
  - diodes
  - g-d breakdown
  - thermal effects
  - charge carrier trapping
  - 3rd step: setting of additional parameters
    - Enhanced Nonlinear model
Compact FET model extraction flow

Various effects are successively added

Dgs = f(Vgs)
Dgd = f(Vgd)
Ids = f(Vgs, Vds)

Cgs = f(Vgs)
Cgd = f(Vgd)

Dgs = f(Vgs, T)
Dgd = f(Vgd, T)
Ids = f(Vgs, Vds, T)

Ids = f(Vgs_trap, Vds, T)

Rs = f(T)
Rd = f(T)
Non linear capacitances

• Gate charge is partitioned into gate source and gate-drain charge. Each charge expression is a function of both VDS and VGS.
• For power amplifier applications, 2D models do not bring a breakthrough in the precision, but they are much more complex.
• 1 dimension capacitances extracted along optimal load-line are preferred due to simplicity. 1D capacitances with equations based on hyperbolic tangents are naturally charge conservatives.
• Output Capacitance Cds is linear – no voltage dependence (weak anyway)

→ Cgd=f(Vgd) + Modeling simplicity. Very good convergence

→ Cgs=f(Vgs) - Validity of the 1D?
Non linear capacitances

- Capacitances modeling: 1D vs 2D

- Better fit of the 2D model in wider domain
- But the 1D model has a good behavior
Non linear capacitances

Cgd • Feedback capacitance Cgd is a strong function of drain voltage.

Cgd capacitance extracted along optimal load-line for power amplification.
Non linear capacitances

$C_{gs}$

• Input capacitance $C_{gs}$ is a strong function of gate voltage.

The gate-voltage non-linearity also effects model’s harmonic generation

$C_{gs}$ capacitance extracted along optimal load-line for power amplification
AMCAD drain current model formulation allows to predict very accurately the I-V curves, the partial derivatives gm and gd, the knee voltage and the transconductance decrease at high current.
Output current source

Idss ↔ amplitude

Vdsp, A ↔ slope

Vp0 ↔ pinch-off  Vds (V)

M, P ↔ fitting parameters

AlphaGm, Vgm, BetaGm, Vdm ↔ gm (derivative)
Diodes

- Gate-drain and gate-source diode equations include forward conduction of gate current

\[ ID = I_s e^{\alpha V_d} \] (a classical formulation)
Breakdown generator

• Gate-drain Breakdown generator

The breakdown phenomena leads to a current from the drain to the gate when the device is pinched-off and for high values of Vds voltage. In this case, the whole negative current characterized on the gate is seen in positive on the drain.

A polynomial expression with order 4 is necessary to model the cross of breakdown curves, with varies depending on the process.
Thermal effects

• Temperature dependence with ambient or chuck temperature

-40°C

25°C

150°C

• Static and Dynamic self-heating effects
Thermal effects

**IV Modeling @ several temperatures**

Measure / IV Model @ 25 °C

Measure / IV Model @ 150 °C

**IV parameters versus temperature**

**Temperature dependence**

**Equations**

**Thermal parameters**
- Access Resistances
- Current Source
- Diodes

\[
\begin{align*}
R_s &= R_{s0} + \alpha_R R_s T \\
R_d &= R_{d0} + \alpha_R R_d T \\
I_{dss} &= I_{dss0} + I_{dss1} T \\
P &= P_0 + P_1 T \\
N_{gs} &= N_{gs0} + N_{gs1} T \\
N_{gd} &= N_{gd0} + N_{gd1} T \\
I_{sgs} &= I_{sgs0} + I_{sgs1} e^{(T/T_{sgs})} \\
I_{sgd} &= I_{sgd0} + I_{sgd1} e^{(T/T_{sgd})}
\end{align*}
\]
Thermal effects

Thermal impedance extraction – by simulation

\[ Z_{th}(s) = \frac{1}{sC_{th1} + \frac{1}{R_{th1} + \frac{1}{sC_{th2} + \frac{1}{R_{th2} + \frac{1}{sC_{th3} + \ldots + \frac{1}{R_{thn}}}}}}} \]
Thermal effects

Thermal impedance extraction – *by measurements*

Wide current pulse characterization

Self Heating Extraction = \( f(t) \)

\[
i(t) = I_0 - \sum_{i=1}^{n} I_i \left( 1 - \exp \left( -\frac{t}{\tau_i} \right) \right)
\]

\[
Z_{th}(t) = \sum_{K=1}^{n} R_{kth} \left( 1 - e^{-\frac{t}{R_{kth}C_{kth}}} \right)
\]

RC cells

Device dynamical self-heating
**Thermal effects**

- Drain current is only temperature dependent model element
- Takes into account ambient temperature and self-heating effects
- Thermal analog circuit to model self-heating and elevated heat sink temperatures
Trapping effects

• Charging and discharging of traps has influence on $I_{ds}$ and leads to current collapse. This is described in the model by trapping effects modifying the gate command and separated into gate and drain lag sub-circuits.
Trapping effects

Gate-lag: decrease of drain current

- green (Vgs0=0 V, Vds0=0 V)
- red (Vgs0=-4 V, Vds0=0 V)

Drain-lag: increase of Vknee

- red (Vgs0=-3 V, Vds0=0 V)
- green (Vgs0=-3 V, Vds0=30 V)

$T_{\text{capture}} \ll t_{\text{IMPULSION}} \ll T_{\text{emission}}$

During the pulses capture takes place, emission freezed
Trapping effects

- Charge of the capacitance = Ionized traps

Charge through Rcapture, Emission through Rémission

Diode = dissymmetry of the capture and emission process

Fundamental assumption: dissymmetry of the capture and emission process

Tuning of the magnitude of the trapping effects
Trapping effects

• Bias dependant gate lag -> current reduction over the entire characteristic
Bias dependent drain lag -> current reduction and shifts the knee-voltage to a higher Vds
Model covers knee walkout to avoid errors in calculation of output power.
Trapping effects

• Decreasing form of the mean output current only reproduced with traps modeled
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– Model Validation
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**Core device model**
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  - 1st step: bias-dependant S parameters
  - Multibias set of linear models
    - 2nd step: large signal fitting
      - Nonlinear model

**Model Enhancement**
- Specific measurements
  - diodes
  - g-d breakdown
  - thermal effects
  - charge carrier trapping
  - 3rd step: setting of additional parameters
    - Enhanced Nonlinear model
      - 4th step: implementation in commercial simulator

**Model Validation**
- Power measurements
  - load-pull measurements
  - CW, pulsed
  - 2-tones
  - time domain
  - 5th step: validation and refinement
    - Final Nonlinear model

*1st step: bias-dependant S parameters
2nd step: large signal fitting
3rd step: setting of additional parameters
4th step: implementation in commercial simulator
5th step: validation and refinement*
**Model validation**

- **Large-signal**

Model validation of a 8x75 µm GaN HEMT with load-pull measurements performed at 6 GHz for optimum PAE load impedance in class-AB.

Model validation of a 8x400 µm GaN HEMT with load-pull measurements performed at 3 GHz for the optimum Pout load impedance in class-B.
Model validation

VNA Based load pull system is preferred for model validation

Specific Architecture

- PA
- Gate
- T
- Tuner f0
- Low loss directional couplers
- CW or pulse RF signal f0 or f1+f2
- VNA
- DUT
- Tuner f0, 2f0, 3f0
- DC or pulse DC supplies + meas Units
- Drain 50Ω
Model validation

VNA Based load pull system is preferred for model validation
Power meter based system are wideband measurement system

VNA based system can be narrowband measurement system

More information for model validation or efficient design
VNA based Load Pull systems

Some Measurement definition

**P\_in**: Power delivered to the DUT by the source

\[ P_{\text{in}} = \frac{1}{2} (|a1|^2 - |b1|^2) = \frac{1}{2} |a1|^2 \times (1 - |\Gamma_{\text{in}}|^2) \]

**P\_out**: Power delivered to the load impedance

\[ P_{\text{out}} = \frac{1}{2} (|b2|^2 - |a2|^2) = \frac{1}{2} |b2|^2 \times (1 - |\Gamma_{\text{load}}|^2) \]

**Power gain** is the ratio of the power delivered to the load \((P_{\text{out}})\) to the power delivered to the transistor by the source \((P_{\text{in}})\).

\[ \text{Gain}_{\text{Power}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{|b2|^2(1 - |\Gamma_{\text{load}}|^2)}{|a1|^2(1 - |\Gamma_{\text{in}}|^2)} \]
Model validation

VNA Based load pull system is preferred for model validation

Specific Architecture

- PA
- Gate
- Tuner f0
- Low loss directional couplers
- DUT
- VNA
- Tuner f0, 2f0, 3f0
- DC or pulse DC supplies + meas Units
- 50Ω
- Drain
- CW or pulse RF signal f0 or f1+f2
- Phase reference

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Large signal impact - class AB, 25V, 10 GHz – Comparison with measurements

With non optimal loads:

- Time domain load pull measurements
- Deembedding in the intrinsic reference plane
- Parasitic extrinsic elements must be accurately extracted by previous S parameter measurements
Testing Model Validity with Pulsed IV Simulations
(Using Agilent ADS)

- Is your FET model suitable for high-frequency design?
  - Is dynamic behavior included?
  - Is it well-fitted for high-frequency, large signals?
  - What is the model’s valid range of use?


Maury – Agilent – AMCAD Solution
Compact Transistor Models: The Roadmap to First-Pass Amplifier Design Success

Amplifier designers have been making use of modern transistor models since their first appearance in the mid-1970s. Models have allowed engineers to create advanced designs with first-pass success, without the need for multiple prototypes and design iterations. But with so many different modeling techniques, how does one select which one to use? The three most common types of models used in industry today are: physical models, compact models and behavioral models.

Physical models, as their name suggests, are based on the physics of the device technology. These models are dedicated to the transistor itself and not the overall circuit. Due to the nature of the model, complex model equations have to be used, which can lead to time-consuming simulations. The advantage of the physical model is that it can be successfully used over the largest operating range, compared to alternate models, since equations are used to describe complete physical rules rather than actual measurement results.

Compact transistor models, based on measured IV and S-parameters, allow designers to shift focus from transistor designs to circuit design. Extracted from quantitative pulsed IV and pulsed S-parameter data and validated with load-pull characterization, compact transistor models contain a reduced set of parameters. Unlike other model types, compact models take into account complex phenomena, such as electrons, thermal and trapping effects. For simulations under nonlinear operating conditions, responses to complex modulated signals (such as EVM or ACPR) are accurately predicted at low-frequency and high-frequency linearity effects are taken into account. Compact transistor models are ideal for system-level applications, as developing a model from IV and S-parameters is straightforward and relatively quick. Packaged-transistor models need to include a die-level model as well as a bonding model and package model, and consequently can be time-consuming and costly.

Behavioral models, based on frequency domain measurements, are far less realistic than physical or compact transistor models, but can be easily developed for any type of component (including die-level or packaged transistors). Behavioral models are considered “black-box” models, where only the response of the component is considered.

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