MIPI M-PHY, D-PHY and C-PHY
Receiver Testing –
Today and Tomorrow

October 21st, 2014
Agenda

– MIPI Overview, history and recent changes
– RX test: recap of methodology
– M-PHY key features, changes in spec & methodology
– D-PHY recap of basics, signaling, LP- and HS- modes
– C-PHY intro on 3-wire 3-level signaling
– Keysight test solutions M8000 based
– Summary, links, QA
Technology Challenges in Mobile Computing
Technology Challenges in Mobile Computing

Too Many Interfaces, All Different
MIPI = Mobile Industry Processor Interface - Goals

- Structure the intestines of mobile devices ranging from smartphones to wireless-enabled tablets and netbooks

- Benefit the entire mobile industry by establishing standards for hardware and software interfaces

- Enabling reuse and compatibility making system integration less burdensome

- The distinctive requirements of mobile terminals drive the development of MIPI Specifications
  - Power saving / battery life
  - Bandwidth on demand
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MIPI’s Layered Approach for Application Standards
Why Three Different PHY-layer Standards?
2013 and before

- **D-PHY**
  - Used for camera (CSI-2) and display (DSI) applications
  - Source synchronous, forwarded ½ rate clock
  - Electrical specifications (parasitic capacitances and return loss (RL)) allow usage of established, relatively inexpensive semiconductor process
  - Complex signaling, different amplitudes and data format for Low Power (LP) and High Speed (HS) mode and non-differential “pattern sequence” signaling transition from LP to HS-mode and vice versa
  - Rev. 1.0 / 1.1 with a continuous data rate range up to 1.0 / 1.5Gb/s respectively

- **M-PHY**
  - Proposed high BW successor of D-PHY addressing camera and display applications
  - Embedded clock and PLL-type CDR
  - Discrete data rates (Gears) up to approximately 12Gb/s; sufficient for quite a while
  - Differential signaling and same amplitude in both HS- and LP- mode
Agilent / Keysight Solutions for MIPI RX PHY-test
2013 and before

M-PHY
J-BERT N4903B

D-PHY
ParBERT 81250
Why three different PHY-layer standards? 2014 onwards

- M-PHY
  - Reluctance of camera group to adapt M-PHY because of
    - Specified lower parasitic capacitance / better RL demands more expensive semiconductor process than for D-PHY
    - Discrete instead a “agile” data rates
    - 8B/10B coding overhead of 25%

- C-PHY started
  - New 3-wire / 3 level data format allowing transmission of >1 bit / symbol
  - Embedded clock, CR based on logic and encoding rules
  - HS mode w/ toggle rates reaching continuously up to 2.5Gbaud / 5.75Gb/s
  - LP mode identical to D-Phy
  - Even more complex signaling (HS mode3 w/ 3 wire 3-level signaling) level

- D-PHY extended
  - Rev. 1.2 w/ max data rate 2.5Gbs (achieved through RX deskew)
  - Rev. 2.x started, data rate project beyond 4.5 Gb/s (6.5Gb/s)
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About Receiver (RX) testing

- RX testing
  An RX test is used to determine an RX’s capability to properly detect the digital signal content, even for worst-case impaired input signals. For this testing…
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  1. A Bit Error Ratio Tester’s (BERT) Pattern Generator (BERT PG) is used to emulate a system’s TX plus channel thus generating a data signal containing the impairments to be expected at the RX input when it is operating in a target system. This signal has to be calibrated according to the specification.
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About Receiver (RX) testing

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  2. The input of the RX under test is stimulated with this signal

  3. Proper detection of the digital content is monitored in a suitable fashion to determine performance according to target BER
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M-PHY Link Example

MIPI M-PHY
- Lanes are unidirectional
- Signaling: differential
- 8B/10B coded
- Transmission may appear in burst
- Embedded clock
- PLL type CDR, needs to synch at the beginning of every burst

MIPI M-PHY options
- High speed and (lower speed) low power mode (same as in D-PHY)
- High and low voltage swing operation can be commonly selected for both modes
- Terminated (100 Ohm) or not terminated operation (for power saving purposes) can individually be selected per mode
MIPI M-PHY Data Rates and Module Types

### High Speed Modes

<table>
<thead>
<tr>
<th>HS_Gear</th>
<th>A</th>
<th>B</th>
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<th>optional</th>
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<tbody>
<tr>
<td>4</td>
<td>9984</td>
<td>11661</td>
<td>RT</td>
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<td>3</td>
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<td>1</td>
<td>1248</td>
<td>1458</td>
<td>RT</td>
<td>NT</td>
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</table>

- Data rate [Gb/s]: 4, 3, 2, 1
- Termination: RT = Resistively terminated, NT = Not Terminated
- \( f_{\text{ref}} = 19.2, 26, 38.4 \text{ or } 52 \text{ MHz} \)
- NT = Not Terminated
- RT = Resistively terminated

### Low Power Modes

#### M-PHY-Type-I Module (PWM)

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<thead>
<tr>
<th>LP_Gear</th>
<th>data rate [Mb/s]</th>
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<td>RT</td>
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<td>3 - 9</td>
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<tr>
<td>2</td>
<td>6 - 18</td>
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<td>12 - 36</td>
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<td>48 - 144</td>
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<td>RT</td>
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#### M-PHY-Type-II Module (NRZ)

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<tr>
<td>fsys = f_{\text{ref}}</td>
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<td>NT</td>
<td>RT</td>
</tr>
</tbody>
</table>

- High Speed Gears / data rates valid for both module types
- Type II module only used for Dig_RF_v4
# Jitter Cocktail for Receiver Tolerance Test

## M-PHY Gear 1 & 2

Jitter Cocktail consists of
- ISI generated through Conformance Channel and Replica Trace
- Dual band RJ
- Dual-tone SJ

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>J-BERT parameter</th>
<th>Target Value</th>
<th>Pattern</th>
<th>TIE-HP-filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Adjust wideband RJ (&gt;(f_{\text{L-RX}})) to achieve (\text{STRJ})</td>
<td>RJ</td>
<td>0.10 (\text{UI}<em>{pp}), 7.9m(\text{UI}</em>{rms})</td>
<td>clk/2 (1010)</td>
<td>1/30UI</td>
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<td>2</td>
<td>Add low frequency RJ (&lt;1/30(\text{UI})) to achieve RJ=(\text{TJ-DJ})</td>
<td>BUJ</td>
<td>0.17(\text{UI}<em>{pp}), 13.4m(\text{UI}</em>{rms})</td>
<td>clk/2 (1010)</td>
<td>(f_{\text{L-RX}})*</td>
</tr>
<tr>
<td>3</td>
<td>Turn all RJ off; calibrate SJ ((f_{\text{SJ1}}, f_{\text{SJ2}}, f_{\text{SJ3}}, f_{\text{SJ4}}))</td>
<td>PJ2</td>
<td>0.15 (\text{UI}_{pp})</td>
<td>CJTPat</td>
<td>off</td>
</tr>
<tr>
<td>4</td>
<td>Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve (\text{STDJ}=0.2\text{UI}) ((\text{STSJ}=\text{STDJ-DDJ})) or DJ=0.35(\text{UI})</td>
<td>PJ1</td>
<td>0.35 (\text{UI}_{pp})</td>
<td>CJTPat</td>
<td>off</td>
</tr>
<tr>
<td>5</td>
<td>Turn all calibrated jitter on. Calibrate to prorated eye mask at BER (10^{-6})</td>
<td>PJ2, Amp</td>
<td>(V_{\text{DIF AC}}=43\text{mV}), (1-\text{TJ}=0.52\text{UI})</td>
<td>CJTPat</td>
<td>off</td>
</tr>
</tbody>
</table>

*) \(f_{\text{L-RX}} = F_{\text{C-RX}} = 1/2\text{MHz}\)
Jitter Cocktail for Receiver Tolerance Test
M-PHY Gear 3 (and 4)

Jitter Cocktail consists of
• ISI generated through Conformance Channel and Replica Trace
• Single RJ (broad-band)
• Dual-tone SJ

<table>
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<th>Step</th>
<th>Action</th>
<th>J-BERT parameter</th>
<th>Target Value</th>
<th>Pattern</th>
<th>TIE-HP-filter</th>
</tr>
</thead>
</table>
| 1    | Add wideband RJ (> 10MHz) to achieve RJ=TJ-DJ | RJ | 0.17\(\text{Ul}_{\text{pp}}\)  
13.4\(\text{mUl}_{\text{rms}}\) | clk/2 (1010) | \(f_{L_{-}\text{RX}}\) * |
| 2    | Turn all RJ off; calibrate SJ (f\(_{SJ1}\), f\(_{SJ2}\), f\(_{SJ3}\), f\(_{SJ4}\)) | PJ2 | 0.15 \(\text{UI}_{\text{pp}}\) | CJPat | off |
| 3    | Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve STDJ=0.2UI (STSJ=STDJ-DDJ) or DJ=0.35UI | PJ1 | 0.35 \(\text{UI}_{\text{pp}}\) | CJPat | off |
| 4    | Turn all callibrated jitter on. Calibrate to prorated eye mask at BER 10\(^{-6}\) | PJ2, Amp | \(V_{\text{DIF, AC}}=45\text{mV}\)  
1-TJ=0.52UI | CJTPat | off |

*) \(f_{L_{-}\text{RX}} = F_{\text{C-RX}} = 1/2/4\text{MHz}\)
M-PHY Definition of RX Eye Diagram

Geometry (channel lengths) supported is identical for all Gears despite increasing loss:
- G3 requires TX de-emphasis (3.5 / 6dB depending on swing and actual channel)
- G4 additionally requires receiver equalization (RX-EQ) with CTLE and one-tap DFE

Target BER is $10^{-10}$: however, to shorten measurement time, calibration is done with $3 \times 10^6$ samples for BER = $10^{-6}$ using “prorated” mask w/ larger eye- width and -height (EW, EH) (CTS 3.0)

Calibration for G4: post processing of measured data emulating reference package and RX-EQ

TJ, DJ, STTJ and STDJ are normative with continuous signal
DJ and STDJ are informative with burst using TIEpp method
Setup for M-PHY RX Test and Calibration

Stress Signal Generation and Calibration according to CTS for Gear1 to Gear3

Test board with Replica Traces
- creating test point (TP) for calibration
- equivalent to the ASIC-input pins
Setup for M-PHY RX Test and Calibration
Stress Signal Generation and Calibration for Gear 4

Test board with Replica Traces
- creating test point (TP) for calibration
- equivalent to the ASIC-input pins

MIPI RX Testing – Today & Tomorrow
Gear 4 Stress Calibration using Scope Postprocessing

- EH < 40mV!
- EW < 0.47UI
- EH ~ 82mV
- EW ~ .53UI

MIPI RX Testing – Today & Tomorrow
Setup for M-PHY RX Test
Stress Signal Generation and Calibration according to CTS

– At gear 4 rates subtle differences may already exist in waveforms measured with oscilloscopes from different vendors
– Vendor specific postprocessing SW may increase differences
– In order to increase consistency SIGTest SW proposed to be used for postprocessing and analysis of eye parameters, i.e. EW and EH
PHY Layer Error Detection

- **Challenges with different protocols:**
  - Asymmetrical lane configuration (e.g. 2x HS upstream / 1x LS downstream)
  - Test modes not mandatory (optional normative / recommendation)
  - Specific method defined in protocol spec, not in PHY spec

- **Various error detection methods:**
  - Line Loopback (i.e. bit level loopback)
  - Logic Loopback (i.e. protocol layer loopback)
  - PPI (=Parallel Processor Interface i.e. parallel data output)
  - IBER (=Internal Bit Error Ratio Counter)

- **Not all MIPI applications have settled on preferred test option**

- **Not possible to provide turnkey solution, RX testing always has a custom portion**
Outlook Mipi M-PHY

M-PHY Spec Roadmap

– V4.0 WG approved draft to be ready by October 31\textsuperscript{st} 2014
– V4.0 Spec December 2014
  • Aligns with UniPro 1.8 schedule, which depends on 8b10b
– V4.1 Spec October proposed for 2015
  • Tighten spec/conformance of digital interface (RMMI)
  • Protocol/PHY optimizations
    - Coding scheme w/ less overhead than 8B/10B
    - Fine data rate granularity (cont range of data rates??)
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D-PHY Universal Lane Module Functions

- Lane consisting of 2 wires, Dp and Dn
- TXs and Rxs: Bidirectional
- Contention Detection (LP only)
- Two set’s of TXs / RXs (HS & LP)
- HS-mode:
  - Small Amplitude, terminated (option)
  - Data format: NRZ
  - Signaling: differential
- LP-mode:
  - Large Amplitude, unterminated
  - Data format: RZ
  - Signaling: non-differential
D-PHY Two Data Lane Phy Configuration

- Source synchronous forwarded double data rate clocking
- Data-rate completely agile, no discrete operating frequencies, continuous range
- RX testing is basically stressing set-up- and hold- time conditions (eye closure mainly due to DDJ and skew between Data and Clock)
D-PHY Physical Layer Timing Diagram

Transition LP to HS mode, HS_clk active earlier / longer

High speed mode,
Differential signaling, 100 ohm termination, source synchronous with double data rate clocking

Low power mode
Unterminated, not differential, clock embedded within data
D-PHY Physical Layer Timing Diagram

Transition HS to LP mode and back, no HS_clk in LP mode

Low power mode
Unterminated, not differential, clock embedded within data

High speed mode,
Differential signaling, 100 ohm termination, source synchronous with double data rate clocking
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C-PHY Universal Lane Module Functions

- TXs and RXs: Bidirectional
- Contention Detection (LP only)
- Two set’s of TXs / RXs (HS & LP)
- HS-mode:
  - Small Amplitude, always 50 Ω “star-type“ termination
  - Data format: 3-phase / 3-level
  - Signaling: 3 wires forming a HS-lane
- LP-mode:
  - Large Amplitude, unterminated
  - Data format: RZ
  - Signaling non-differential
Transition HS to LP mode and back

D-PHY

3-Phase

A, B, C

Packet Data → Tail → Trail → HS Exit → Prepare → Constant +x (aka zero) → Pre., Sync, etc. → Packet Data
3 Phase Encoding Concept for C-PHY (HS-mode)

- A data encoding technique utilizing trios rather than pairs of wires
  - 50 Ohm “star-type“termination
  - Utilizes differential receivers, rejecting common mode noise
  - Drivers work similar to D-PHY but control 3 instead of 2 outputs
- Both clock and data are encoded and transported together in a single trio
  - Always a transition at every symbol boundary, which simplifies clock recovery and allows data rate to be completely agile
3-phase Signal Examples 1Gsym/s
HS signal only

- Clean HS signal no jitter no skew
- separated (offset-shifted, left) and overlaid (same offset, right)
  note: for each UI each voltage level appears exactly once!
C-PHY Block diagram

Coding rules and possible wire states:
- 27 possible wire states
- 6 allowed wire states (+x, -x, +y, -y, +z, -z) only those states with different voltage on each wire
- From one symbol to the next symbol only 5 wire states are possible, because a transition is required for CR
- Theoretical coding gain: \( \log_2(5) = 2.32 \)
- Practically usable gain is 2.28 by sending 16 bits in 7 symbols
C-PHY Block diagram

Drawing showing T2 Driver type w/ active mid-level

midpoint voltage is stable at +V/2
(except for asymmetries during transitions (to be filtered by capacitor))
C-PHY Block diagram

Positive Polarity States

Master side

Slave side

“A” to “B” (+x state)

Negative Polarity States

Master side

Slave side

“B” to “A” (-x state)

“B” to “C” (+y state)

“C” to “A” (+z state)

50Ω

100Ω

Drawing showing T2 Driver type w/ active mid-level
C-PHY Block diagram
C-PHY possible TX Realization (principle)

T2 Driver type:
active mid-level, extra pair of Transistors w/ 100Ω

T1 Driver type:
passive mid-level w/ both transistors "open"
C-PHY Signal Characteristics
High Speed Only

Unit Intervall #1
A-B = 0.0-0.5
  = -0.5 = weak 0
B-C = 0.5 – 1.0
  = -0.5 = weak 0
C-A = 1.0 – 0.0
  = 1.0 = strong 1

Unit Intervall #2
A-B = strong 1
B-C = weak 0
C-A = weak 0

Unit Intervall #3
A-B = weak 1
B-C = weak 1
C-A = strong 0
**C-PHY Eye Diagram and Mask Test**

High Speed Only, A-B

- Clock is recovered from the earliest edge of a symbol transition.
- A delay circuit with negative hold time is used to sample data. Supposed to be more resistant to noise and jitter on the system.
Jitter Tolerance Calibration and Measurement

1. Calibrate the Rise/Fall times from the test equipment generator to approx. 115ps using 20%-80% transition time converter.

2. Calibrate the Eye width of three differential signals A-B, B-C, A-C to be 0.7UI by adding Jitter (e.g. DCD) over the already present switching jitter, of course using proper C-PHY clock recovery algorithm.

3. Add ISI jitter by either using a HW channel or SW-programming of the generator to meet the 0.3UI of channel ISI requirement.

4. Tune the Amplitude and the amount of ISI to meet the eye mask requirement of +40 to -40mV for EH and 0.4UI for EW.
   (Allow 10% of variation in calibration over the time scale wrt. the targeted eye mask spec.)

5. After generating the worst case eye as per the mask requirements, Check for any errors in the receiver by comparing the received pattern with the receiver expected pattern and varying DC Common mode.
## Key Features of PHY-Layer Standards

<table>
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<tr>
<th></th>
<th>Rev</th>
<th>Max Data Rate (Gb/s)</th>
<th>Data format</th>
<th>Clocking</th>
<th>Clock Recovery</th>
<th>EQ</th>
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<td>HS</td>
<td>LP</td>
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# Release Status of Standards and Related CTSs

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wip = work in progress
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How Can All of This Be Tested?

Keysight M8000 Series of BER Test Solutions

– Modular system in AXI form factor /frame consisting of
  • HW modules M8041A and M8051A plus M8070 SW forming Keysight J-BERT M8020A
  • modular up to 4 channels enabling channel skew measurements
  • Very much comparable to N4903
– Very well suited for M-PHY
– ...

MIPI RX Testing – Today & Tomorrow
1:1 match of CTS proposed set-up with actual Keysight J-BERT set-up
ISI conformance channel realized through N4915 60001 SATA ISI trace (2)
Test Setup Using Agilent J-BERT M8020A

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Test Setup Using Agilent J-BERT M8020A

M8020A's modularity addresses multichannel applications
# Jitter Cocktail for Receiver Tolerance Test

**M-PHY Gear 1 & 2**

Jitter Cocktail consists of
- ISI generated through Conformance Channel and Replica Trace
- Dual band RJ
- Dual-tone SJ

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>J-BERT parameter</th>
<th>Target Value</th>
<th>Pattern</th>
<th>TIE-HP-filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Adjust wideband RJ (&gt;f\textsubscript{L,RX}) to achieve STRJ RJ</td>
<td>RJ</td>
<td>0.10 UI\textsubscript{pp} &lt;br&gt; 7.9mUI\textsubscript{rms}</td>
<td>clk/2 &lt;br&gt; (1010)</td>
<td>1/30UI</td>
</tr>
<tr>
<td>2</td>
<td>Add low frequency RJ (&lt;1/30UI) to achieve RJ=TJ-DJ BUJ</td>
<td>BUJ</td>
<td>0.17UI\textsubscript{pp} &lt;br&gt; 13.4mUI\textsubscript{rms}</td>
<td>clk/2 &lt;br&gt; (1010)</td>
<td>f\textsubscript{L,RX} *</td>
</tr>
<tr>
<td>3</td>
<td>Turn all RJ off; calibrate SJ (f\textsubscript{SJ1}, f\textsubscript{SJ2}, f\textsubscript{SJ3}, f\textsubscript{SJ4}) PJ2</td>
<td>PJ2</td>
<td>0.15 UI\textsubscript{pp}</td>
<td>CJTPat</td>
<td>off</td>
</tr>
<tr>
<td>4</td>
<td>Keep all RJ off but keep PJ2 on; calibrate STSJ (240 MHz) to achieve STDJ=0.2UI (STSJ=STDJ-DDJ) or DJ=0.35UI PJ1</td>
<td>PJ1</td>
<td>0.35 UI\textsubscript{pp}</td>
<td>CJTPat</td>
<td>off</td>
</tr>
<tr>
<td>5</td>
<td>Turn all calibrated jitter on. Calibrate to prorated eye mask at BER 10\textsuperscript{-6} PJ2, Amp</td>
<td>PJ2, Amp</td>
<td>V\textsubscript{DIE, AC}=43mV &lt;br&gt; 1-TJ=0.52UI</td>
<td>CJTPat</td>
<td>off</td>
</tr>
</tbody>
</table>

*) f\textsubscript{L,RX} = F\textsubscript{C,RX} = 1/2MHz
4. Short Term DJ Cal w/ J-BERT N4903B

Caused by CJPAT over Board Trace + HSSJ

Keep RJ/BUJ off and PJ2 on
Turn on PJ1 with frequency set to >1/30UI e.g. 240MHz

Measure DJ with TIE turned off
Calibrate DJ to target value of  MTDJ = 350mUI
4. Short Term DJ Cal w/ J-BERT M8020A
Caused by CJPAT over Board Trace + HSSJ

Keep RJ/BUJ off and PJ2 on
Turn on PJ1 with frequency set to >1/30UI e.g. 240MHz

Measure DJ with TIE turned off
Calibrate DJ to target value of  MTDJ = 350mUI
4. Short Term DJ Cal w/ J-BERT M8020A

Must stop CJPAT over board trace + HSSJ

Mesure DJ with TIE turned off

Calibrate DJ to target value of $MTDJ = 350 \text{mUI}$

Keep RJ/BUJ off and PJ2 on

Turn on PJ1 with frequency set to $>1/30 \text{UI}$ e.g. 240MHz

---

**Property list**

- PJ1 On
- PJ2 On
- BUJ Off
- RJ Off

**MTDJ = 350\text{mUI}**

**MIPI RX Testing – Today & Tomorrow**
How Can All of This Be Tested?

Keysight M8000 Series of BER Test Solutions

- Modular system in AXI form factor /frame consisting of
  - HW modules M8041A and M8051A plus M8070 SW forming Keysight J-BERT M8020A
  - modular up to 4 channels enabling channel skew measurements
  - Very much comparable to N4903
- Very well suited for M-PHY
- Test Automation: SW Keysight N5990A option 165 & Bitifeye Frame Generator BIT-2060-0001-0
- ...
Building Blocks for a Test and Related SW Products

- **List of parameters to be calibrated along with measurement set-up**
  - AutoCal
  - Cal tables

- **List of (CTS-specified) tests to be performed along with measurement set-up per test**
  - **Test Setquencer**

- **Test Automation**
  - **Keysight N5990A Test Automation SW**
  - **Bitifeye Frame Generator**

- **Patterns & Parameters**
  - **Sequence / pattern editor for all relevant data formats also determining PHY-parameters**
  - **Editor for PHY-parameters**

- **Result capturing**

- **Documentation of Results**

- **RX**
  - **DUT**
  - **TX / Register / DLL**
N5990A Automation Software

Setup of Test Flow

- Parameters of selected item
- Calibrations
  - HS, NRZ (RT)
  - LP, PWM (NT)
- RX tests
  - HS, NRZ (RT)
  - LP, PWM (NT)
N5990A Automation Software
DUT Configuration, Integration of IBERRReader

- Connect (string connection): will be called once at the beginning of the test run. The connection string can contain a customized address (like a COM port) to access to the tool which is able to read out the internal counters of the DUT.

- Init (string mode): will be called once at the beginning of each test. This allows to configure the DUT into the test mode of a particular test (HS or PWM, Gear, Functional Test).

- ResetDUT(): will be called once at each test point. This allows to reset error counters, or set the DUT in a defined mode to be ready for the next test point.

- GetCounter(out double errorCounter, out double bitCounter) will be called after or during a test point execution. The errorCounter value can contain a CRC- or symbol-error, and the bitCounter can contain a bit or burst counter. The counters can provide just simple indicators, if errors happened and if the DUT was able to receive data, or in case of both error and bit counters being implemented, to calculate BER.

- Copy the compiled MPhyBerReader.dll into the ValiFrame Program Files folder.

- A new entry in the BER Reader List will be visible.

- After selection of the Custom BER Reader the N5990A automation software can connect with the DUT.
How Can All of This Be Tested?

Keysight M8000 Series of BER Test Solutions

- Modular system in AXI form factor /frame consisting of
  - HW modules M8041A and M8051A plus M8070 SW forming Keysight J-BERT M8020A
  - modular up to 4 channels enabling channel skew measurements
  - Very much comparable to N4903
- Very well suited for M-PHY
- Test Automation: SW Keysight N5990A option 165 & Bitifeye Frame Generator BIT-2060-0001-0
- How to address C-PHY / D-PHY?
  - We now integrate Keysight AWG modules substituting 8041/51A’s NRZ PGs while still operating under a typical BERT use model
Setup for C-PHY: M8190A, 5 Slot Frame, Embedded Controller

1-lane C-PHY DUT

embedded controller (1 slot)
Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller

4X channel density (4 channels in 1 slot module vs 2 channels in 2 slot module)
Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller

Alternative setup: M8195A, 2 slot frame, embedded Controller
Setup for C-PHY: M8195A, 5 Slot Frame, Embedded Controller

3 AWG modules capable of driving up to 12 wires (up to 4x C-PHY lanes)

required synchronization module not shown
Realization of "C-PHY-GUI" within M8070A SW

C-PHY Frame Generator integrated M8070 SW / M8000 BER solution

Definitions available for:
- Pattern & coding
- Low Power to High Speed mode transition
Realization of "C-PHY-GUI" within M8070A SW

C-PHY Frame Generator integrated M8070 SW / M8000 BER solution

Definitions available for:
- Pattern & coding
- Low Power to High Speed mode transition

Parameter editor for Impairments
Agilent / Keysight Solutions for MIPI RX PHY-test
2013 and before

M-PHY
J-BERT N4903B

D-PHY
ParBERT 81250
Agilent / Keysight Solutions for MIPI RX PHY-test

2015: Complete Solutions

**M-PHY**
- J-BERT N4903B

**C-PHY**
- AWG M8190A w/ M8085 special SW

**D-PHY**
- ParBERT 81250 w/ MATLAB script

M8000 family of BER test solutions
- J-BERT M8020A / M8070 / 85A
- AWG M8195A / M8070 / 85A

MIPI RX Testing – Today & Tomorrow
Page 69
Agenda

– MIPI Overview, history and recent changes
– RX test: recap of methodology
– M-PHY key features, changes in spec & methodology
– D-PHY recap of basics, signaling, LP- and HS- modes
– C-PHY intro on 3-wire 3-level signaling
– Keysight test solutions M8000 based
– Summary, links, QA
Advantages of Keysight Solution

– All PHY-standards to be addressed from M8000 platform
– CTS-conformant test setup, characterization and test
– Simple, repeatable automated and unattended calibration and test execution using automation SW N5990A opt 165
– Variety of error counting methods from BERT ED to IBER reader interface supported by N5990A test automation SW
– For M-PHY: direct match between J-BERT N4903B / M8020A capabilities and M-PHY required jitter cocktail
– Flexible Jitter generation to characterize RX beyond specifications to determine margins
– BitifEye Frame Generator SW BIT-2060-0001-0 allowing to choose and mix LP and HS traffic as in real application and to place custom data hassle-free into compliant M-PHY bursts
Summary

We discussed

– Goals of MIPI alliance
– Recent development and reasoning of PHY-layer standards
– Important capabilities and aspects of RX testing of different PHY-layers
– Introduction to C-PHY
– Rx test requirements, current and future keysight solutions
Literature

- www.keysight.com/find/J-BERT
- www.keysight.com/find/M8020A
- www.keysight.com/find/mipi-mphy
- http://mipi.org/
Keysight MIPI Total Solution Coverage

**Transmitter Characterization**
- DSAQ93204A Infinium
- U7238B D-PHY, U7249B M-PHY, N5467B C-PHY UDA
- InfiniiMax Probes
- Switch matrix
- N5465A InfiniiSim
- N2809A PrecisionProbe

Industry’s highest analog bandwidth, lowest noise floor/sensitivity, jitter measurement floor with unique cable/probe correction

**Receiver Characterization**
- N4903B/M8020A JBERT
- M8190 AWG
- 81250A ParBERT
- N5990A Automated characterization

Highest precision jitter lab source with automated compliance software for accurate, efficient, and consistent measurement

**Impedance/Return Loss Validation**
- E5071C ENA Option TDR
- DCA 86100D Wideband sampling oscilloscope
- N1055A TDR/TDT
- 54754A TDR/TDT

Precision impedance measurements and S-Parameter capability

**Protocol Stimulus and Analysis**
- U4421A D-PHY CSI-2 / DSI Analyzer and Exerciser
- U4431A M-PHY Analyzer (UFS, UniPro, CSI-3, SSIC, M-PCIe)
- Scope Protocol Decoder
  - N8802A CSI-2 / DSI
  - N8807A DigRF v4
  - N8808A UniPro
  - N8818A UFS
  - N8809A LLI
  - N8819A SSIC
  - N8820A CSI-3
  - N8824A RFFE

Fast upload and display, accurate capture, intuitive GUI and customizable hardware. Correlate physical and protocol layer.

**Keysight Technologies**
The End
Thank you!
Questions?

Contact:
Michael_Fleischer-Reumann@keysight.com
Phone: +49 7031 464 8420
# Three PHYs “at a glance”

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>M-PHY v3.1</th>
<th>D-PHY v1.2</th>
<th>C-PHY v1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Primary use case</strong></td>
<td>Performance driven, bidirectional packet/network oriented interface</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
<td>Efficient unidirectional streaming interface, with low speed in-band reverse channel</td>
</tr>
<tr>
<td><strong>HS clocking method</strong></td>
<td>Embedded Clock</td>
<td>DDR Source-Sync Clock</td>
<td>Embedded Clock</td>
</tr>
<tr>
<td><strong>Channel compensation</strong></td>
<td>Equalization</td>
<td>Data skew control relative to clock</td>
<td>Encoding to reduce data toggle rate</td>
</tr>
<tr>
<td><strong>Minimum configuration and pins</strong></td>
<td>1 lane per direction, dual-simplex, 2 pins each (4 )</td>
<td>1 lane plus clock, simplex, 4 pins</td>
<td>1 lane (trio), simplex, 3 pins</td>
</tr>
<tr>
<td><strong>Maximum transmitter swing amplitude</strong></td>
<td>SA: 250mV (peak)</td>
<td>LP: 1300mV (peak)</td>
<td>LP: 1300mV (peak)</td>
</tr>
<tr>
<td></td>
<td>LA: 500mV (peak)</td>
<td>HS: 360mV (peak)</td>
<td>HS: 425mV (peak)</td>
</tr>
<tr>
<td><strong>Data rate per lane (HS)</strong></td>
<td>HS-G1: 1.25, 1.45 Gb/s</td>
<td>80 Mbps to ~2.5 Gbps (aggregate)</td>
<td>80 Mbps to 2.5 sym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)</td>
</tr>
<tr>
<td></td>
<td>HS-G2: 2.5, 2.9 Gb/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>HS-G3: 5.0, 5.8 Gb/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(Line rates are 8b10b encoded)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Data rate per lane (LS)</strong></td>
<td>10kbps – 600 Mbps</td>
<td>&lt; 10 Mbps</td>
<td>&lt; 10 Mbps</td>
</tr>
<tr>
<td><strong>Bandwidth per Port (3 or 4 lanes)</strong></td>
<td>~ 4.0 – 18.6 Gb/s (aggregate BW)</td>
<td>Max ~10 Gbps per 4-lane port (aggregate)</td>
<td>Max ~ 17.1 Gbps per 3-lane port (aggregate)</td>
</tr>
<tr>
<td><strong>Typical pins per Port (3 or 4 lanes)</strong></td>
<td>10 (4 lanes TX, 1 lane RX)</td>
<td>10 (4 lanes, 1 lane clock)</td>
<td>9 (3 lanes)</td>
</tr>
</tbody>
</table>
Reference CTLE

Figure 42  Examples of CTLE Frequency Responses

<table>
<thead>
<tr>
<th>HS-RX Reference Equalizer</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{AC}$</td>
</tr>
<tr>
<td>$A_{DC}$</td>
</tr>
<tr>
<td>$f_z$</td>
</tr>
<tr>
<td>$f_{p2}$</td>
</tr>
</tbody>
</table>

$$H(s) = \frac{A_{DC} \omega_p \omega_{p2}}{\omega_z} \frac{s + \omega_z}{(s + \omega_p)(s + \omega_{p2})}$$
Reference CTLE and DFE

The DFE characteristics are defined by the following equation:

\[ y_k = x_k - V_{DFE\_RX} \]

\[ y_k = x_k - d_1 \text{sgn}(y_{k-1}) \]

(Equation 25)

where \( y_k \) is the output voltage signal of the DFE, \( x_k \) is the input voltage signal to the DFE, \( V_{DFE\_RX} \) is the DFE feedback voltage signal, \( k \) is the sample index of a data bit and \( d_1 \) is the DFE feedback coefficient. **Figure 43** illustrates the Reference DFE diagram.

**Figure 43  Reference DFE Diagram**

<table>
<thead>
<tr>
<th>HS-RX Reference Equalizer</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DFE_RX} )</td>
</tr>
</tbody>
</table>