ADS USB-3, PCIe-3 Test Benches with Waveform Bridge to Instrument Certified Compliance Test Applications

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Jian Yang, John LaDue
Keysight EEsof EDA

Keysight EEsof EDA Simulation Tools for Signal Integrity and Power Integrity

Advanced Design System
EMPro
SystemVue
What is Compliance Test Bench?

Design in ADS

PCI Express Test Report
Overall Result: PASS

Save simulated waveform

Run PCIe 3.0 Compliance Test Application

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Why Compliance Test Bench?

- Break the wall between Design Simulation and Lab Measurement
  - Exact same compliance software used for simulation and measurement
- Probing point is not accessible inside the IC chip
  - Equalization takes place inside the chip for SERDES devices
  - It must be simulated to show if the data can be recovered by the receiver
- Compliance Test Bench provides compliance validation before committing to hardware fabrication.
Agenda

1. High speed digital (HSD) physical layer (PHY) interface challenges
2. PCIe-3 PHY specification and ADS Compliance Test Bench (CTB)
3. USB-3 PHY specification and ADS CTB
4. Demo
5. Sneak preview of what’s coming
6. Call to Action
Zettabyte Era: Moving Data at 5-56 Gbps per Lane

HDTV
5x..10x more bandwidth than standard TV

Internet
YouTube uses as much bandwidth as the whole internet in 2000 (200 TBytes/day)

The Digital Home
Video-on-Demand, IPTV

Online Gaming
World of Warcraft, XBox360 etc.

Mobile Services
Mobile internet becomes affordable: iPhone, Video over Wireless Networks

Derivative Trader, Universities, Research labs
Data update 1-2 times/s High data exchange

Storage Area Networks
Broadband access will create new bandwidth demand (e.g. decentralized backup solutions)

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Impedance Discontinuity is Everywhere at Gbps Speed

Backplanes

Connectors

PC Boards

IC Packages

Cables
PCBs Are Critical Links in HSD Systems
Challenges in Serial Data Networks

High speed digital signals experience high frequency attenuation as they travel through a long lossy PCB channel. Clean, open, logical 1 & 0 at launch from transmitter. Logical 1 & 0 can be hard to distinguish at end of long interconnects; (this is often called a “closed eye”).

Fast, sharp, edges at transmitter launch. Smeared edges at end of long interconnect.

Circuit Board/Backplane

Circuit Board & Twisted Pair Differential Cable

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### PCIe Evolution

<table>
<thead>
<tr>
<th>PCIe Architecture</th>
<th>Raw Bit Rate</th>
<th>Interconnect Bandwidth</th>
<th>Bandwidth Lane Direction</th>
<th>Total Bandwidth for x16 link</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 1.1</td>
<td>2.5 GT/s</td>
<td>2 Gb/s</td>
<td>~250 MB/s</td>
<td>~8 GB/s</td>
</tr>
<tr>
<td>PCIe 2.0</td>
<td>5.0 GT/s</td>
<td>4 Gb/s</td>
<td>~500 MB/s</td>
<td>~16 GB/s</td>
</tr>
<tr>
<td>PCIe 3.0</td>
<td>8.0 GT/s</td>
<td>8 Gb/s</td>
<td>~1 GB/s</td>
<td>~32 GB/s</td>
</tr>
</tbody>
</table>

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## Key Features of PCIe

<table>
<thead>
<tr>
<th>Feature</th>
<th>PCI Express 2.0</th>
<th>PCI Express 3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit Rate</td>
<td>5 GT/s</td>
<td>8 GT/s</td>
</tr>
<tr>
<td>Encoding/Decoding</td>
<td>8B/10B</td>
<td>128B/130B</td>
</tr>
<tr>
<td>Overhead</td>
<td>20%</td>
<td>1.54%</td>
</tr>
<tr>
<td>Scrambling</td>
<td>Optional</td>
<td>Always</td>
</tr>
<tr>
<td>Effective Bit Rate</td>
<td>4Gb/s per lane</td>
<td>7.88Gb/s per lane</td>
</tr>
<tr>
<td>Transmission path</td>
<td>Same as Gen1</td>
<td>Same as Gen1 and Gen2</td>
</tr>
<tr>
<td>Receiver Testing</td>
<td>Informative</td>
<td>Required</td>
</tr>
</tbody>
</table>

- PCI Express 3.0 upgrades the encoding scheme to **128b/130b** from the previous **8b/10b** encoding.
- Reducing the overhead to approximately 1.54% \((130-128)/130\), as opposed to the 20% overhead of PCI Express 2.0.
- Uses “**Scrambling**” method of line encoding into channel.
PCIe Physical Layer: TX -> Channel -> RX

TxEQ – De-emphasis and Pre-shoot

RxEQ – CTLE

Figure 4-69: Loss Curves for Behavioral CTLE

RxEQ – DFE

Figure 4-70: Equation and Flow Diagram for 1-tap DFE
PCle 3.0: Transceiver IBIS-AMI Model Generation
PCle 3.0 IBIS-AMI models in ADS Channel Simulation

Tx_AMI Parameters

- Model_Specific
- SpecifyFilterBy
- Taps
- Preshoot_Deemphasis
- SSC_Deviation
- SSC_ModulationRate

Rx_AMI Parameters

- Model_Specific
- CTLE
- ON_OFF
- Factor
- RealPoles
- RealZeros
- CDR
- LoopFilter_Factor
- LoopFilter_RealPoles
- LoopFilter_RealZeros
- VCO_Sensitivity
- DFE
- InitCoefficients
- AdaptiveEQ
- Alpha
- LimitCoefficients
- CoefficientMaximums
- CoefficientMinimums
### PCIe 3.0 PHY Chip-to-Chip Simulation

![Diagram of PCIe 3.0 PHY Chip-to-Chip Simulation](image)

<table>
<thead>
<tr>
<th>Passive Interconnect Modeling</th>
<th>TX/RX Modeling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via Models</td>
<td>IBIS AMI</td>
</tr>
<tr>
<td>Connector S-Parameters</td>
<td></td>
</tr>
<tr>
<td>PCB Transmission Line</td>
<td></td>
</tr>
<tr>
<td>Package S-parameter Models</td>
<td></td>
</tr>
</tbody>
</table>

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Host Side: Tx_AMI, PCB traces, Via field

Device Side: Rx_AMI, Device PCB traces, Via field

Connector S-Parameters

PCle 3.0 Compliance Test Step-1: run simulation to generate waveforms
PCle 3.0 Compliance Test Step-2: launch PCle Compliance Test App

- Simulate PHY for electrical compliance, before any hardware prototype is made
- Same compliance tool to post-process simulated waveforms and measured waveform

Infiniium Offline and PCle Compliance Test App running on PC is the same software as what you use on your Oscilloscope
PCle 3.0 Compliance Test Application

- It represents a Test & Measurement vendor’s Method of Implementation (MOI), based on PCle 3.0 Compliance Test Specification (CTS)
- It usually runs on T&M vendor’s test instrument
- Keysight PCle 3.0 compliance test software runs on standalone PCs
PCIe 3.0 Compliance Test Step-3: run tests to generate test PASS/FAIL report

Summary of Results

<table>
<thead>
<tr>
<th>Test Statistics</th>
<th>Passed: 6</th>
<th>Failed: 0</th>
<th>Total: 6</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Margin Thresholds</th>
<th>Warning</th>
<th>Critical</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 2 %</td>
<td>0 %</td>
<td></td>
</tr>
</tbody>
</table>

PCI Express Test Report

Overall Result: **PASS**

Test Configuration Details

<table>
<thead>
<tr>
<th>Device Description</th>
<th>Device ID</th>
<th>Preset Type</th>
<th>Test Session Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Description</td>
<td>Device 1</td>
<td>None</td>
<td>Infiniium SW Version</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>05.50.0009</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Infiniium Model Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>N8900A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Infiniium Serial Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No Serial</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Application SW Version</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.42</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Debug Mode Used</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Last Test Date</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2015-05-21 16:33:52 UTC +05:30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Actual Value</th>
<th>Margin %</th>
<th>Pass Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Clock, Clock Frequency (Data Clock) PCIe 3.0, 8.0 GHz</td>
<td>100.01 MHz</td>
<td>0.0 %</td>
<td>100.00 MHz &lt;= VALUE &lt;= 100.02 MHz</td>
</tr>
<tr>
<td>System Board Tx, Test Vectors PCIe 3.0, 8.0 GHz</td>
<td>125.0000 ps</td>
<td>0.0 %</td>
<td>124.5000 ps &lt;= VALUE &lt;= 125.5000 ps</td>
</tr>
<tr>
<td>System Board Tx, Pinsense Test PCIe 3.0, 8.0 GHz</td>
<td>Pass</td>
<td>0.0 %</td>
<td>100.0 % Pass</td>
</tr>
<tr>
<td>System Board Tx, Peak Differential Output Voltage (Transition) PCIe 3.0, 8.0 GHz</td>
<td>65.8 mV</td>
<td>2.0 %</td>
<td>64.0 mV &lt;= VALUE &lt;= 67.6 mV</td>
</tr>
<tr>
<td>System Board Tx, Peak Differential Output Voltage (Non Transition) PCIe 3.0, 8.0 GHz</td>
<td>61.9 mV</td>
<td>2.4 %</td>
<td>60.0 mV &lt;= VALUE &lt;= 63.8 mV</td>
</tr>
<tr>
<td>System Board Tx, Eye Metric PCIe 3.0, 8.0 GHz</td>
<td>111.13 ps</td>
<td>0.4 %</td>
<td>96.4 % VALUE &lt;= 41.25 ps</td>
</tr>
</tbody>
</table>
USB Evolution

USB 2.0 (2000)
- 480Mb/s
- NRZ
- 1 bi-directional link
- 4 signals (D+, D-, VBUS, GND)

USB 3.0 (2008)
- 5Gb/s
- 8B/10B coded
- 2 uni-directional links
- 4 additional signals
- Backward compatible with 2.0

USB 3.1 (2013)
- 10Gb/s
- 128B/132B coded
- Same links and pins as 3.0
- Backward compatible with 2.0 and 3.0
USB 3.1: Gen1 vs Gen2 Comparison

<table>
<thead>
<tr>
<th></th>
<th>Gen1</th>
<th>Gen2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data rate</strong></td>
<td>5 Gb/s</td>
<td>10 Gb/s</td>
</tr>
<tr>
<td><strong>Encoding</strong></td>
<td>8b/10b</td>
<td>128b/132b (20% additional bandwidth over 8b/10b)</td>
</tr>
<tr>
<td><strong>Tx REF EQ</strong></td>
<td>Normative Post: -3 dB</td>
<td>Informative Pre: 2.7 dB Post: -3.3 dB</td>
</tr>
<tr>
<td><strong>Rx REF EQ</strong></td>
<td>CTLE</td>
<td>CTLE (6 level) + 1 tap DFE</td>
</tr>
<tr>
<td><strong>CDR (JTF BW)</strong></td>
<td>4.9 MHz</td>
<td>7.5 MHz</td>
</tr>
<tr>
<td><strong>Eye Height / Mask</strong></td>
<td><img src="image1.png" alt="Gen1 eye mask" /></td>
<td><img src="image2.png" alt="Gen2 eye mask" /></td>
</tr>
<tr>
<td><strong>TJ</strong></td>
<td>132 psec (0.66 UI)</td>
<td>71.4 psec (0.714 UI)</td>
</tr>
<tr>
<td><strong>Target Channel</strong></td>
<td>3 meter (-17 dB @ 2.5 GHz)</td>
<td>1 meter (-20 dB @ 5 GHz)</td>
</tr>
</tbody>
</table>
USB 3 Compliance Channel

Used to test for worst case channel conditions

**USB 3.0 Compliance Channels**
- **Standard connector:**
  - Channel loss will dominate
  - 11” PCB trace for device testing
  - 5” PCB trace for host testing
  - 3 meter USB 3.0 cable
- **Micro connector:**
  - Channel loss will dominate
  - 11” PCB trace for device testing
  - 5” PCB trace for host testing
  - 1 meter USB 3.0 cable
- **Tethered:**
  - Channel loss will dominate
  - 11” PCB trace for device testing
  - 5” PCB trace for host testing
  - short USB 3.0 cable

**USB 3.1 Compliance Channels**
- **Reference Host + Cable Assembly + Reference Device**
  - 7 dB
  - 6 dB
  - 7 dB

- Die to die target is 20 dB @ 5 GHz
- Symmetric loss for host and device
- Host/device exceeding 7 dB may need repeater

**Short Channel:**
- no cable and shortest possible PCB traces
USB 3 Compliance Test Bench

Step 1: Generate Simulated Waveforms in ADS
USB 3 Compliance Test Bench

Step 2: Load ADS waveforms in the USB Compliance App
USB 3.1 Compliance Test Bench

Step 3: Run compliance tests and view results
Demo
ADS Simulation for 100GBASE-CR4 and -KR4
Summary

– PCIe 3: PHY operating at 8GT/s on x1, x2, x4, x16 lanes
– USB 3: PHY operating at 10Gb/s over cable, connector and PCB
– 100GbE: PHY operating at 25Gb/s per lane on 4 lanes
– Closed eye at Rx input pin: Tx EQ and Rx CTLE/DFE needed to open the eye
– Simulate various channel conditions and equalization settings for robust design
– Simulated waveforms are used to run the same compliance tests as those on a scope
Take Action!

– Try it for yourself!
  • Download this presentation and try out the demos at: www.keysight.com/find/eesof-hsd-seminar

– Contact your Keysight representative for licensing and questions.