DDR5 is Coming! Are You Ready?

Keysight EEsof EDA
May, 2017
JEDEC Preview DDR5 in June 2017

JEDEC DDR5 & NVDIMM-P Standards Under Development

Preview both at JEDEC’s Server Forum in June 2017

ARLINGTON, Va., USA – MARCH 30, 2017 –JEDEC Solid State Technology Association, the global leader in the development of standards for the microelectronics industry, today announced that development of the widely-anticipated DDR5 (Double Data Rate 5) and NVDIMM-P Design standards is moving forward rapidly. Publication for both is forecasted for 2018. Industry users will have the opportunity to learn more about each standard at JEDEC’s Server Forum event in Santa Clara, CA on Monday, June 19, 2017. For more information and to register, visit the JEDEC website.

**DDR5 will provide double the bandwidth and density over DDR4, Speed will increase from 3.2Gbps to 6.4Gbps**
Challenges for DDR5

Challenge #1  Timing margin will be further eroded by ISI and RJ, stressed eye specs must comprehend BER at prescribed confidence intervals (1E-16 BER for DDR4).

**Question:** Is SPICE-Like simulation still practical for system margins prediction at ultra-low BER?  **Answer is NO!**

![Image of eye diagrams and measurement data](image-url)
Challenges for DDR5

Challenge #2: Channel attenuation becomes more significant so **tunable equalizations** become necessary to deal with closed eyes

**Question:** How to account for tunable equalizations in DDR simulation?
SPICE-Like Sim vs. Statistical Sim

- **SPICE-Like (Transient) Approach**
  - 1 million bits is required to do jitter separation and predict eye opening accurately at low BER

- **Statistical Approach**
  - Widely used for SERDES design for over 10 years
  - Calculation for eye probabilities at ultra low BER in seconds without running an actual bit sequence

---

32 bits Tran Sim 119 sec  
1066 bits Tran Sim 4636 sec  
Ultra-low BER Statistical Sim 42 sec
Why Statistical Approach is Fast?

Statistical methodology assumes the system to be LTI (Linear Time Invariant)

1. Transient analysis to get step responses of the channel for both rise and fall edge
2. The Linear Superposition Method is used to directly compute the eye probability distributions of a conceptually infinite non-repeating bit pattern

- Accurate BER prediction in a very short amount of time.
- The duty-cycle-distortion (DCD), periodic jitter (PJ), random jitter (RJ), crosstalk and ISI are calculated accurately by the statistical approach.
Question: Power supply noise is time variant, how to capture its effect with the statistical approach?
Solution - Mask Correction Factor (MCF)

- **Definition of MCF:**
  - EH and EW shrinkages induced by the power supply noise only.

- **Steps to extract MCF:**
  - Run *Transient simulations* on two cases, one with PDN and the other without PDN.
  - Find the EH and EW values at the expected BER level respectively.
  - Extract the MCF by subtracting the values of these two cases.
    - EH difference – Amplitude MCF
    - EW difference – Jitter MCF

<table>
<thead>
<tr>
<th>Amplitude MCF</th>
<th>Jitter MCF</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 mV</td>
<td>19 ps</td>
</tr>
</tbody>
</table>
Usage of Mask Correction Factor (MCF)

- Apply to the mask data to compensate power supply noise for the statistical analysis
- Correct the eye height and eye width value at a certain BER level

Example:

<table>
<thead>
<tr>
<th></th>
<th>Amplitude MCF</th>
<th>Jitter MCF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Original Mask</td>
<td>25 mV</td>
<td>19 ps</td>
</tr>
<tr>
<td>Corrected Mask</td>
<td>0.24 UI</td>
<td>19 ps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>DDR4 DQ Mask in JEDEC Spec</th>
<th>New DQ Mask After Correction factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>EW</td>
<td>0.2 UI</td>
<td>0.24 UI</td>
</tr>
<tr>
<td>EH</td>
<td>130 mv</td>
<td>155 mv</td>
</tr>
</tbody>
</table>
Solution Validation

- **Xilinx® KCU 105 FPGA Platform Board**
  - 9.27 x 5 inch, 16 layers PCB

- **DDR4 Memory**
  - 2.4 GB Micron DDR4 memory (4 banks)

- **Measurement Setup:**
  - Keysight’s DSAV334A Infinium Oscilloscope
  - N6462A DDR4 Compliance Test Application
  - Measured at 2400 Mbps speed grade with 109 million bits, which is close to $1e^{-8}$ BER
- PCB EM Modeling
  - Pure 3D EM engine (ADS SIPro) was used to extract accurate EM models for PCB
  - Include only one I/O Bank (16 bits) for a faster EM model generation assuming minimal crosstalk between I/O banks
- DDR Bus Simulation (Statistical Approach)
  - @ BER = 1e^{-8} EH = 374 mV, EW = 356 ps
  - @ BER = 1e^{-16} EH = 367 mV, EW = 348 ps
Side-By-Side Comparison

- **Statistical analysis vs. measured comparison:**
  - Reasonable agreement
  - Larger amplitude and jitter noise with the measured data due to the power supply noise contribution
MCF Extraction for KCU105 Board

- MCF Extraction
  - Pre-layout models used for the channel
  - Transient Simulation w/ and w/o PDN on 64 DQ lines with 5K bits

![MCF Extraction Graph]

<table>
<thead>
<tr>
<th></th>
<th>Amplitude MCF</th>
<th>Jitter MCF</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/ PDN</td>
<td>94 mV</td>
<td>16 ps</td>
</tr>
<tr>
<td>Wo/ PDN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Cisco, Keysight, Keysight Technologies
Correlation with MCF Applied

- Excellent agreement:
  - 2% eye width difference on simulation vs. measured @ $1 \times 10^{-8}$ BER
  - 2.2% eye height difference on simulation vs. measured @ $1 \times 10^{-8}$ BER

<table>
<thead>
<tr>
<th></th>
<th>DDR BUS Sim Result @ $1 \times 10^{-16}$ BER</th>
<th>DDR BUS Sim Result @ $1 \times 10^{-8}$ BER</th>
<th>Measurement Result (@$1 \times 10^{-8}$ BER)</th>
<th>Sim/Measure Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>W/O MCF</td>
<td>With MCF</td>
<td>W/O MCF</td>
<td>With MCF</td>
</tr>
<tr>
<td>Eye Width</td>
<td>323 ps</td>
<td>307 ps</td>
<td>348 ps</td>
<td>332 ps</td>
</tr>
<tr>
<td>Eye Height</td>
<td>360 mv</td>
<td>266 mv</td>
<td>371 mv</td>
<td>277 mv</td>
</tr>
</tbody>
</table>

Compared
Corrected Mask – Still Within Spec!

<table>
<thead>
<tr>
<th>Amplitude MCF</th>
<th>Jitter MCF</th>
</tr>
</thead>
<tbody>
<tr>
<td>94 mV</td>
<td>16 ps</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>measurement</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>WidthAtBER</td>
<td>3.229E-10</td>
</tr>
<tr>
<td>HeightAtBER</td>
<td>0.360</td>
</tr>
<tr>
<td>TimingMarginUL</td>
<td>6.771E-11</td>
</tr>
<tr>
<td>TimingMarginUR</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>TimingMarginLL</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>TimingMarginLR</td>
<td>6.354E-11</td>
</tr>
<tr>
<td>VoltageMarginUL</td>
<td>0.028</td>
</tr>
<tr>
<td>VoltageMarginUR</td>
<td>0.065</td>
</tr>
<tr>
<td>VoltageMarginLL</td>
<td>0.034</td>
</tr>
<tr>
<td>VoltageMarginLR</td>
<td>0.071</td>
</tr>
<tr>
<td>MinVoltageMarginU</td>
<td>0.028</td>
</tr>
<tr>
<td>MinVoltageMarginL</td>
<td>0.034</td>
</tr>
</tbody>
</table>

**DDR4 DQ Mask in JEDEC Spec**
- **Eye Width**: 0.2 UI
- **Eye Height**: 130 mv

**New DQ Mask After Correction factor**
- **Eye Width**: 0.23 UI
- **Eye Height**: 224 mv
Accurate Statistical-Based DDR4 Margin Estimation using SSN Induced Jitter Model

Hee-Soo LEE, Keysight Technologies
Cindy Cui, Keysight Technologies
Heidi Barnes, Keysight Technologies
Luis Boluna, Keysight Technologies

Why Equalizations are Necessary for DDR5?

A Typical DDR System & Channel Attenuation

DDR Channel Attenuation becomes more significant as data rate increases!
How to Model Equalizations in Single-ended IBIS?

Solution -- ADS DDR Equalization Models

- ADS DDR Tx and Rx Equalization Models
  - Work with IBIS model in Statistical DDR BUS Simulation
  - Support De-emphasis, CTLE, Optimized DFE and FFE
Equalizations in Real DDR4 Design


Solution Validation

→ Functional Eye Measurement.

→ **Functional Eye width** = 310.8ps.
→ **Jitter** = 416 - 310.8ps = 105.2ps

Post CTLE DQ Eye Jitter with Power Supply Noise

Conclusion

- **Statistical simulation approach** is a must for DDR4/DDR5 to predict ultra-low BER eye in an efficient and timely manner.

- The **Mask Correction Factor** (MCF) method is proposed to capture the power supply noise with DDR statistical simulation and to estimate the timing and voltage margins accurately.

- Channel Attenuation becomes more significant and **tunable equalizations** become necessary for DDR5.

- **ADS DDR Tx/Rx Equalization** models have been used in real DDR4 design to simulate equalizations with single-ended IBIS models.

- Great correlation were shown between the Statistical simulation approach and measurements.
Want More Resources?

ADS Bundle Used for DDR4/DDR5 Analysis:
- W2223BP ADS Core, TransConv, Channel, CILD, Layout, SIPro, PIPro Bundle
- W2309EP DDR Bus Simulator

Signal Integrity & Power Integrity Resources
- www.keysight.com/find/eesof-ads-sipi-resources
- www.keysight.com/find/eesof-tutorials-signal-integrity

Try it for free for 30 days with absolutely no obligation.
- www.keysight.com/find/hsdswtrials
Thank you!

QUESTIONS?